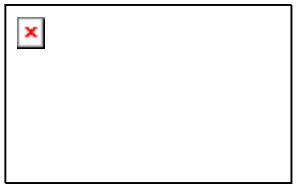

The University of New Mexico

Stochastic Interconnect Layout Sensitivity Model

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** Abbott Diabetes Care, Alameda, CA 94502*

Outline

1. *Overview of Process Defects*
2. *Definition of "Layout Sensitivity"*
3. *Statistical Layout Sensitivity Model*
4. *Application in VLSI design/verification process*
5. *Conclusions*

Outline

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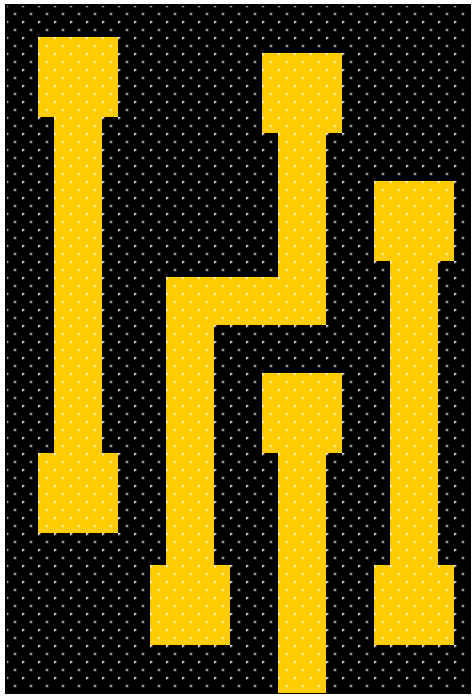
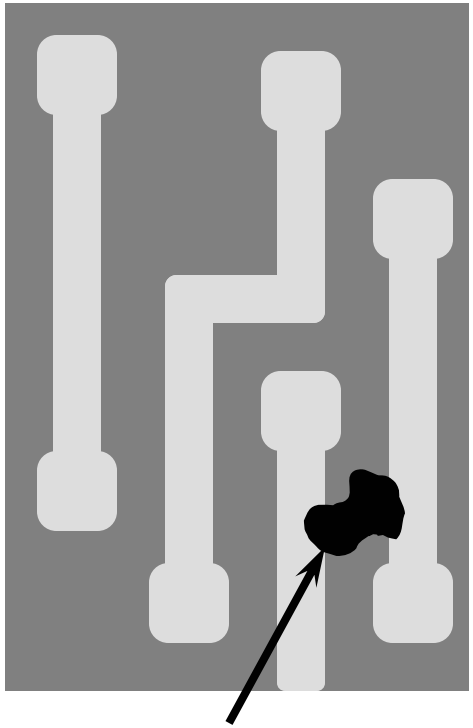
Process Defects and Yield Loss

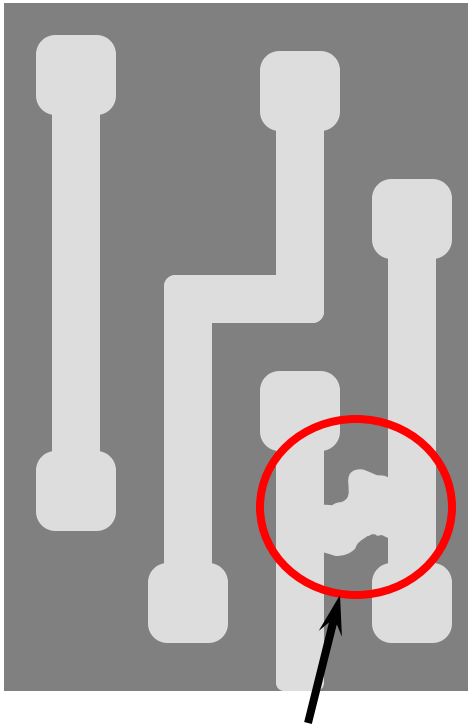
Process Defect Causing Fault (Short)



Original layout



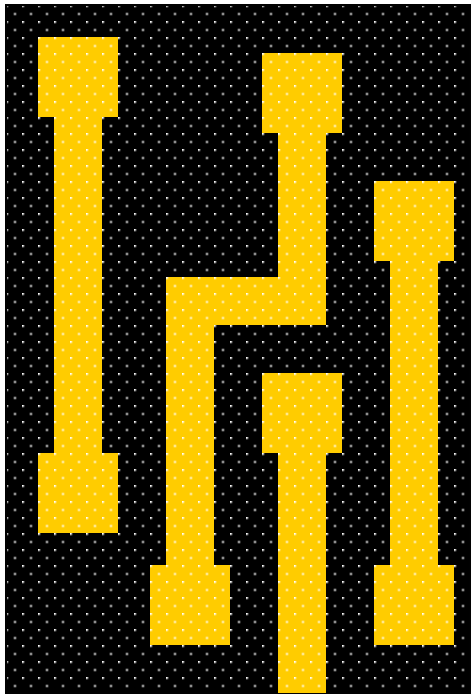
A particle or a process defect



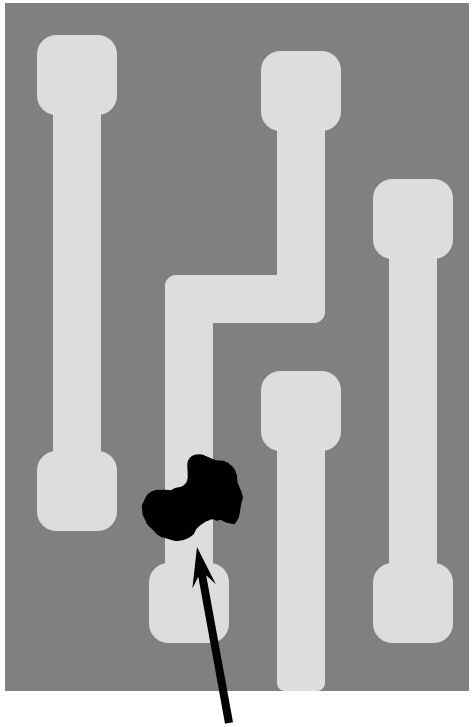
Short defect

Process Defects and Yield Loss

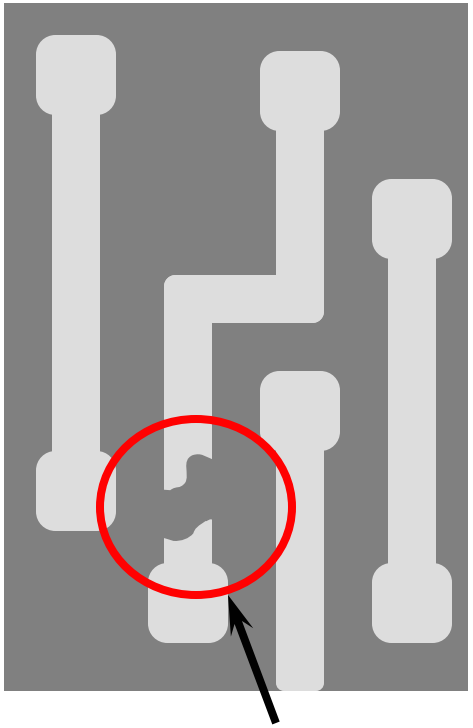
Process Defect Causing Fault (Opens)



Original layout

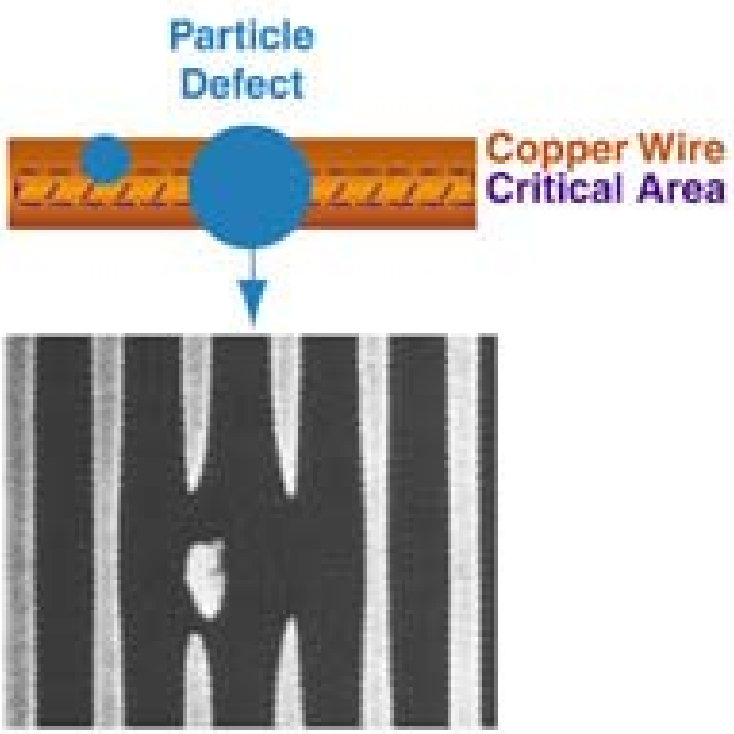


A particle or a process defect

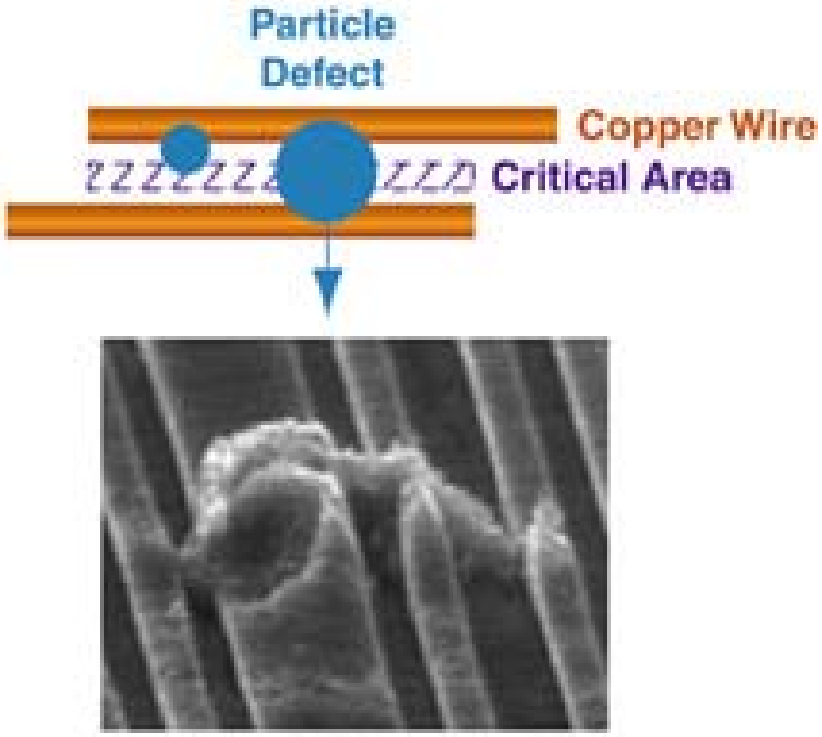


open defect

Process Defect Photographs



Open Circuit



Short Circuit

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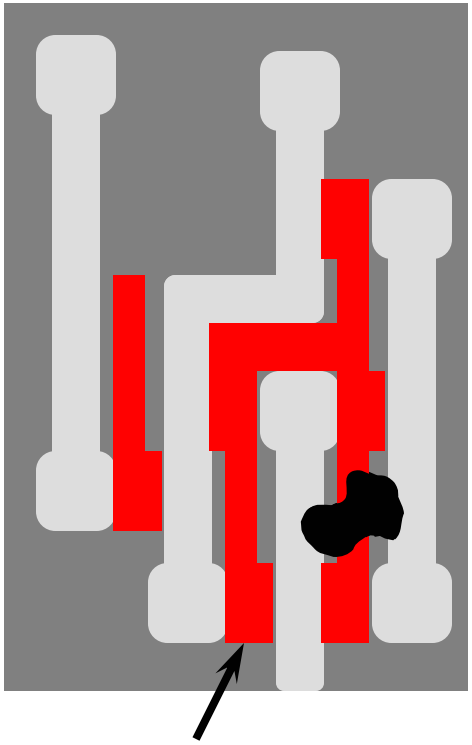
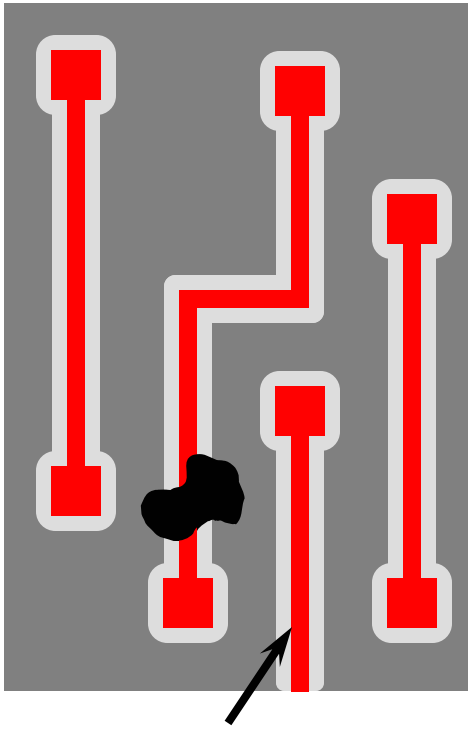
Critical Area and Layout Sensitivity

Short defects



Critical area for short defects

Open defects



Critical area for open defects

What is challenging?

- For yield analysis, layout sensitivity must be calculated for a range of defect sizes.
- Extraction of layout sensitivity in a real chip requires extensive computations, which makes it a very time consuming process.
- Statistical model can expedite the process significantly.

Critical Area Analysis Methods

- ***Geometric Methods:*** Compute the area of critical region for every defect size and for every rectangular element in layout using *shape-expansion*, *shape-overlap*, and *shape-intersection* → needs extensive computation

- ***Monte Carlo Simulation:*** Draw a large number of defects with their radii distributed, check for each defect if it causes an failure, and divide the number of defects causing faults by the total number of defects to derive the probability of fault → not accurate with small number of samples

- ***Grid Method:*** Assume an integer grid over the layout and compute the critical radius at every grid point → not accurate with small number of grids

- ***Stochastic Method:*** Compute layout sensitivity from statistical features of the layout using analytical model → generic but very fast, *excellent for prediction*

History Layout Sensitivity

- B. R. Mandava, "Critical area for yield models," IBM, East Fishkill, NY, Tech. Rep. TR22.2436, January ***1982***.
- W. Maly and J. Deszczka, "Yield estimation model for VLSI artwork evaluation," Electron Lett., vol. 19, no. 6, pp. 226–227, March ***1983***.
- A. V. Ferris-Prabhu, "Defect size variations and their effect on the critical area of VLSI devices," IEEE J. Solid-State Circuits, vol. SC-20, pp. 878–880, Aug. ***1985***.
- . . . . . .
- A. Nicoli, "Signoff Evolves From Design-Rule Checking To Yield Analysis," Electronic Design, July 24 ***2006***, http://elecdesign.com/Articles/ArticleID/13132/13132.html
- J. Yan, B. Chiang, "Timing-Constrained Yield-Driven Wiring Reconstruction for Critical Area Minimization," International Conference on Embedded Systems, pp. 899-906, January ***2007***

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Preliminary Analysis

Assumptions:

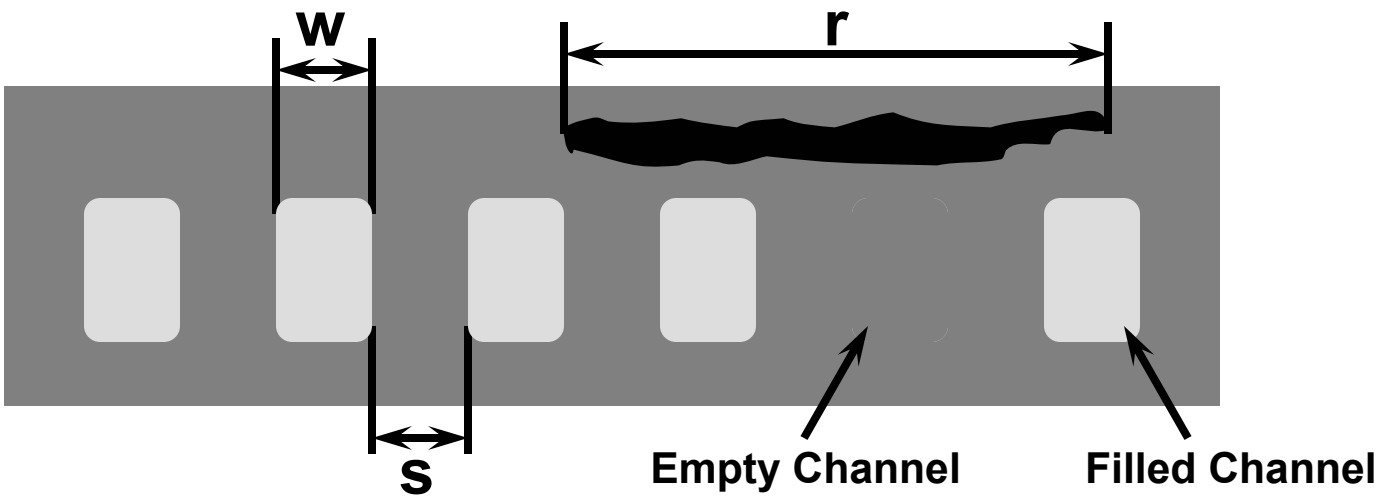
- Interconnects are placed on grids
- Layout is represented by a 1D system
- Defect is approximated by a rectangle

Our Goal:

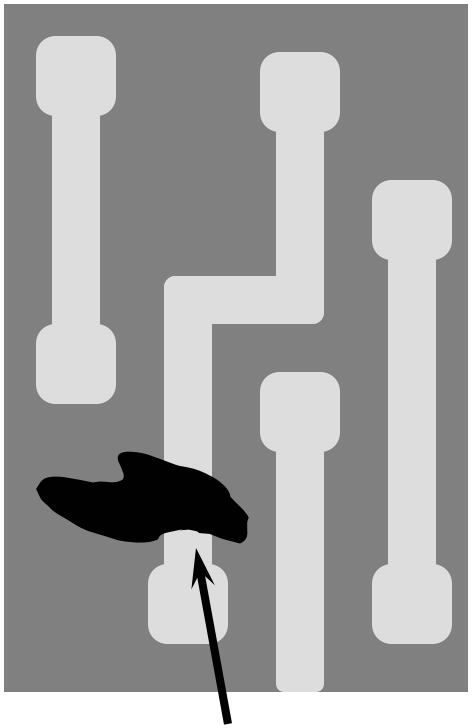
Layout Sensitivity = Probability of Failure

Definitions

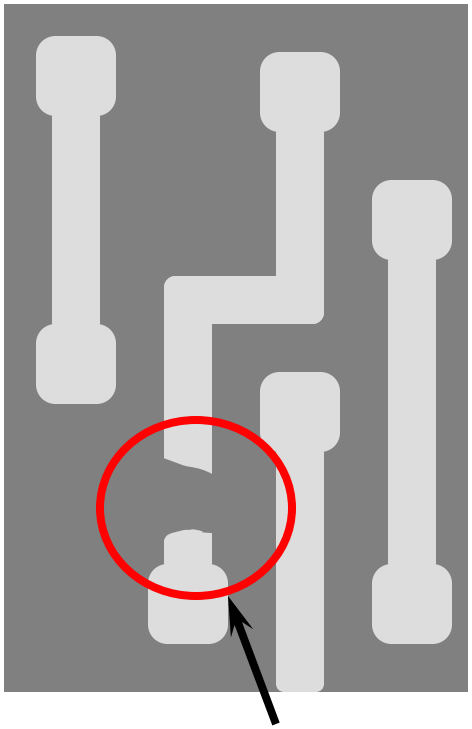
w	Interconnect width
s	Interconnect spacing
r	Defect radius
d	Probability of filled channel
1-d	Probability of empty channel



Process Defects for Opens



A particle or
a process defect



open defect

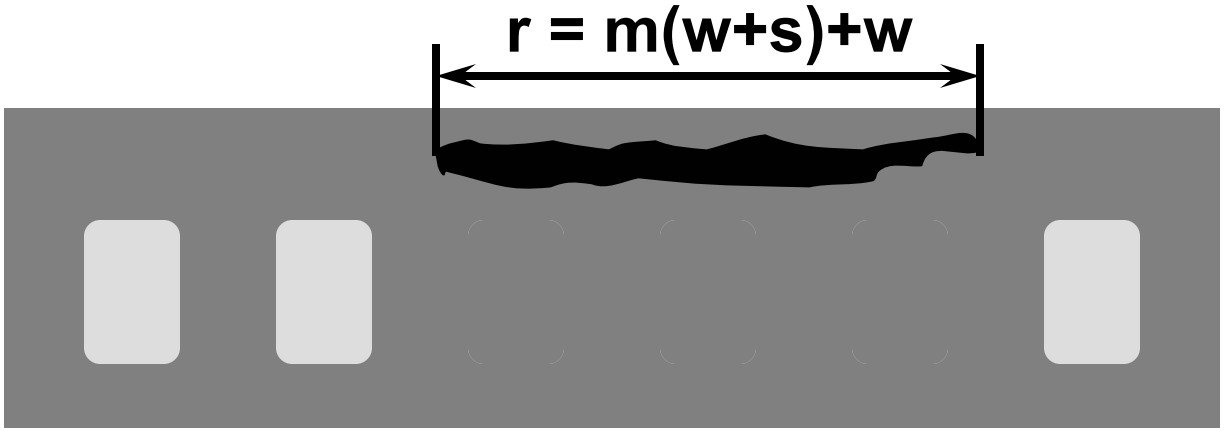
Layout Sensitivity for Opens

Defect size $r = m(w+s)+w$

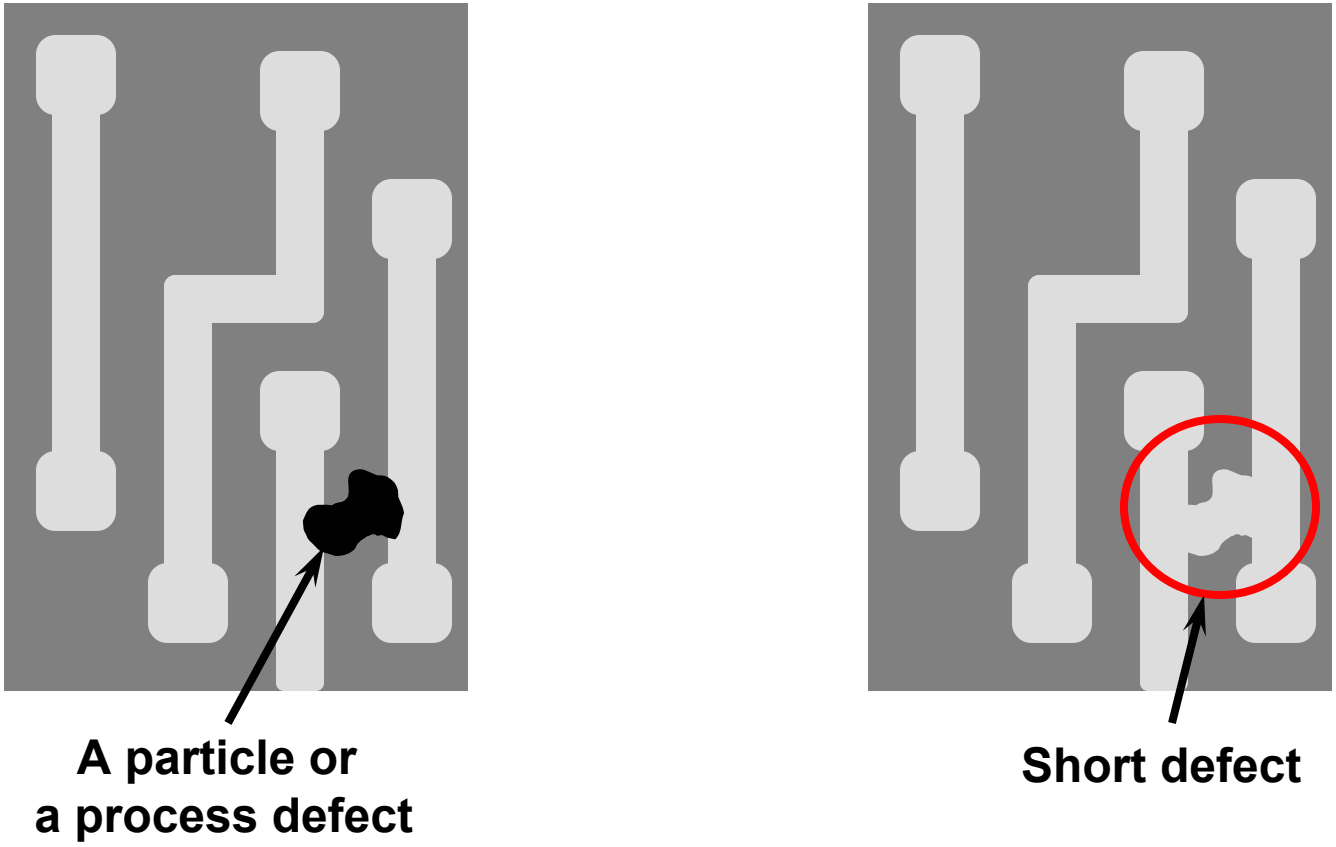
Survival probability $P_s = (1-d)^m$

Failure probability $P_f = 1 - (1-d)^m$

Layout Sensitivity $S_o = 1 - \left(1 - d\right)^{\frac{r-w}{w+s}}$



Process Defects for Shorts



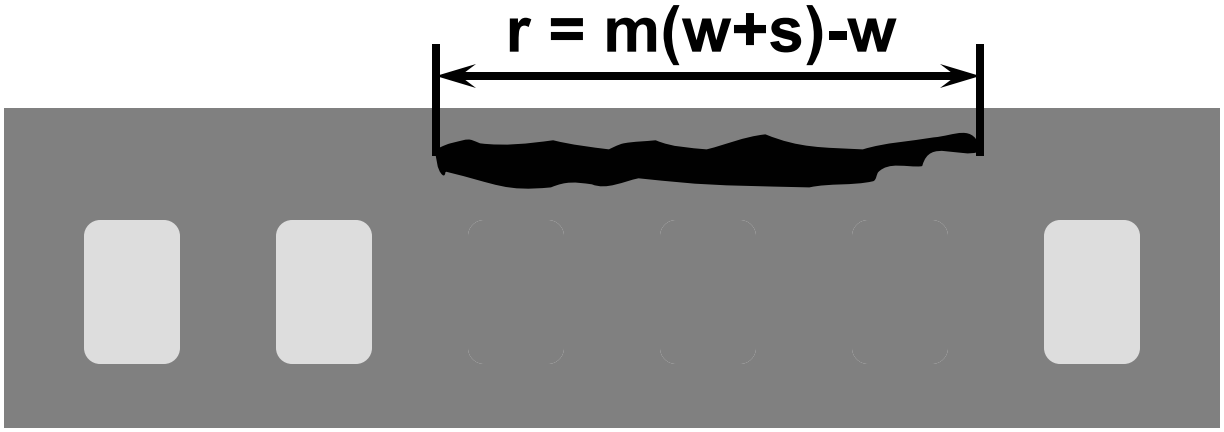
Layout Sensitivity for Shorts

Defect size $r = m(w+s)-w$

Survival probability $P_s = (1-d)^m + m \cdot d \cdot (1-d)^{(m-1)}$

$(1-d)^m$: **m empty channel**

$m \cdot d \cdot (1-d)^{(m-1)}$: **1 filled and (m-1) empty channel**



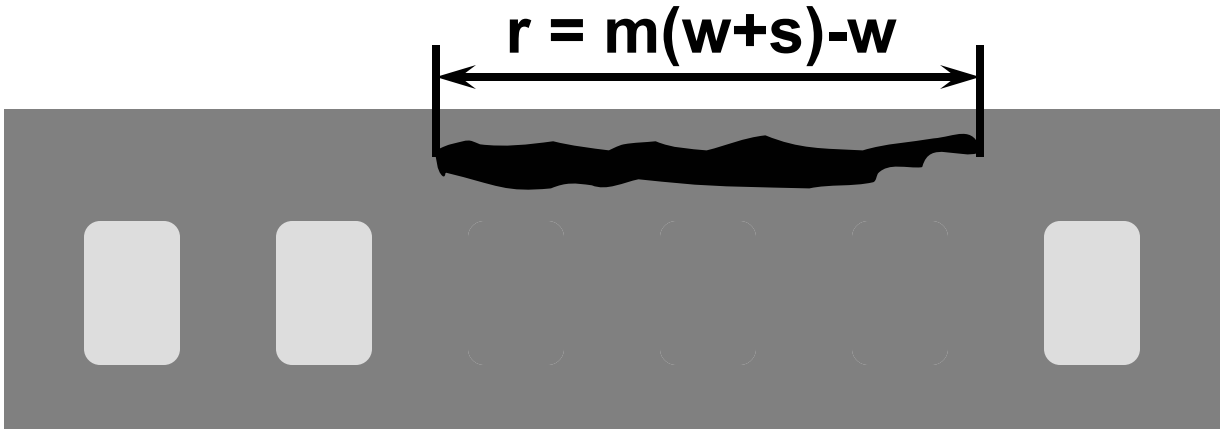
Layout Sensitivity for Shorts

Defect size $r = m(w+s)-w$

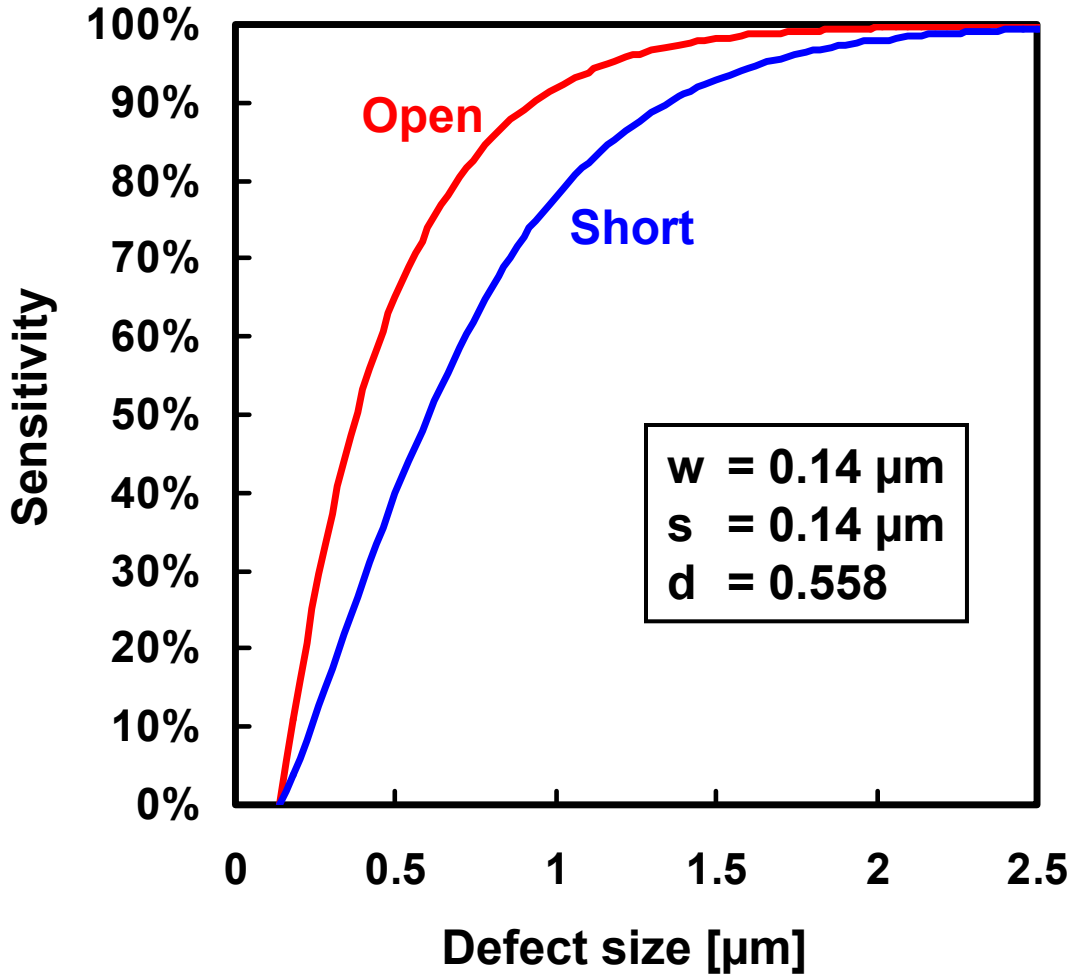
Survival probability $P_s = (1+(m-1)d)(1-d)^m$

Failure probability $P_f = 1 - (1+(m-1)d)(1-d)^m$

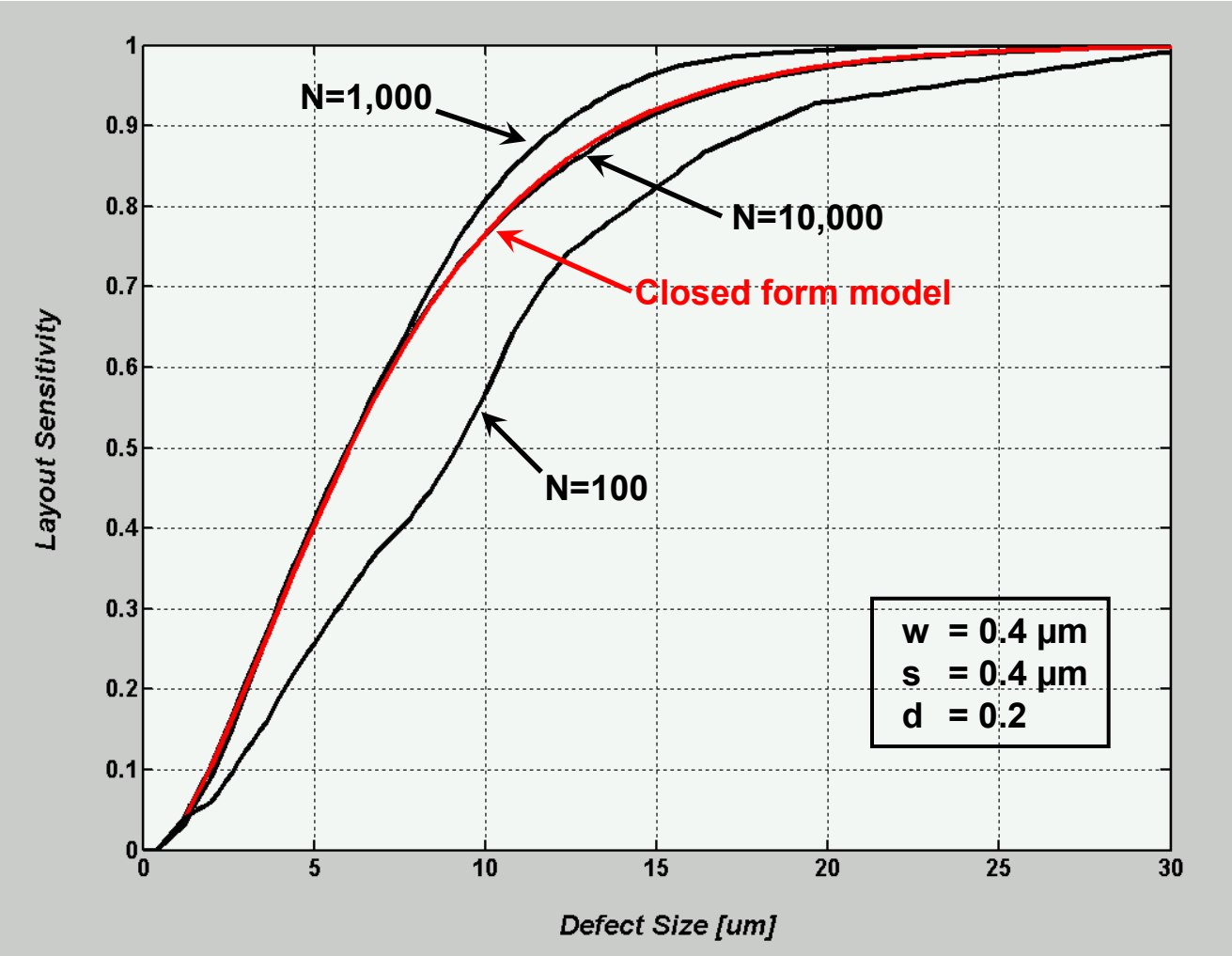
Layout Sensitivity $$S_s = 1-\left(1+\left(\frac{r-s}{w+s}\right)d\right)\left(1-d\right)^{\frac{r-s}{w+s}}$$



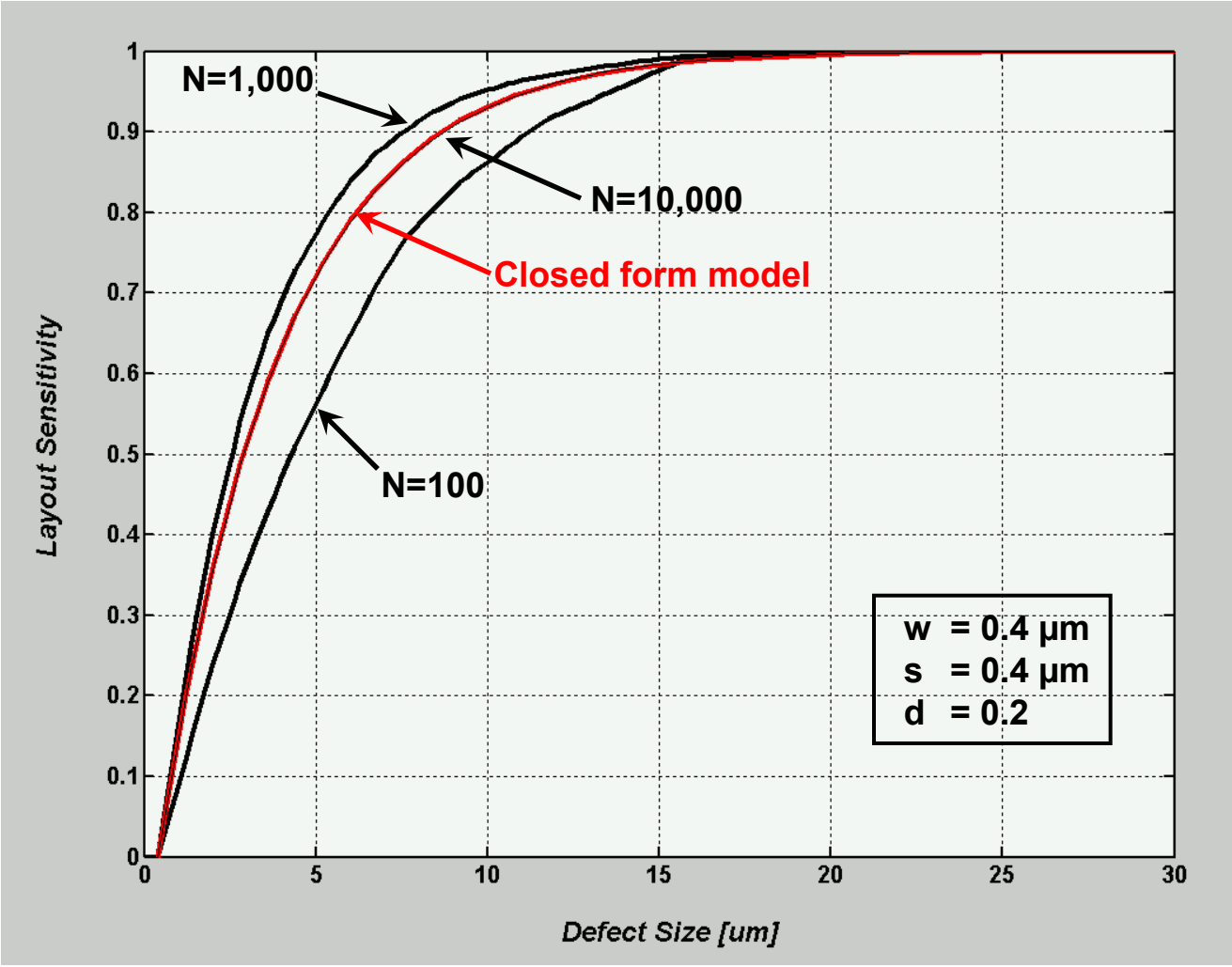
Layout Sensitivity versus Defect Size



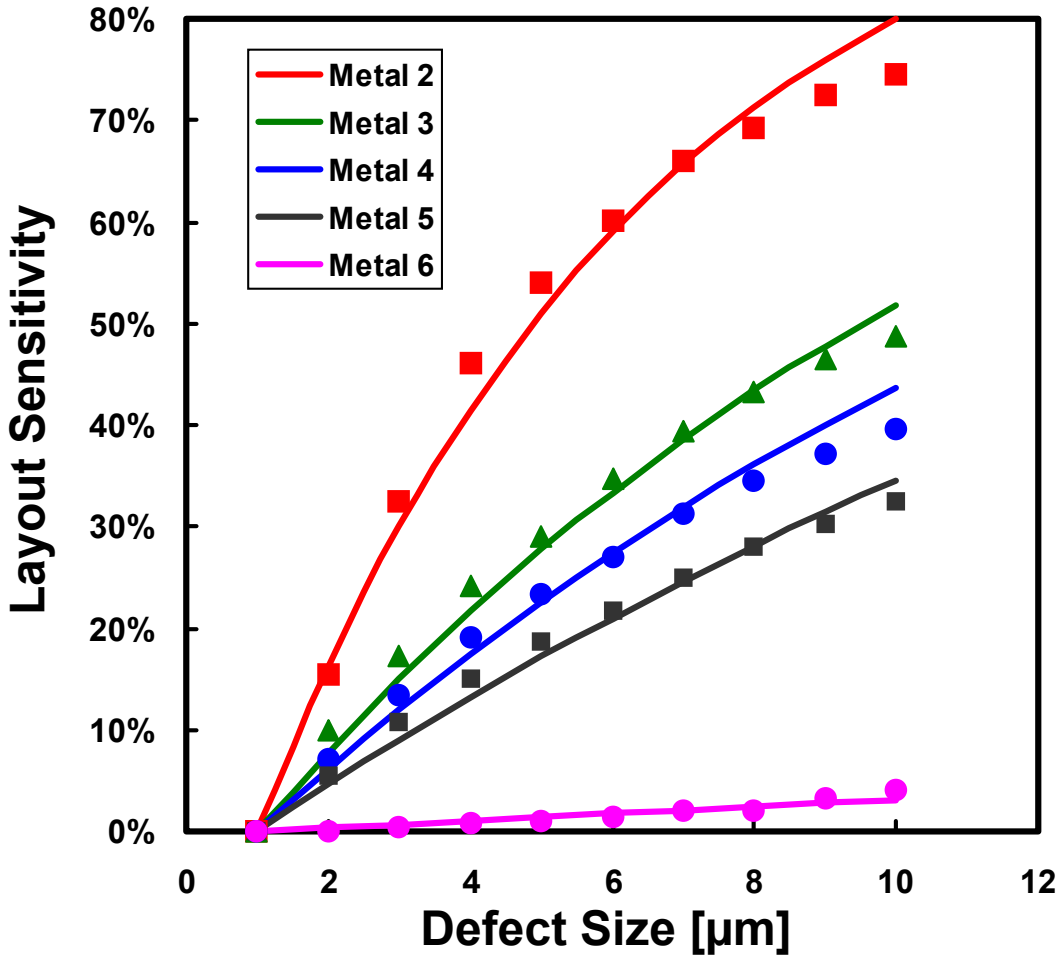
Mote-Carlo Simulation Results for Shorts



Mote-Carlo Simulation Results for Opens



Example for Opens in a Real Chip



Data from: J. Segal, L. Milor, and Y. Peng, "Reducing baseline defect density through modeling random defect-limiting yield," Micro Magazine, Jan 2000

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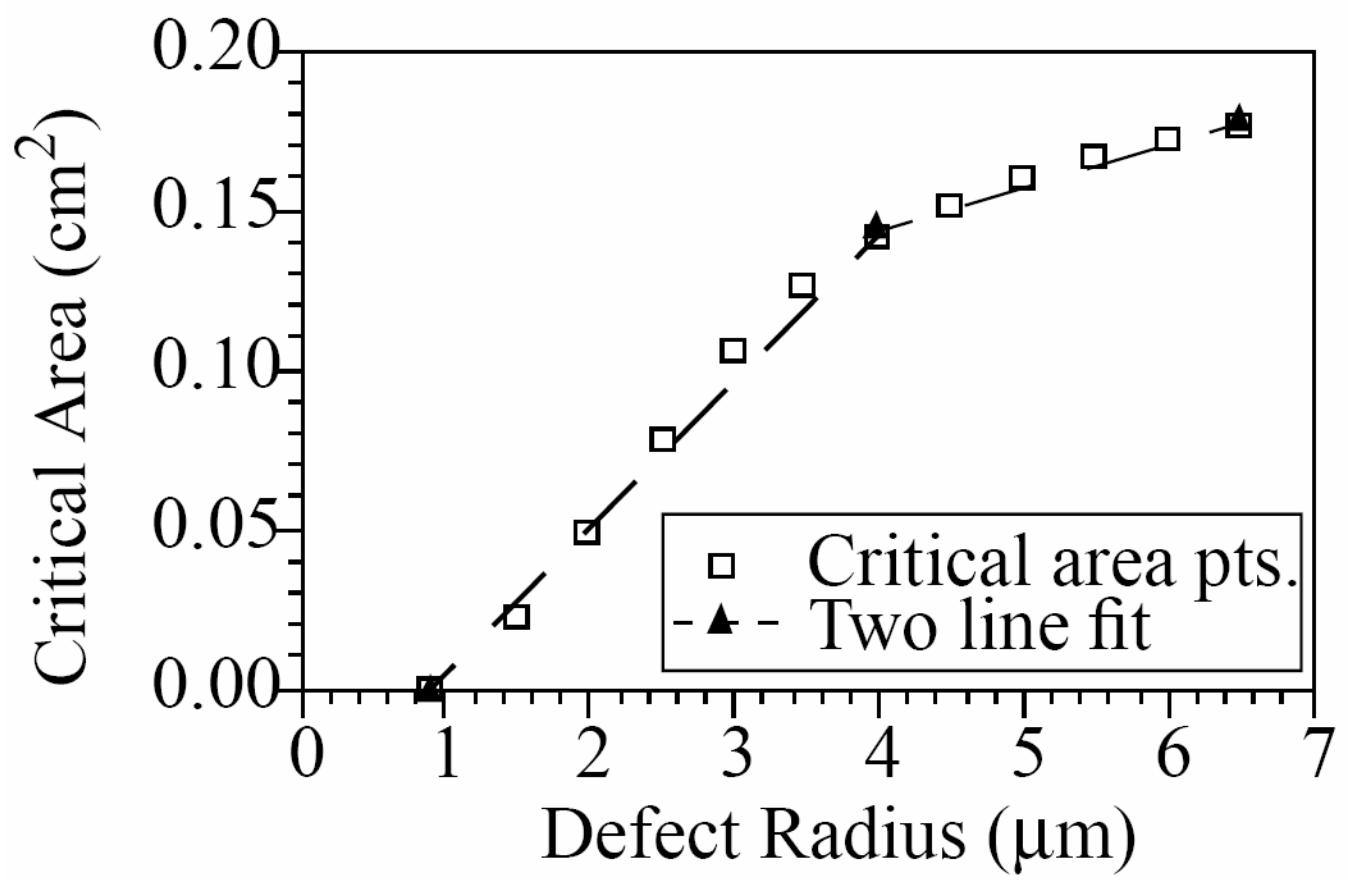
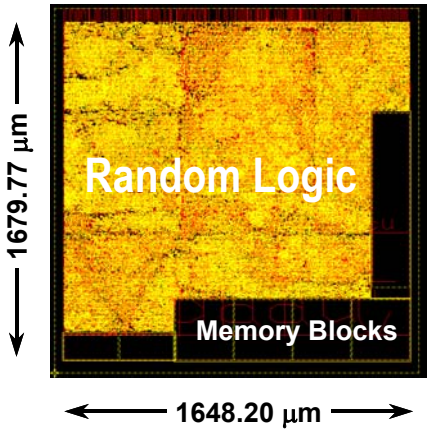
Application 1: Prediction of Layout Sensitivity

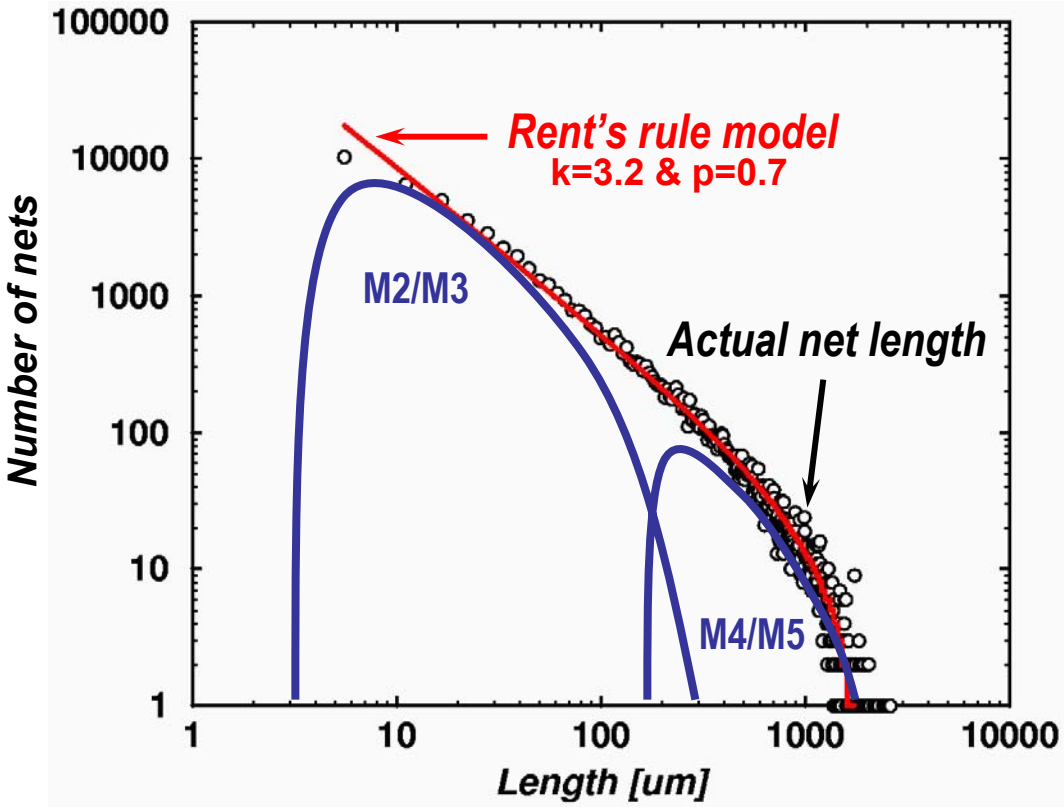


H. Heineken and W. Maly, "Performance-Manufacturing Tradeoffs in IC Design," DATE 1998

Wire Length Distribution



Number of logic gate = 200,000
Number of metal layer = 6
Technology = 130 nm

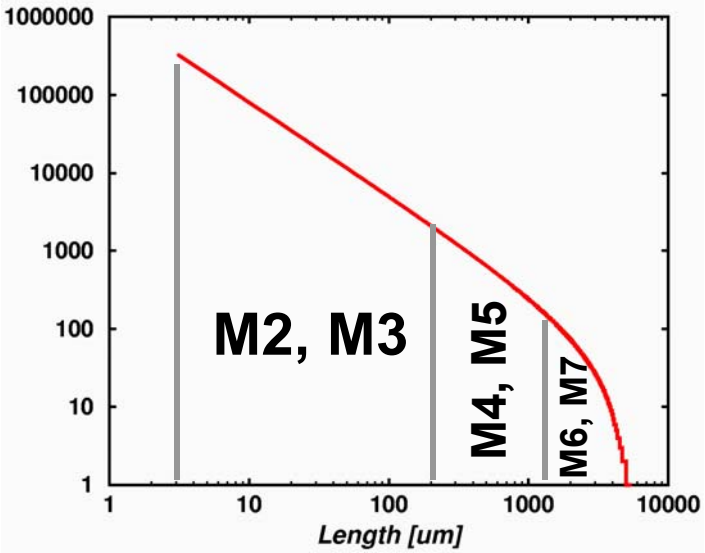


Wire length distribution

Prediction for 45nm Technology Node

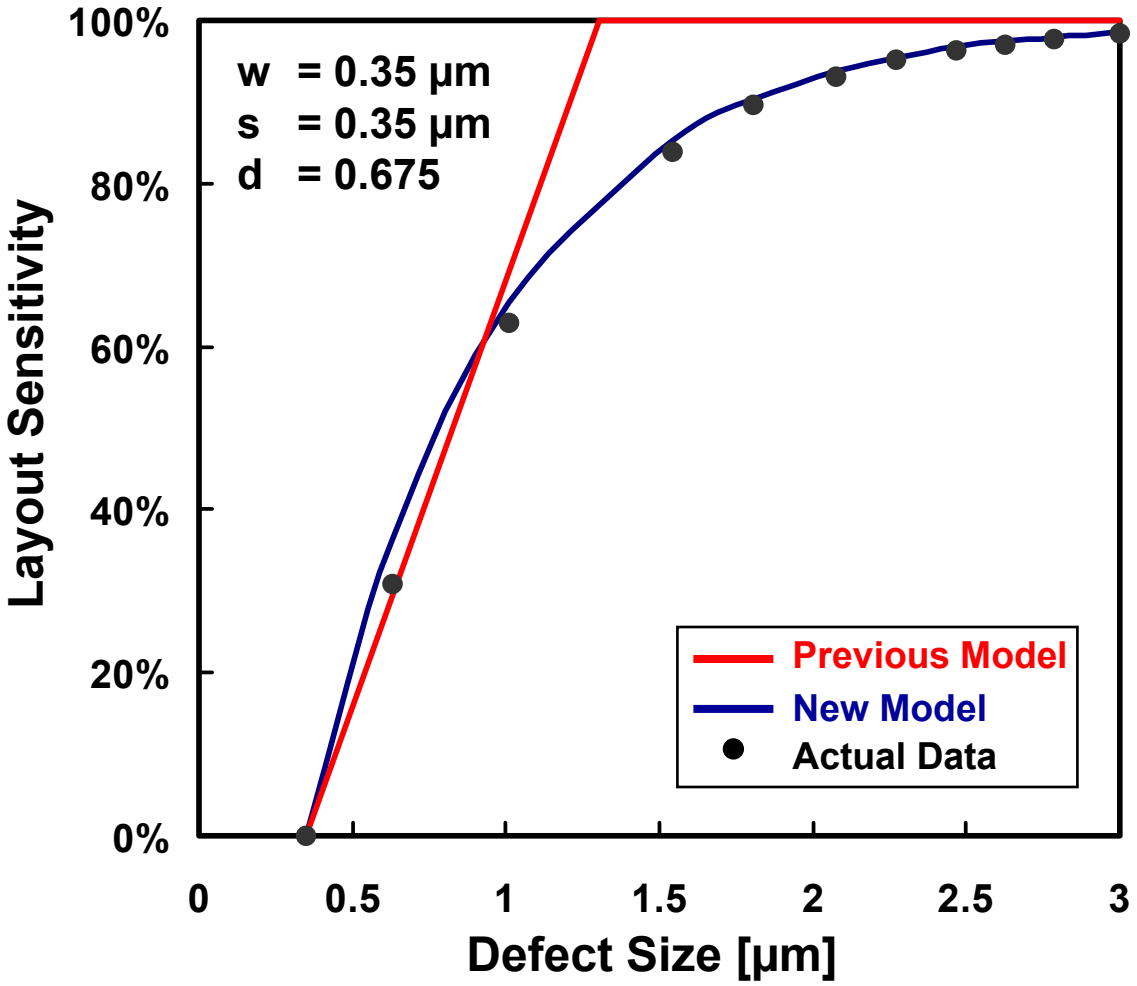
Number of logic gate = 75 Million
Raw Gate Density = 854 KGate/mm^2

# of nets = 55.6 Million
Gate Pitch = 1.14 um
Chip size = 9.8 mm
Average Length = 19.7 um
Median Length = 2.2 um
Total wire length = 1.37 Km



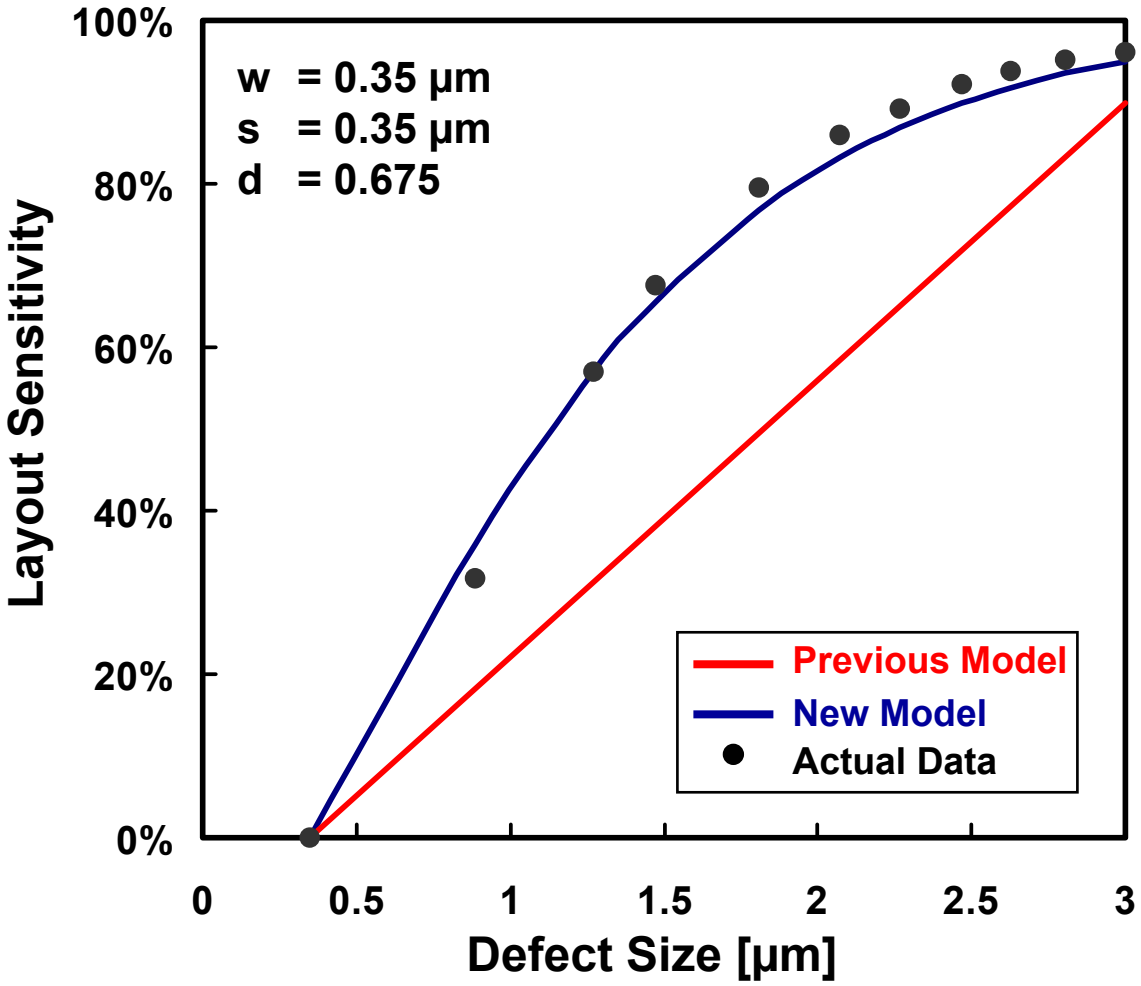
Metal Layers	L_{min} [μm]	L_{max} [μm]	Ch. Density	% Net
M2, M3	1.14	102	64 %	96 %
M4, M5	102	557	52 %	3 %
M6, M7	557	5100	26 %	1 %

Example: New Layout Sensitivity for Opens



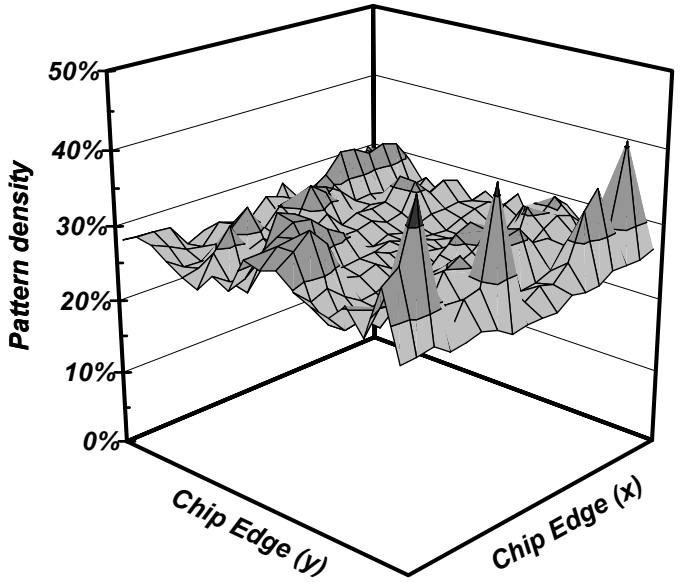
Data from: P. Christie and J. de Gyvez, "Pre-Layout Prediction of Interconnect Manufacturing," System Level Interconnect Prediction Workshop, pp. 167-173, March 2001

Example: New Layout Sensitivity for Shorts

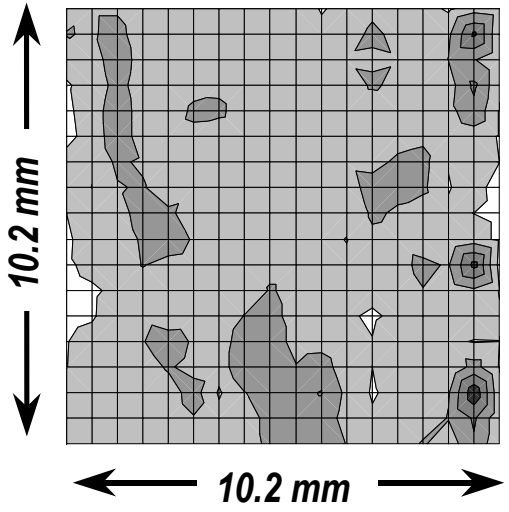


Data from: P. Christie and J. de Gyvez, "Pre-Layout Prediction of Interconnect Manufacturing," System Level Interconnect Prediction Workshop, pp. 167-173, March 2001

Application 2: Layout sensitivity Patterns

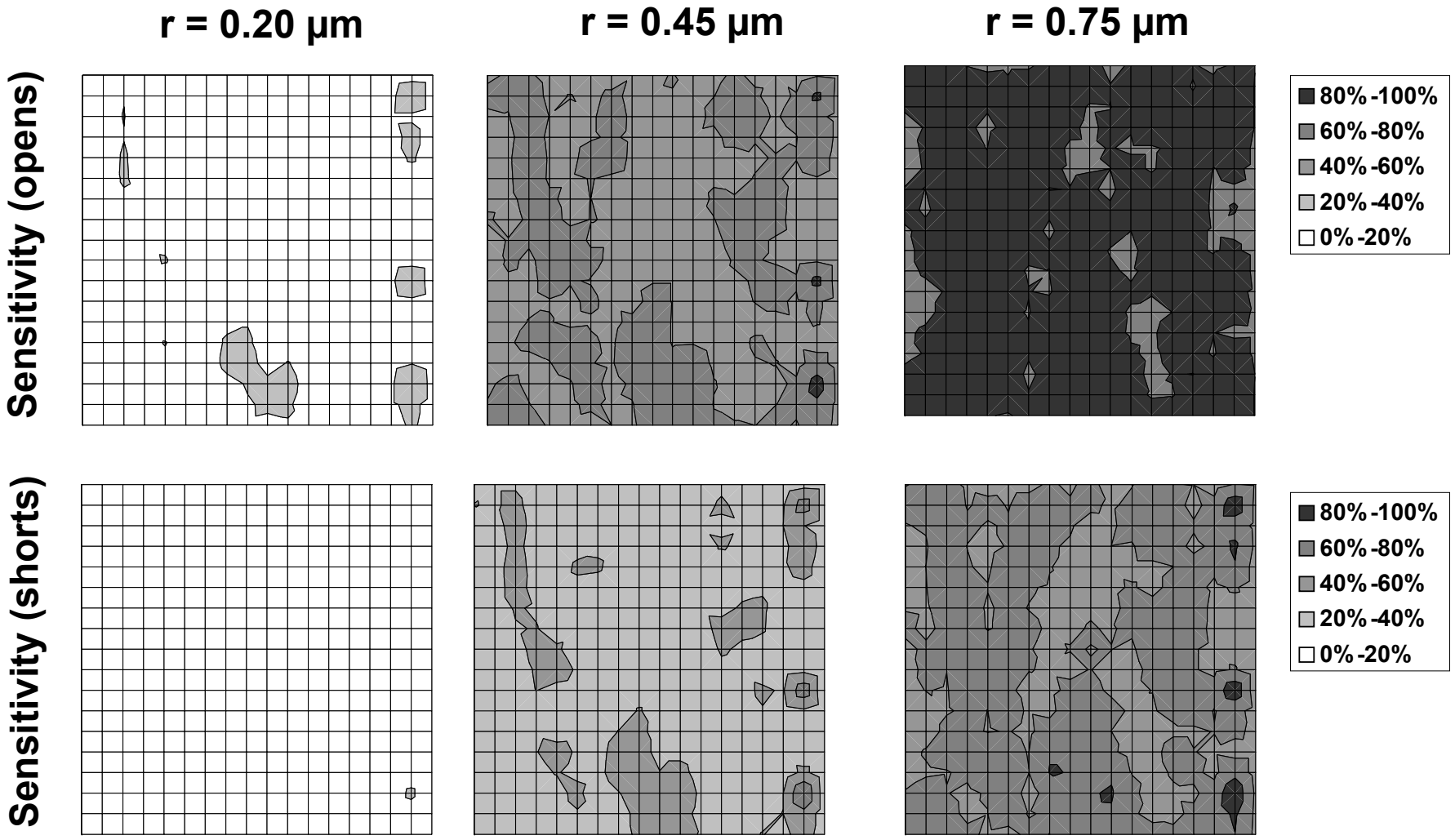


A 3-D Pattern Density Distribution



A 2-D Pattern Density Distribution

Layout Sensitivity Patterns



Conclusions

- **Layout sensitivity and critical area analysis has been around since 1982.**
- **Yield analysis and layout sensitivity is becoming more concern for modern VLSI designs. Critical area analysis is now part of design signoff process.**
- **Stochastic layout sensitivity model can expedite the yield analysis process significantly.**
- **Statistical modeling of layout sensitivity is just the beginning of many other applications for prediction of VLSI yield and manufacturability.**