



Synthetic Traffic Generation: a Tool for Dynamic Interconnect Evaluation

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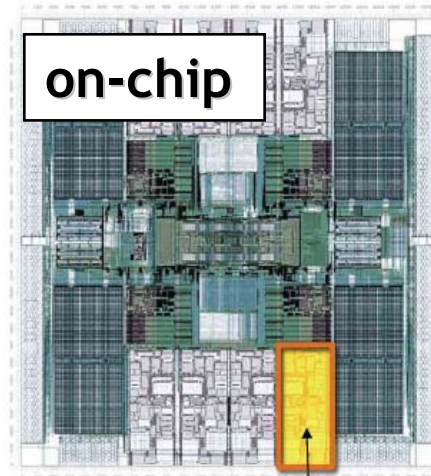
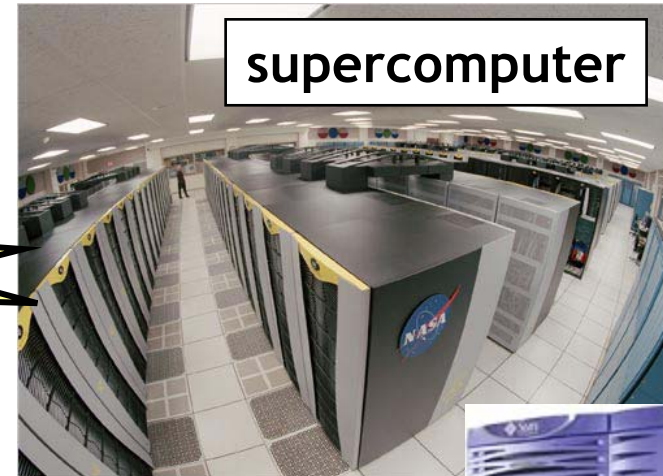
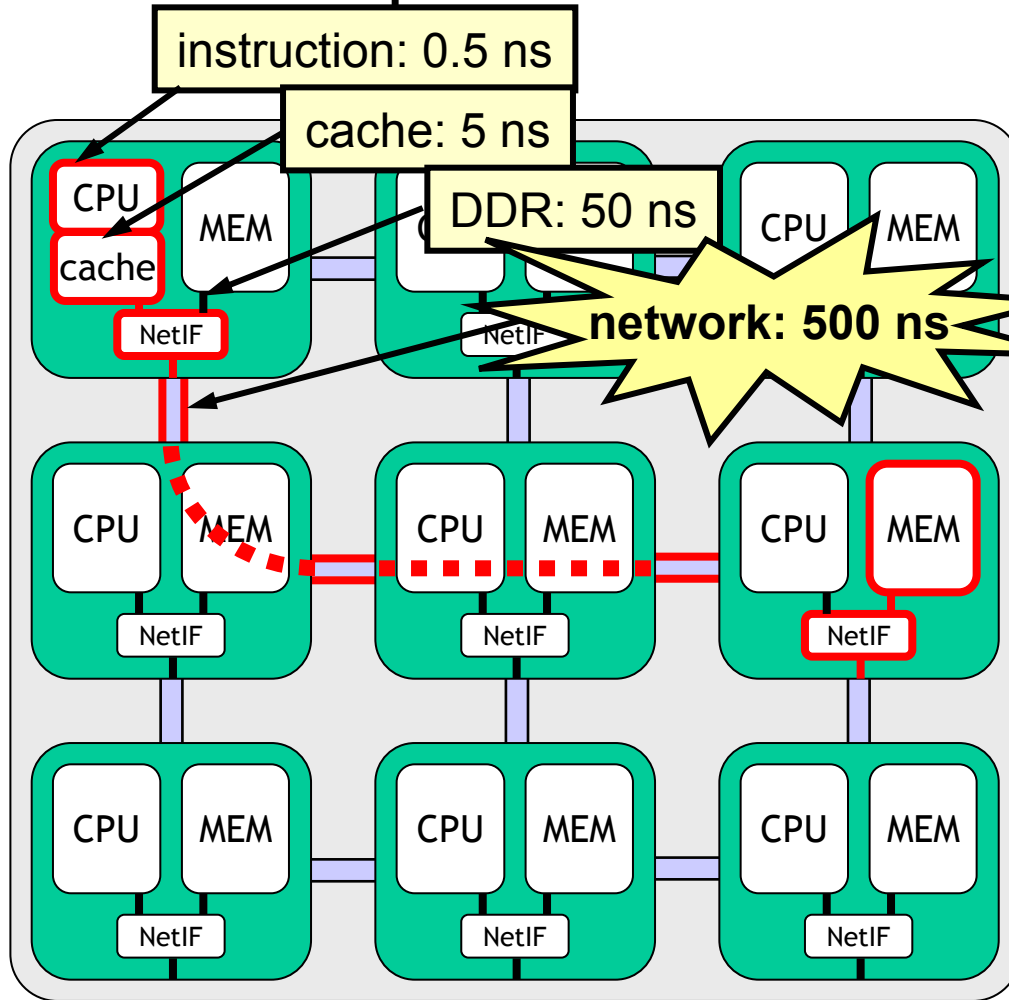


Outline

- **Introduction**
- Synthetic traffic generation
- Results
- Conclusions

Distributed shared-memory architecture

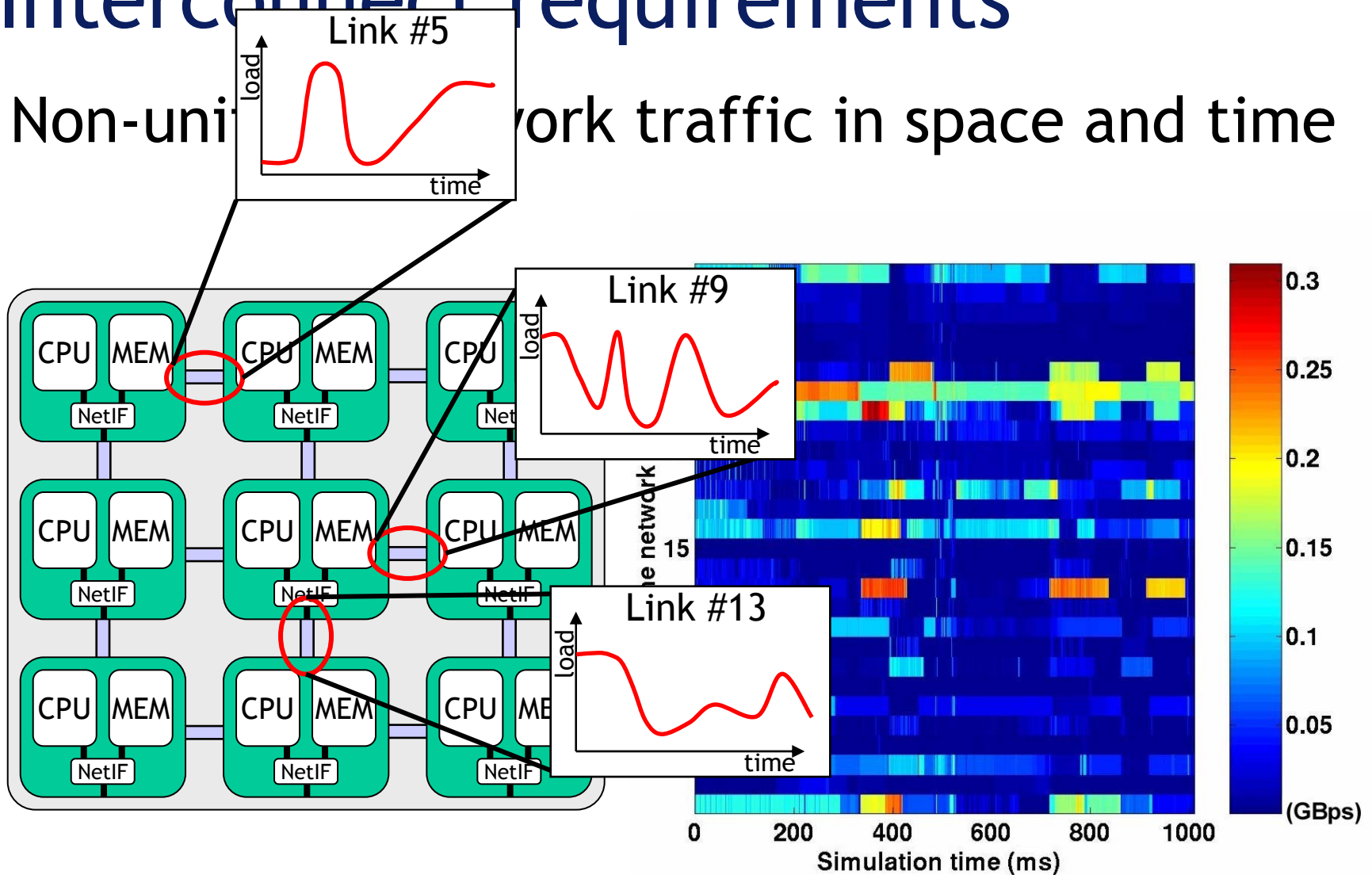
Network is part of the memory hierarchy



UltraSPARC-Core

Interconnect requirements

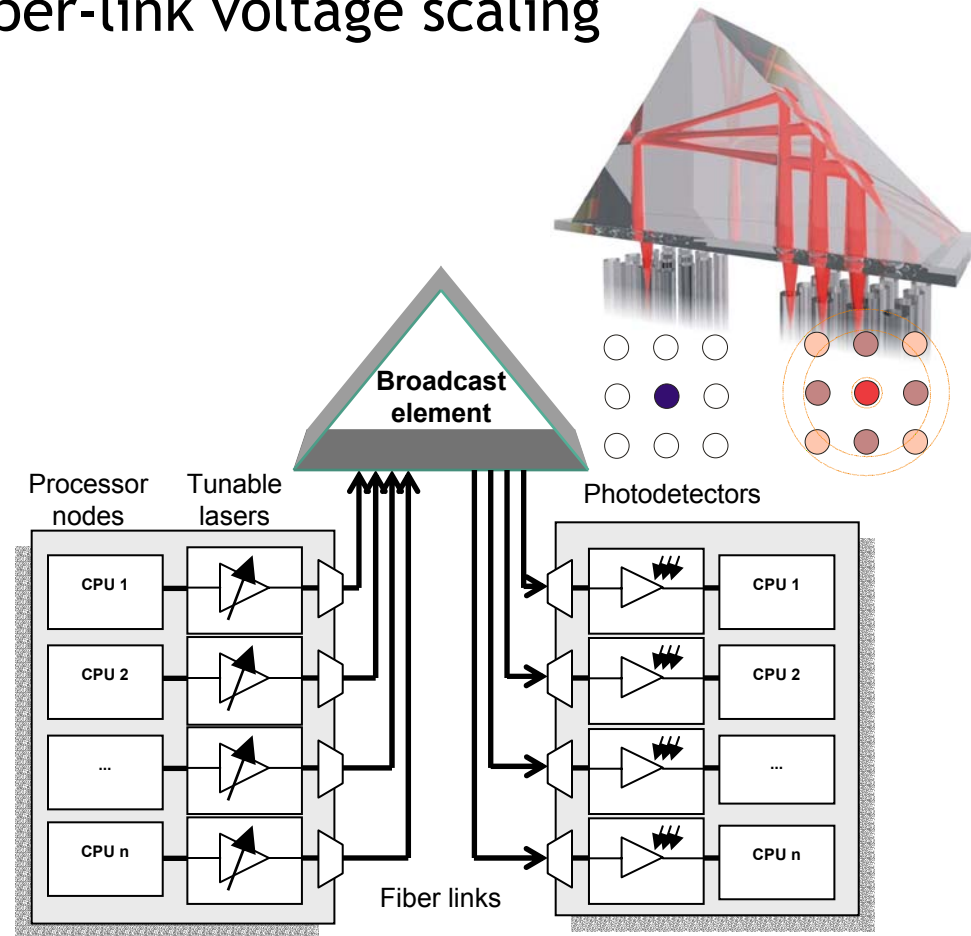
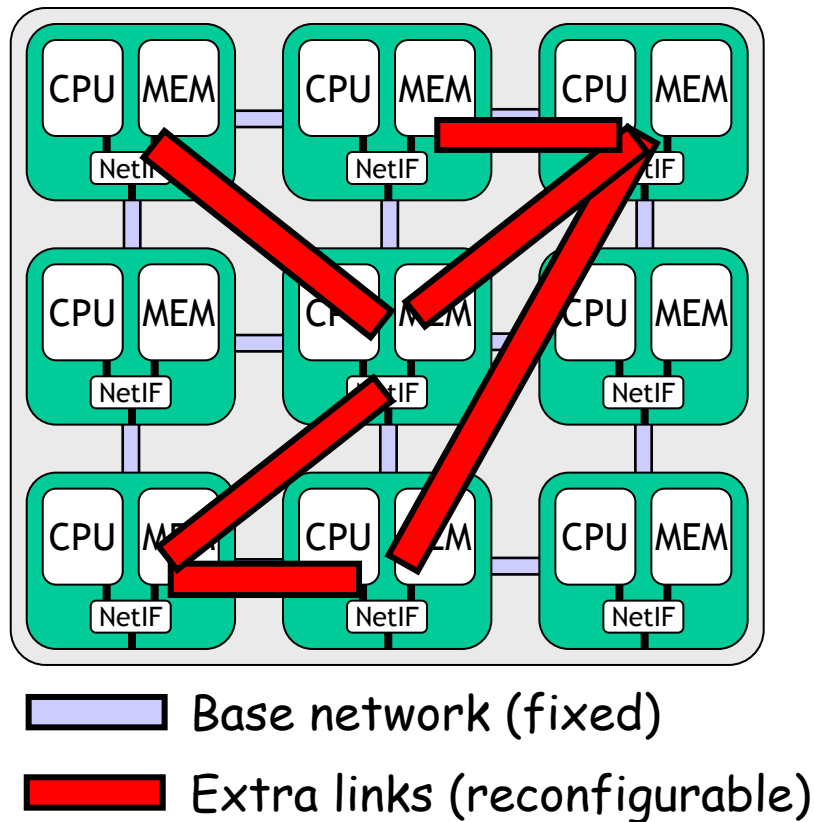
Non-uniform network traffic in space and time



=> Reconfigurable network?

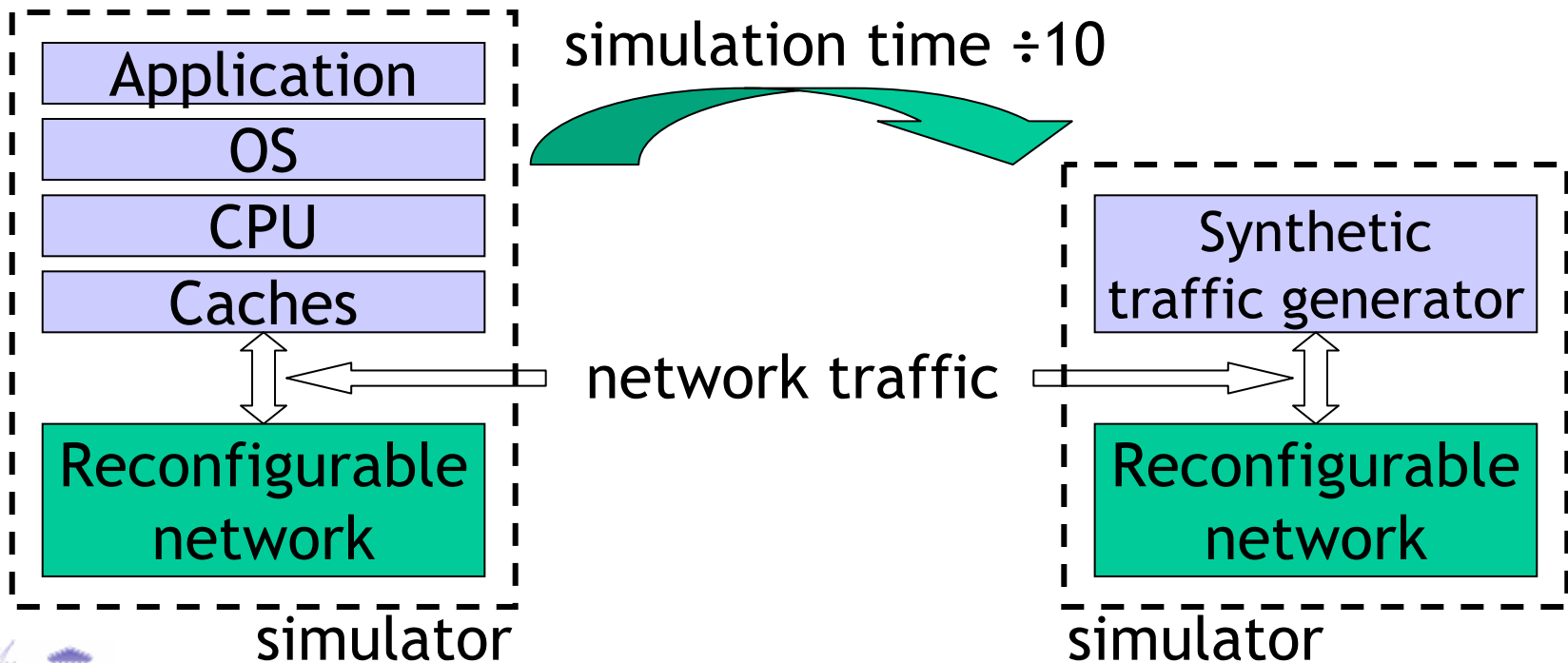
Reconfiguration implementation: base network + extra reconfigurable links

other 'dynamic networks': e.g. per-link voltage scaling



Evaluate networks with synthetic traffic

- Mimics the behavior of real traffic
- But without the computational cost of modeling application, OS, CPUs, caches, ...



We need better synthetic traffic

Reconfiguration exploits low-frequency dynamics in the network traffic

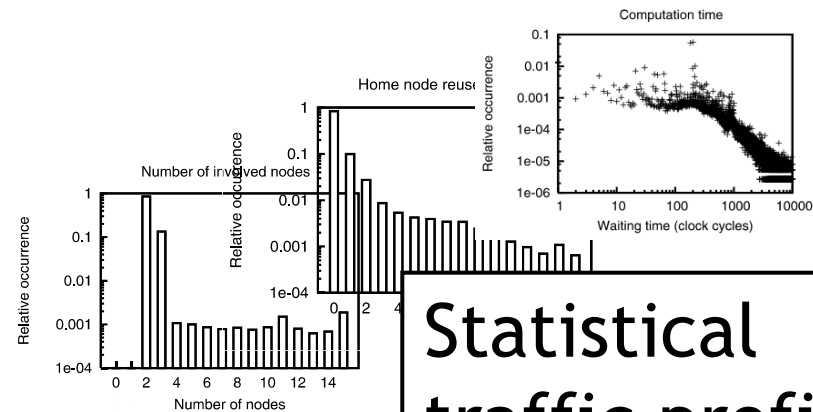
- Trace-driven simulation using **static** traffic patterns (uniform, hotspot, shuffle, ...) **won't do!**
- Full **execution-driven** simulation (traffic is driven by application: FFT, weather forecast, database) is **too slow!**

Outline

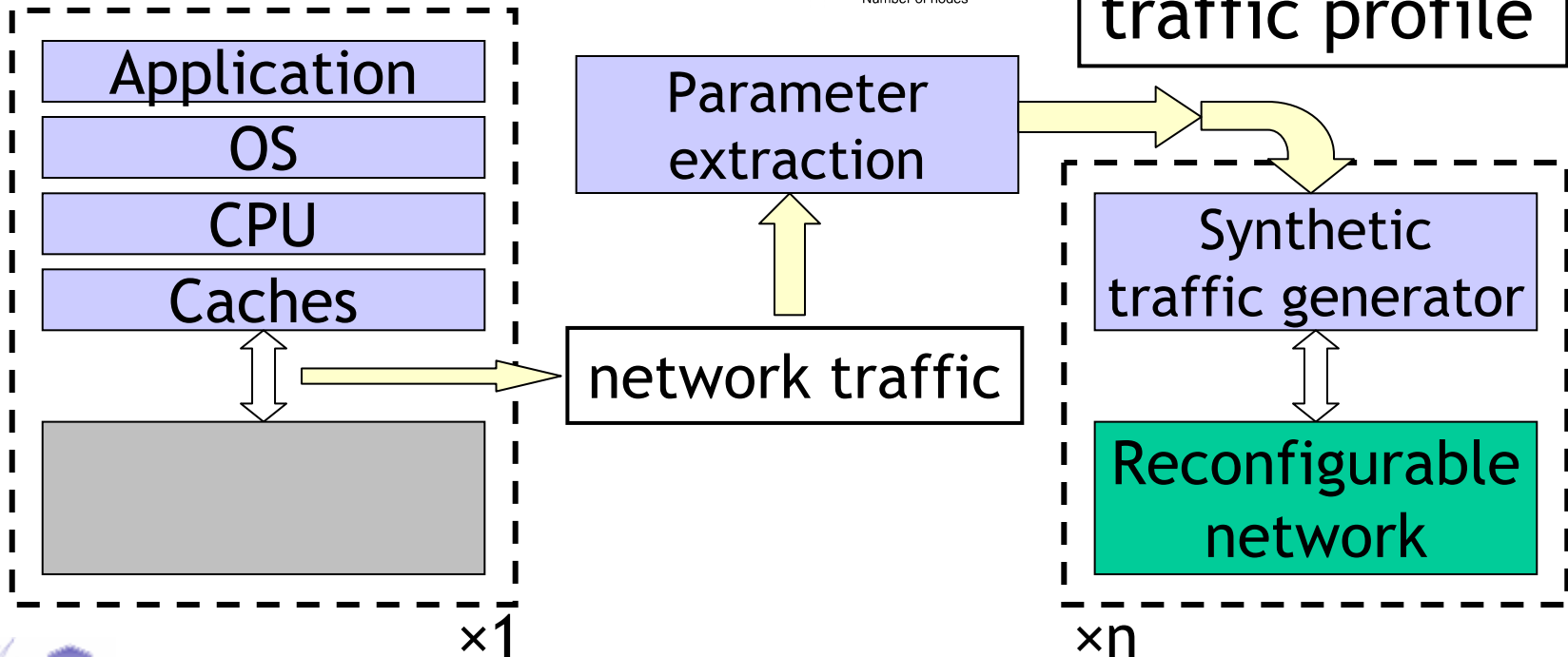
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Realistic synthetic traffic generation

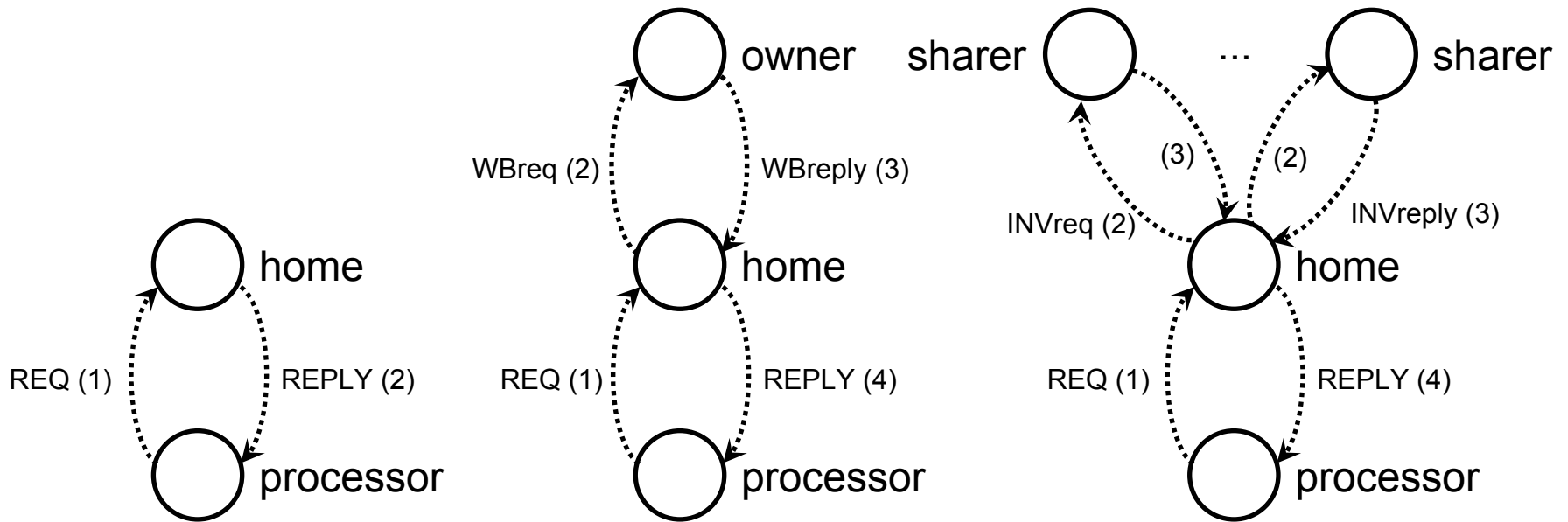
- One execution-driven simulation
- Resulting traffic profile re-used many times



Statistical traffic profile

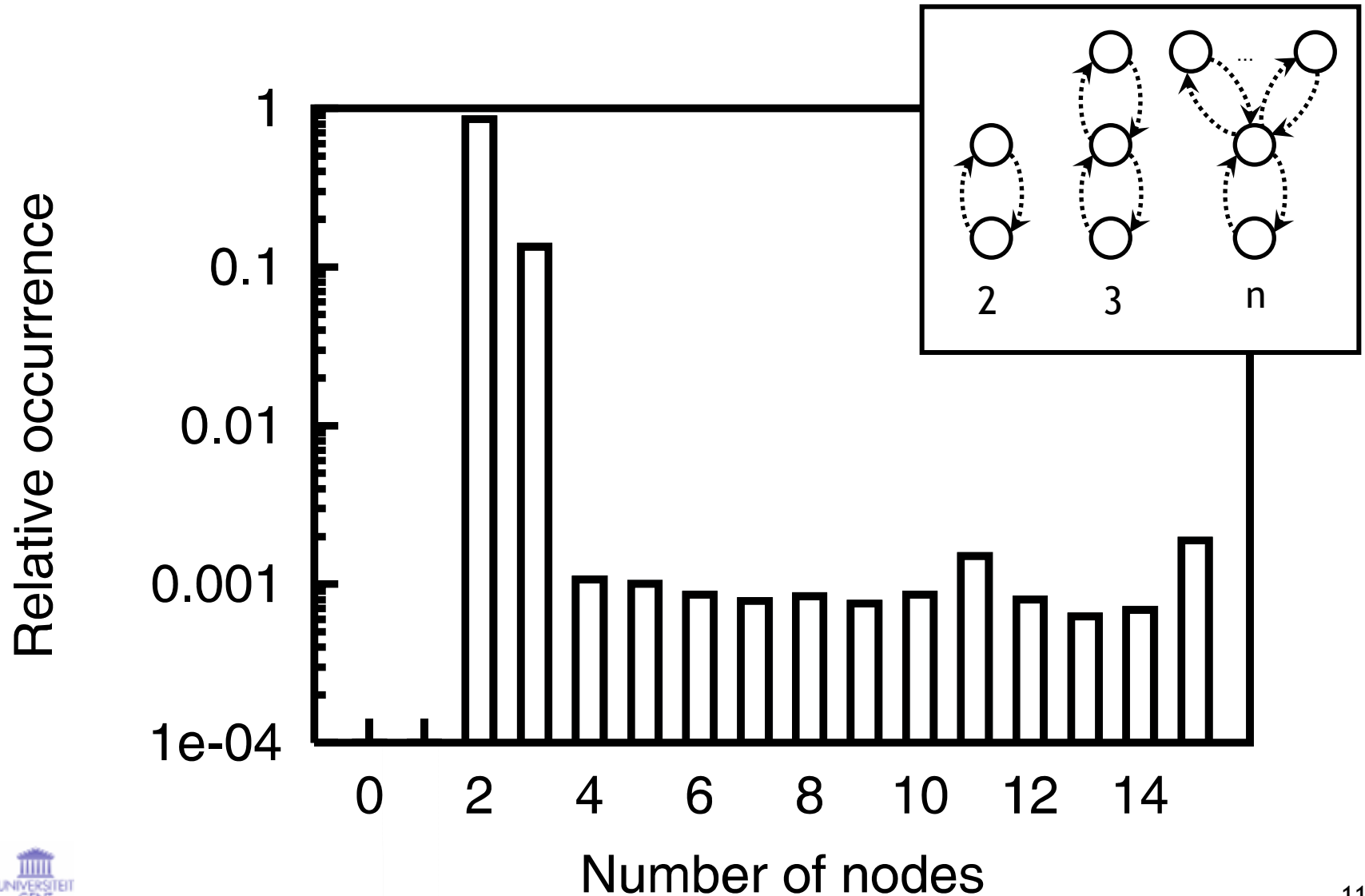


Preserve packet-interdependencies by using packet groups

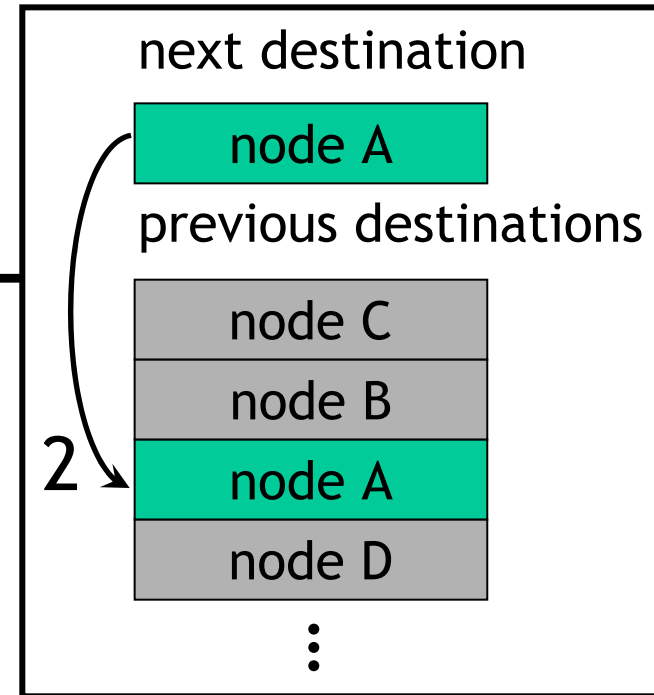
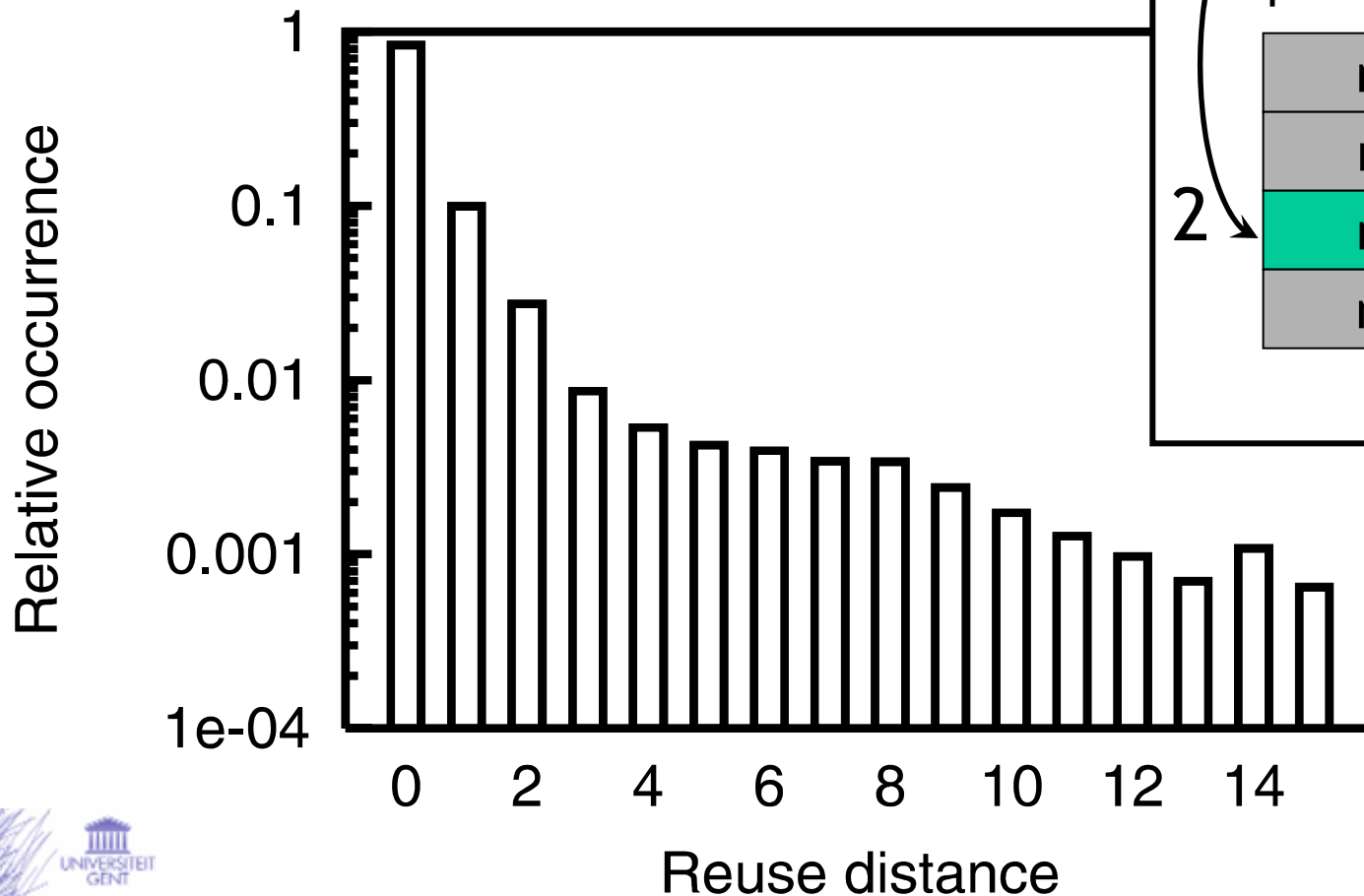


Packets are processed/generated in groups, corresponding to one memory operation each

Distribution of # involved nodes

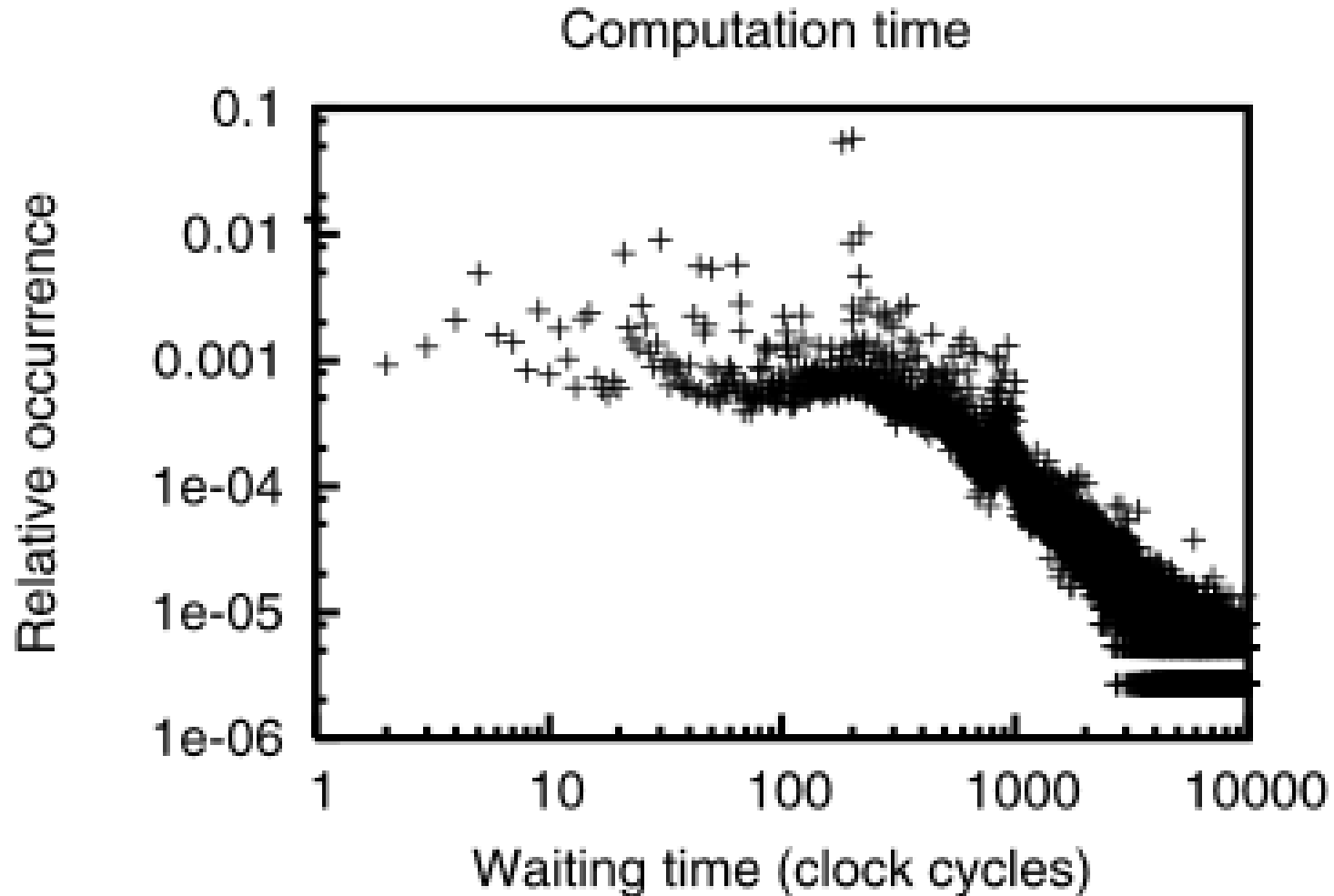


Reuse distance of home nodes: introduce locality



Computation or 'think' time

Models time delay between subsequent requests



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Simulations

- Simulation platform: Simics, providing *functional* multiprocessor simulation
 - 16 UltraSPARC III processors
 - SPLASH-2 parallel benchmarks
- Timing model:
 - Computes the latency for each memory access
 - Models caches, interconnection network
 - Base network: 4x4 torus
 - Extra links: configurable number, fan-out, reconfiguration interval

```
Compiling generic-cache.c: OK!
Compiling gc-common.c: OK!
Compiling modula_1d.c: OK!
Linking /home/christof/simics/simics-1.6.11/x86-linux/lib/libgeneric-cache-v9.so
[Christof@cluster:lib] make clean-generic-cache
Deleting generic-cache-v9...
[Christof@cluster:lib] make generic-cache
[Christof@cluster:lib] make generic-cache-32
Creating version.h
Creating dependencies: gc-common.c
Creating dependencies: generic-cache.c
Compiling generic-cache-v9-variant.c: OK!
Compiling generic-cache.c: OK!
Compiling gc-common.c: OK!
Compiling modula_1d.c: OK!
Linking /home/christof/simics/simics-1.6.11/x86-linux/lib/libgeneric-cache-v9.so
[Christof@cluster:lib] ]

[mpd1-0-image] Opened subfile 'sarek-1fp.conf'
[post-code-image] Opened subfile 'sarek-1fp.conf'
[post-data-0-image] Opened subfile 'sarek-1fp.conf'
[isprom-image] Opened subfile '.../input/sare
[memory-0-image] Opened subfile 'sarek-1fp.conf'
[memory-0-image] Opened subfile 'sarek-rradix-tra
raff'
[memory-0-image] Opened subfile 'sarek-rradix-tra
caff'
[su256-2-0-image] Opened subfile 'sarek2-solaris
[su256-2-0-image] Opened subfile 'sarek-1fp.conf'
[su256-2-0-image] Opened subfile 'sarek-rradix-t
at.caff'
simics: c
Magic breakpoint
[cpu7] <?0b000000000001e8>: <?0b0000000019e9
00>, ago)
simics: c
Magic breakpoint
[cpu7] <?0b000000000001e8>: <?0b0000000019e9
00>, ago)
simics: ]
```

Simulations

Once per benchmark:

Simulate execution of the benchmark, base network only, measuring traffic profile ⁽¹⁾

For each set of extra link parameters:

- Execution-driven simulation with reconfigurable network ⁽²⁾
→ *“correct” result*
- Trace-driven simulation using (simplified) traffic from (2)
→ *tracing error*
- Trace-driven simulation using (simplified) traffic from (1)
→ *traffic-dependence on network*
- Trace-driven simulation using synthetic traffic
→ *total error*

Several parameters can be measured

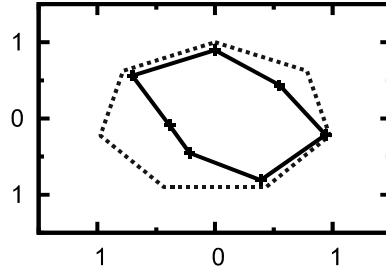
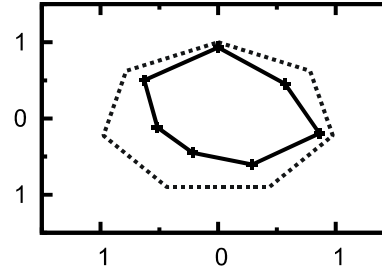
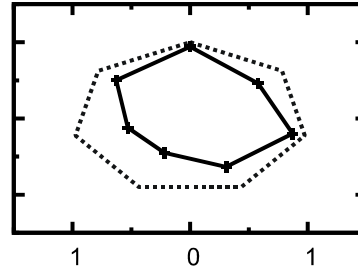
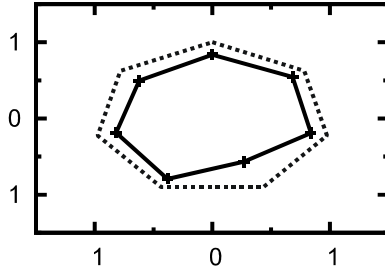
execution-driven

trace (this network)

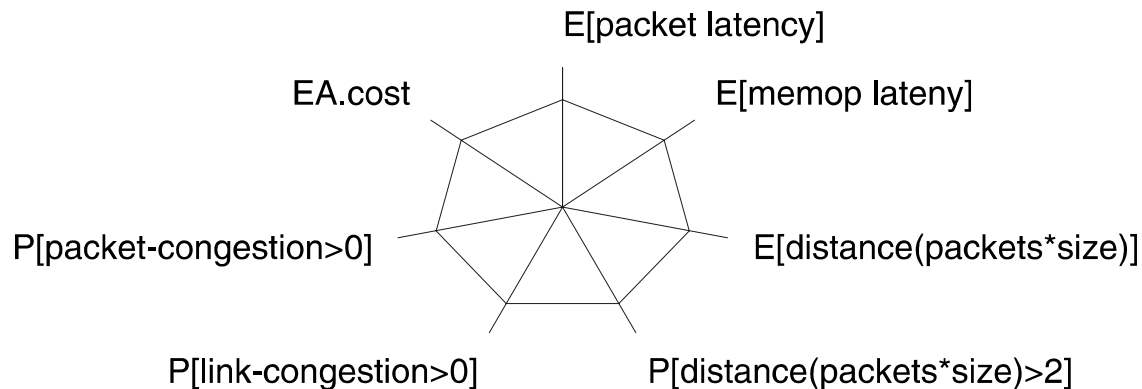
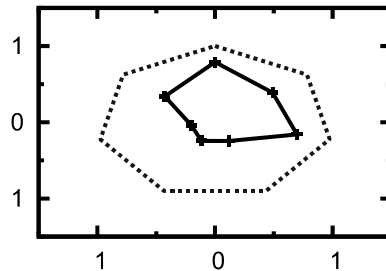
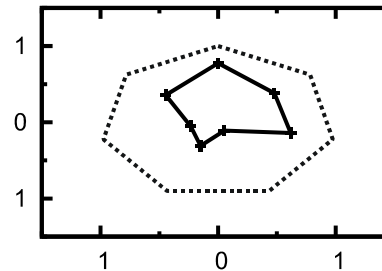
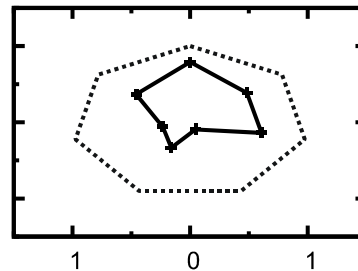
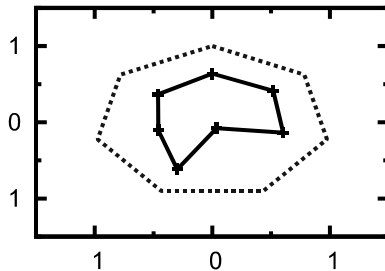
trace (base network)

synthetic

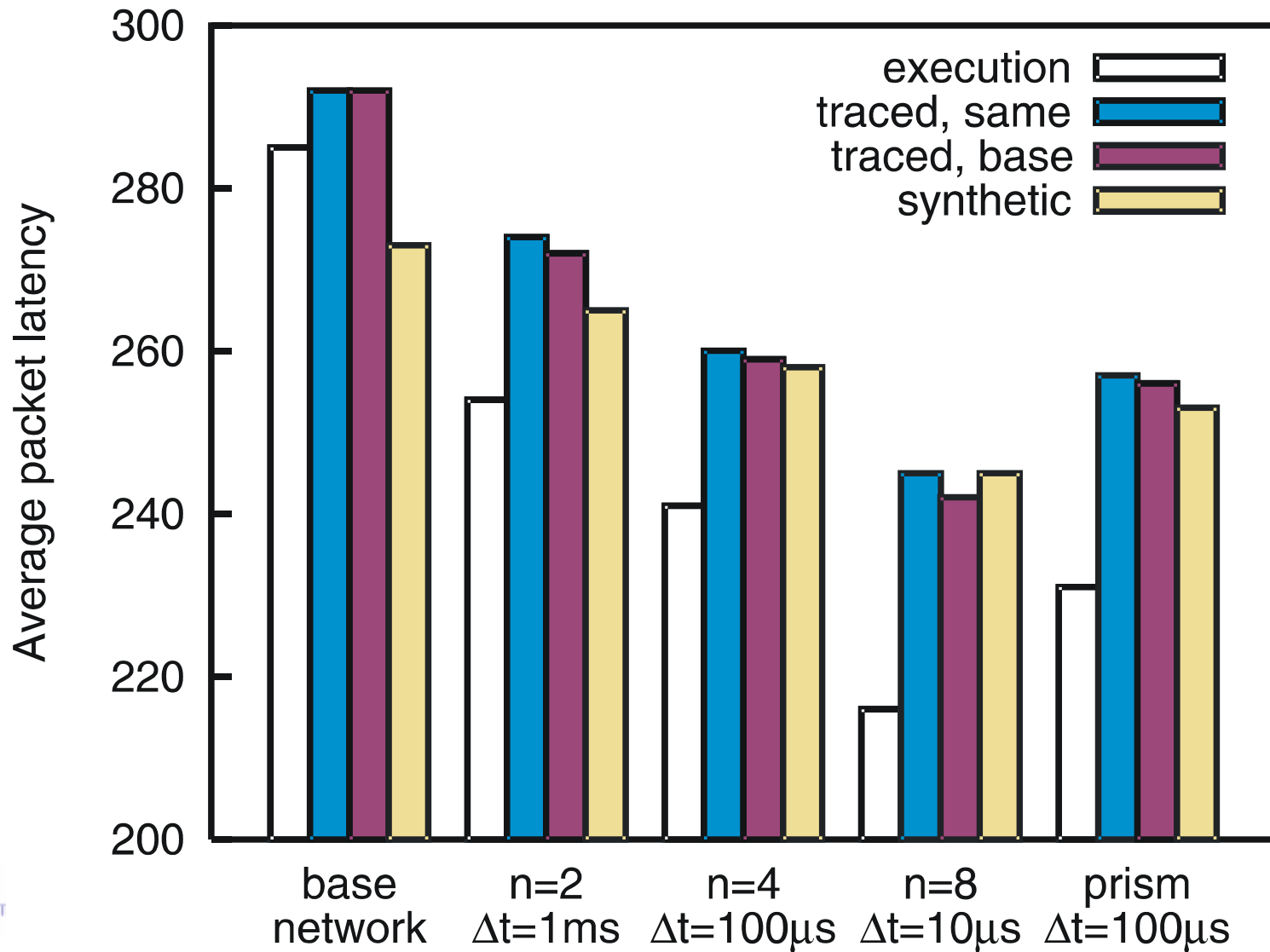
$n = 2$
 $f = 2$
 $\Delta t = 1 \text{ ms}$



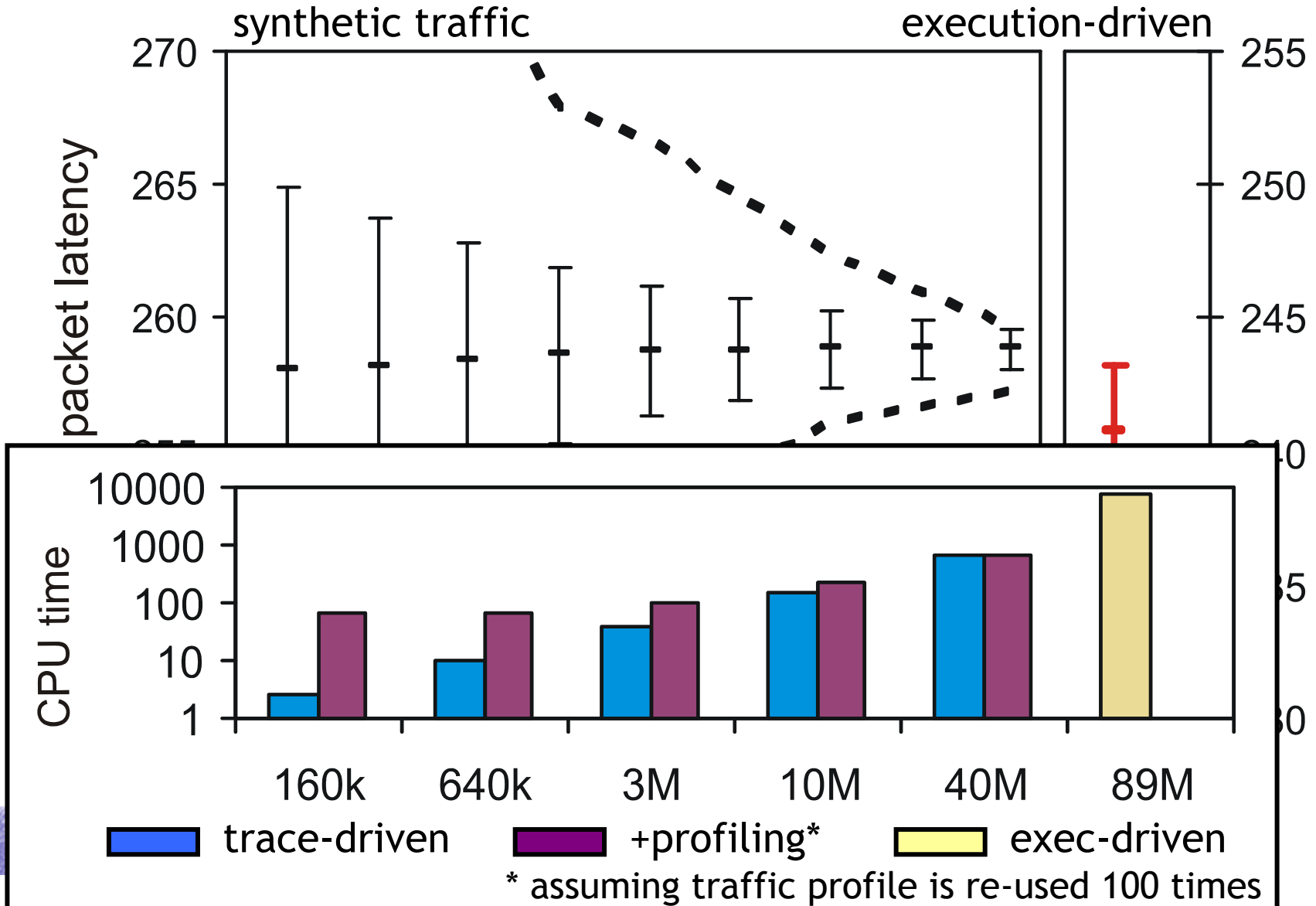
$n = 8$
 $f = 2$
 $\Delta t = 10 \text{ s}$



Detailed view of “average packet latency”



Variability for shorter traces



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Conclusions

- Synthetic traffic generation was extended to
 - shared-memory cache-coherence protocols,
 - reconfigurable networks
- Good relative accuracy for different network topologies
- Much less computationally expensive (x10), even more so for shorter traces (x100)
- Reproducibility equal to or better than execution-driven simulations