Impact of Interconnect Length Changes on Effective Materials Properties (Dielectric Constant)*

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Outline

- The general problem
- Motivation and importance to IBM
- Impact of interconnect length changes on effective materials properties (dielectric constant)
  - Performance Model
  - Comparison of model estimates with data extracted from POWER4 chip designs
- Conclusions
- Future work

The General Problem

The general problem

Methodologies to evaluate and quantify the performance impact of proposed design changes are needed prior to migrating chip designs to future technology nodes.

On-chip interconnect is required to satisfy a set of electrical and physical constraints in present and future technologies.

The General Problem

The general problem

Questions

How can we quantify the performance impact of changes to interconnect lengths in a design?

How do we evaluate a performance model?

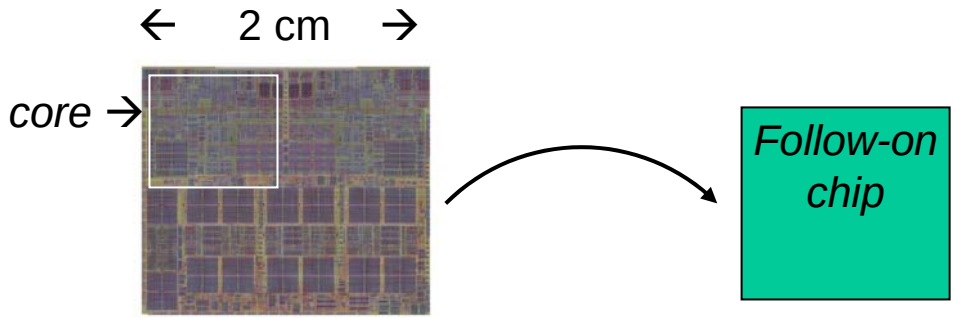
How do model estimates compare with estimates derived from interconnect measurements in POWER4 chip designs?

Example

The general problem

Questions

POWER4 microprocessor



Goals:

(1) Obtain estimates of the performance impact of changing interconnect length in four control logic designs in the core

(2) Re-express performance impact as an *effective reduction in dielectric constant* (low-k)

Method:

(1) Derive performance model

(2) Compare estimates with measurements

Motivation and Importance to IBM

Issues:

Wire length

Via count

Performance

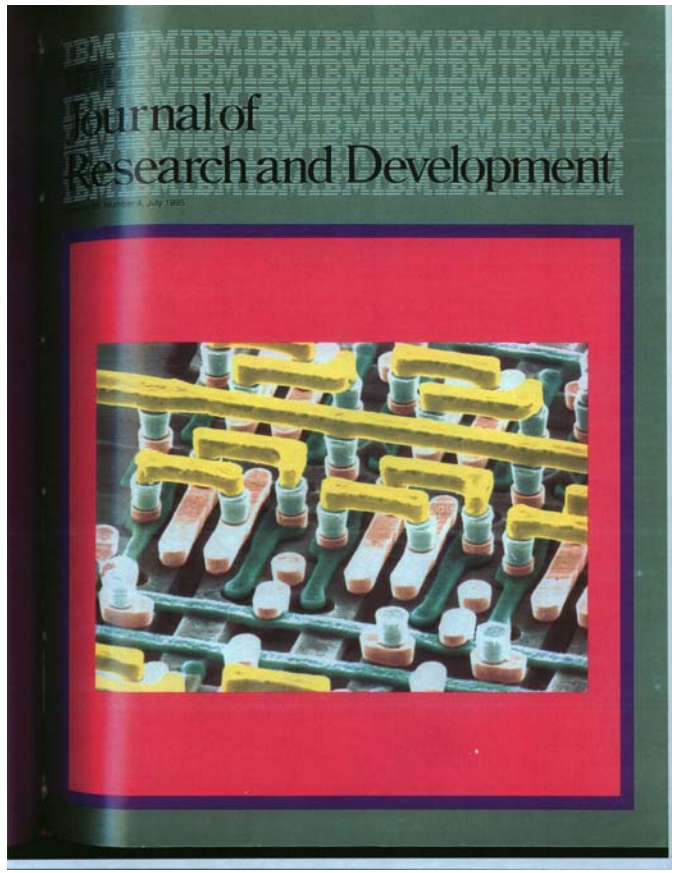
Metal layers

Wire cross-sections

Wire design

Yield

Design cost



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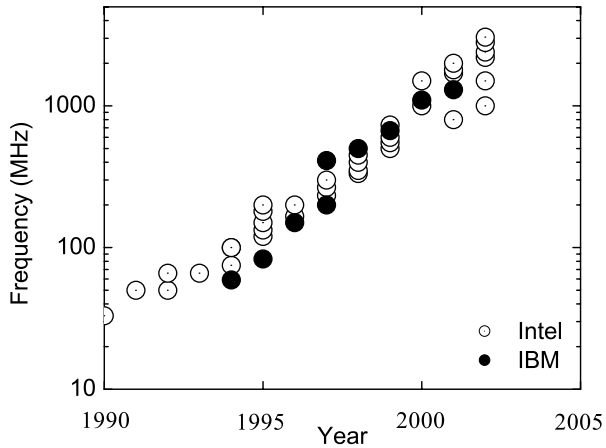

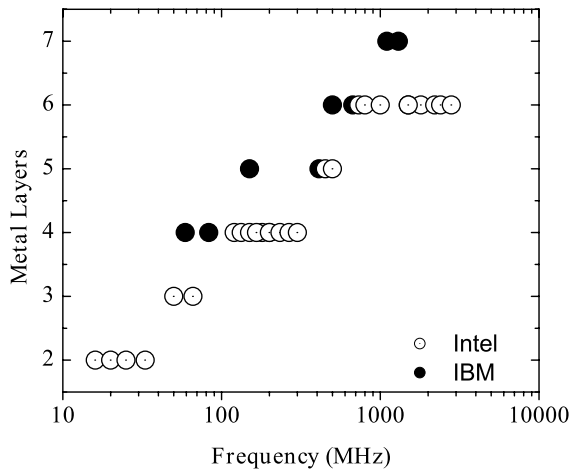

Ref: Microprocessor Report (various), H. Schleich, W. Schultheiss

Motivation and Importance to IBM

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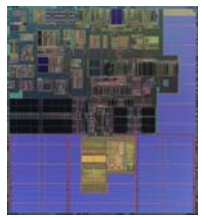
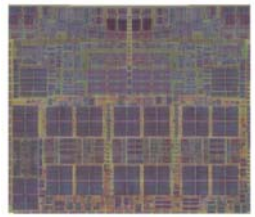
	Intel	**IBM**
chip	Itanium2 	POWER4 
date	7/2002	12/2001
frequency	1.0 GHz	1.3 GHz
area	400 mm^2	415 mm^2
transistors	221Million	174 Million
power	130 Watts	155 Watts
device process	0.18-micron bulk	0.18-micron SOI
metal layers	6 Al	7 Cu

Ref: Microprocessor Report (various), Joseph Czajkowski

How Can We Estimate Impact of Interconnect Length Changes on Timing-Critical Paths?

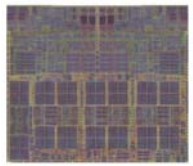
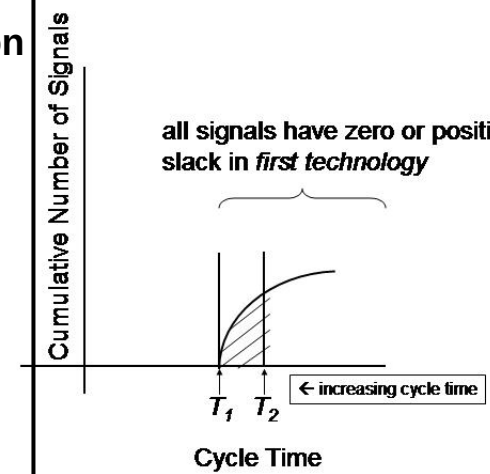
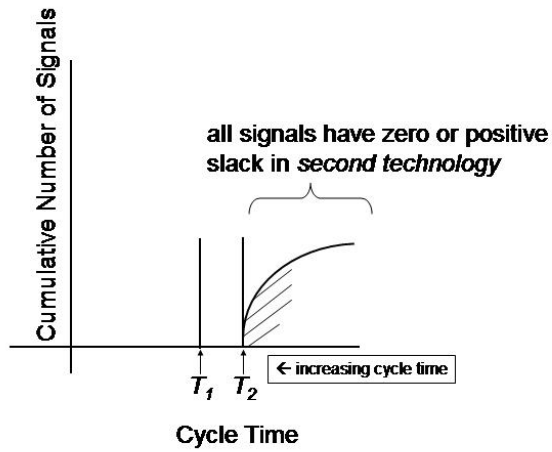
Better interconnect estimates will be more important as chips continue to increase in complexity and device count

Currently, information about interconnect requirements and measurements are needed for successful design of today's complex ULSI chip circuitry

Our work provides a method to quantify the impact of interconnect length changes on performance

Design Migration

Performance Model Parameters

	IBM	Follow-on chip
chip	POWER4 	
technology node	1	2
cycle time	T_1	T_2
device delay	τ_{d1}	τ_{d2}
wire length, delay	L_1, τ_{w1}	L_2, τ_{w2}
path delay	τ_1	τ_2
slack distribution		

Design Migration

Performance Model Parameters

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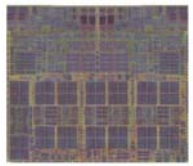
chip	POWER4 	
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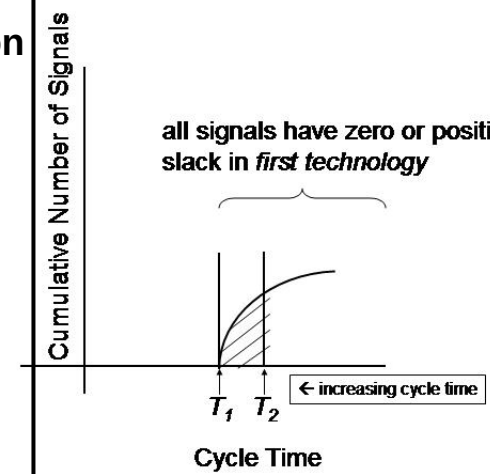
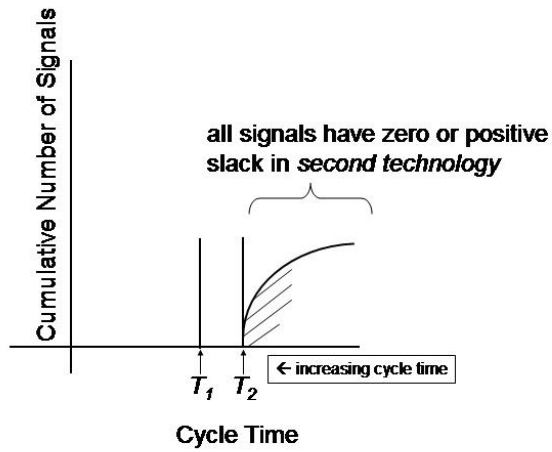
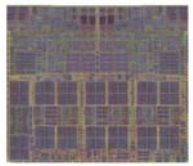
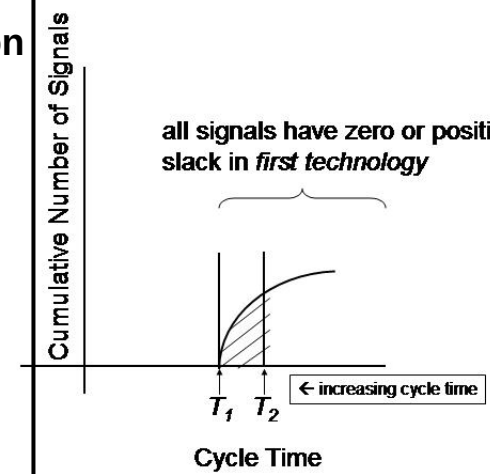
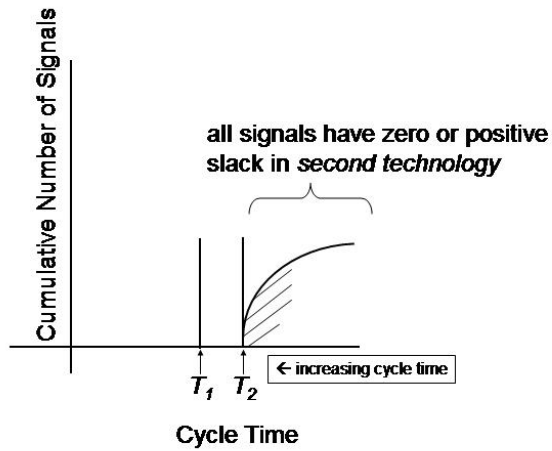
slack distribution		

d = cycle time ratio

s = device scaling factor

Design Migration

Performance Model Parameters

	IBM	Follow-on
chip	POWER4 	
technology node	1	2
cycle time	T_1	$d = T_1 / T_2$ T_2
device delay	τ_{d1}	$s = \tau_{d1} / \tau_{d2}$ τ_{d2}
wire length, delay	L_1, τ_{w1}	L_2, τ_{w2}
path delay	τ_1	τ_2
slack distribution		

Performance Model

Design Migration

Write the path delay as a sum of delay contributions from wires and devices*

Write expressions for path delays τ_1 *and* τ_2

Assume $\tau_1 = T_1$ *(zero slack)*

Consider the simple case of a critical path composed of one wire and one device:

$$\tau_2 = \tau_{w2} + \frac{1}{s} T_1 - \frac{1}{s} \tau_{w1} > T_2$$

Use lumped wire delay model of Rabaey Digital Integrated Circuits: A Design Perspective. Englewood Cliffs, NJ: Prentice-Hall (1996).

Performance Model

Design Migration

Write expression for path delay τ_1' in technology 1 such that the delay in the migrated design equals T_2 (zero slack):

$$\tau_1' = T_1 + \left(T_1 + d\tau_2\right) < T_1$$

To achieve this, the wire delay τ_{w1}' in technology 1 is:

$$\tau_{w1}' = \frac{\tau_1'}{T_1}\tau_{w1} = a_{w1}\left(L_1'\right)^2 + b_{w1}L_1'$$

Solve for L_1'

Performance Model

Design Migration

Model Equations

Express the relative netlength reduction: f_1

$$f_1 = \frac{L_1' - L_1}{L_1}$$

Express performance improvement as a normalized dielectric constant: ε_1'

$$\varepsilon_1' = \frac{\tau_{w1}'}{\tau_{w1}}$$

Express relative performance improvement: f_ε

$$f_\varepsilon = \frac{\varepsilon_1' - \varepsilon_1}{\varepsilon_1}$$

Express fractional performance improvement: f

$$f = \frac{f_\varepsilon}{f_1}$$

Performance Model

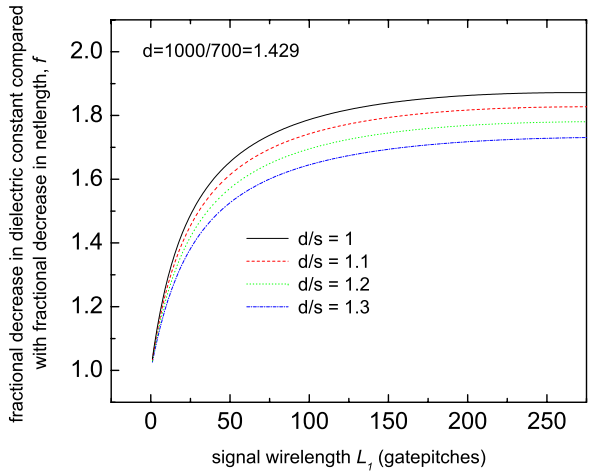
Design Migration

Model Equations

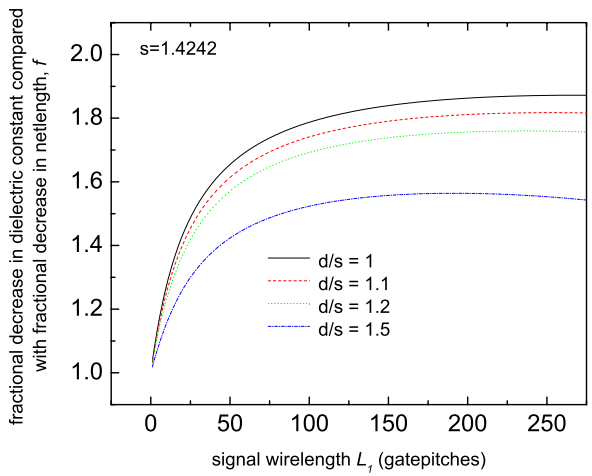
Performance Improvement

Fractional performance improvement: $f = \frac{f_\varepsilon}{f_1}$

f



f



Design Data

Performance model assumptions and inputs

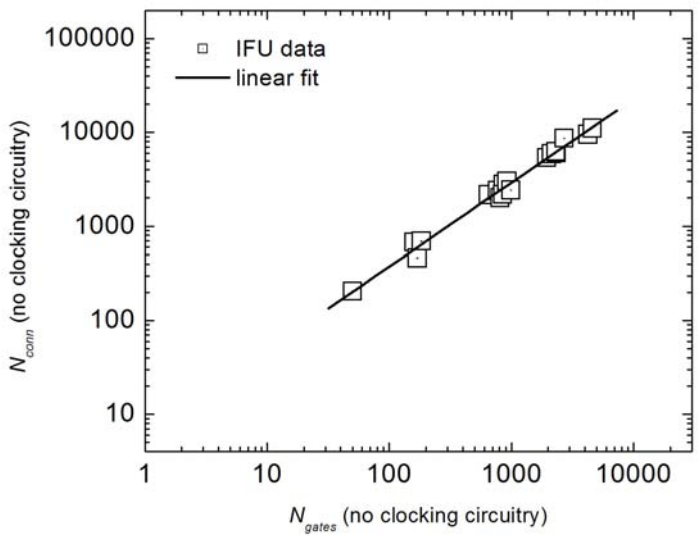
- *Each path contains one wire and one device*
- *Four metal layers are used in signal wiring*
- *Each path has zero slack*
- *T_1/T_2 = 1000ps/700ps ~ 1.439*
- *s ~ 1.424*

Interconnect model inputs

*Extract functional Rent parameters from POWER4 IFU for use with Davis model***

k^f_R = 6.15

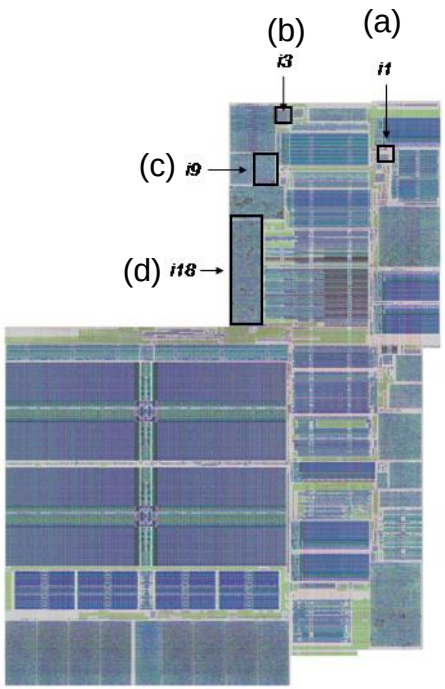
p^f_R = 0.89



**See interpretation of Rent's memos for ULSI circuitry: M. Y. Lanzerotti, G. Fiorenza, R. A. Rand, IEEE Trans. VLSI, vol. 12, Dec. 2004, pp. 1330-1347.

Cycle Time of Critical Paths

Cycletime requirement in technology 1 to satisfy zero slack in technology 2

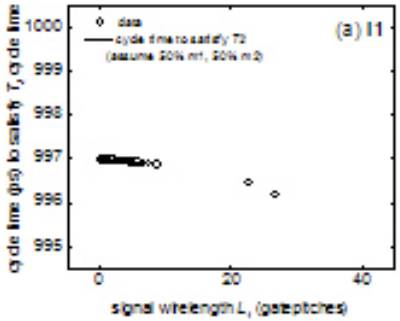


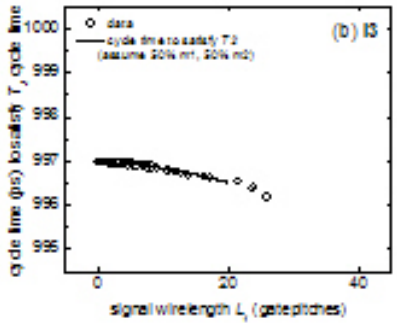
(a)

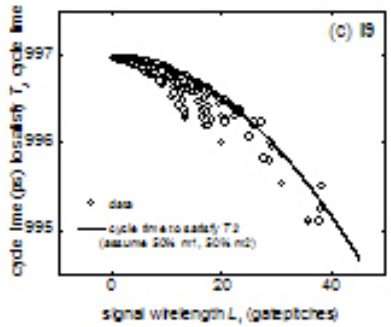
(b)

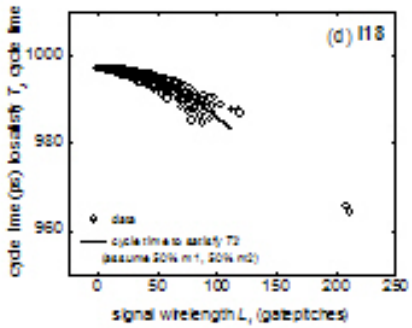
(c)

(d)



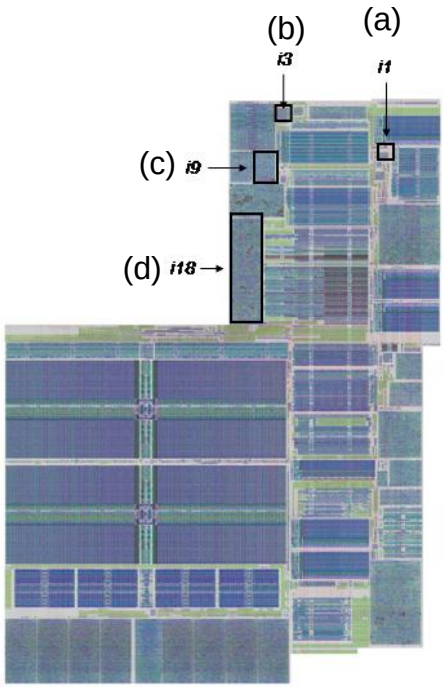






Performance Improvement

Netlength reduction
(Left-Hand Side)
and effective
reduction in
dielectric constant
(Right-Hand Side)

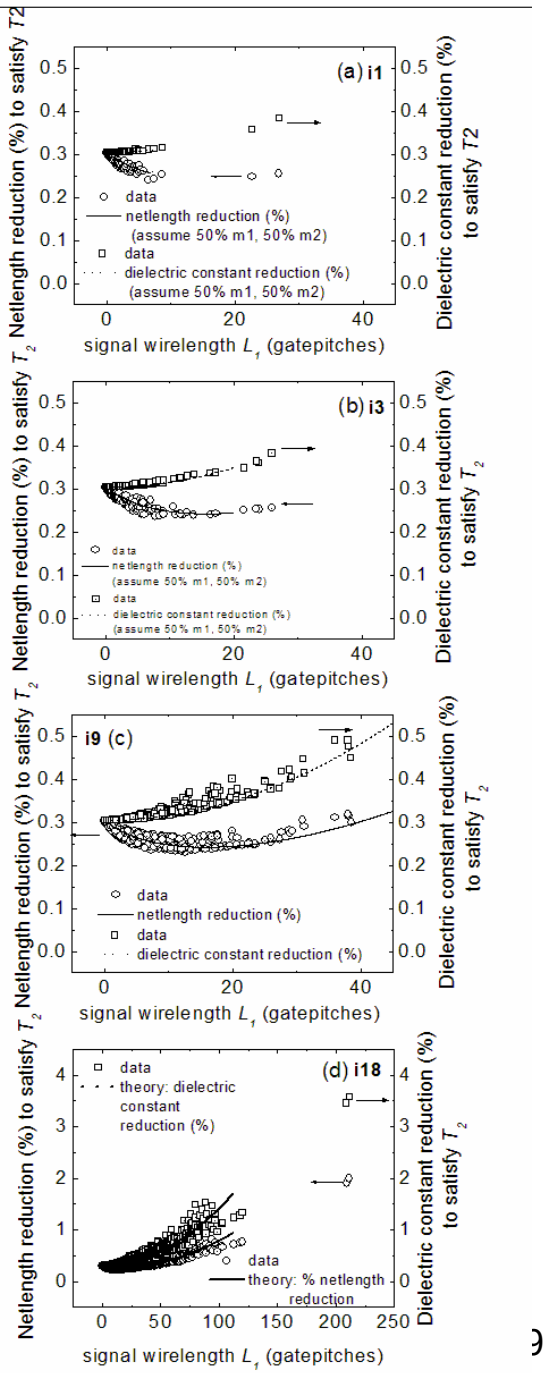


(a)

(b)

(c)

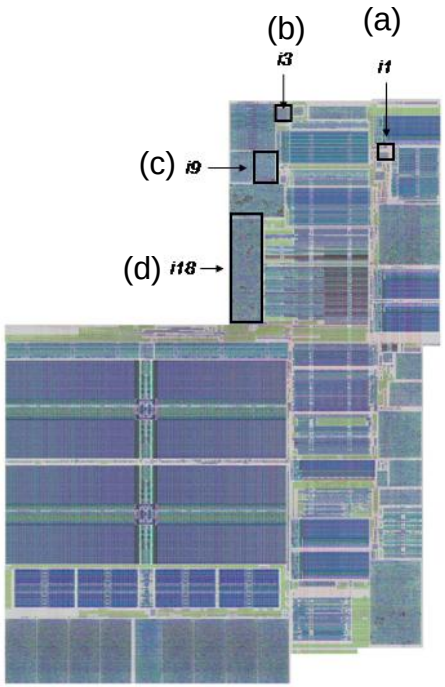
(d)



Relative Performance Improvement

Relative dielectric constant reduction

$f > 1$



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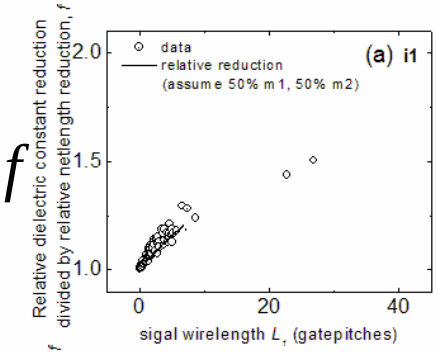
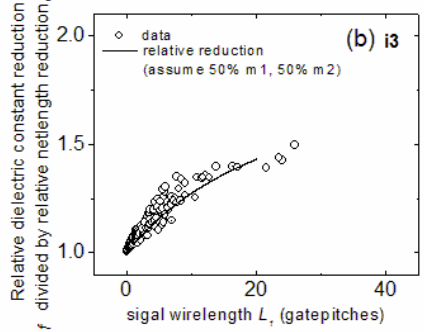
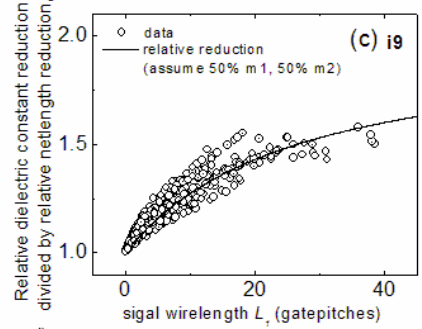
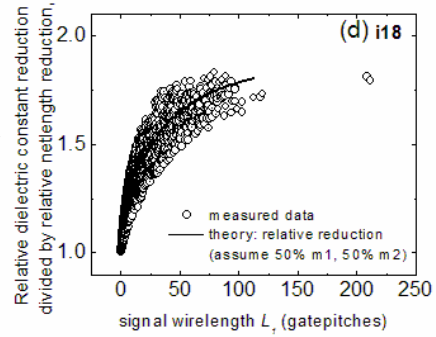
(c)

(d)









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connect Predi

Conclusions

Methods to evaluate and quantify performance impact due to reductions in interconnect length in chip designs have value in ULSI chip design:

- Estimates quantify the extent to which design changes can ***mimic*** effects of expensive ***low-k*** fabrication processes
- Estimates quantify the performance impact of migrating design to a future technology node
- Design changes can be implemented late in the design cycle
- Design changes selectively target timing-critical signals

Future Work

Consider impact of interconnect length changes on power dissipation, reliability, and yield

Extract design netlists from POWER6 designs

-Extract design characteristics

Consider differences between models and real design characteristics:

-Designs are typically not square

-Design area occupancy is less than unity

-Some signals have greater-than-unity fan-out

-Range of applicability of Rent's rule covers half the range of gate partition sizes