Energy Efficient High Speed On-Chip Signaling in Deep Submicron CMOS Technology

I.Ben Dhaou and H.Tenhunen.

Royal Institute of Technology,

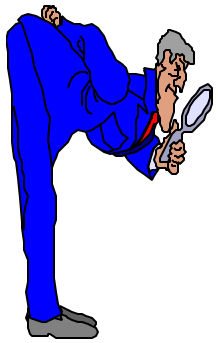
Dept. Of Elect., ESDLab,

SE-164 40 Kista, Sweden

Outlines

- Design challenges in Deep-submicron CMOS
- Our Approach to tackle DSM effects
- Problem formulation and Related work
- Current mode MVL
  - Qualitative analysis of the On-Chip Interconnect (OCI)
  - Energy-efficient signaling
- Simulation results
- Concluding remarks

DSM: opportunities and challenges



L (μm)	Tox (Å)	Vdd (in V)	Vt (in V)	Line thickness (μm)	Width and spacing (μm)	Sheet resistance (Ω/)	Tins (in μm)	Dielectric constant
0.25	**50**	**2.5**	**0.625**	**0.5**	**0.3**	**0.044**	**0.65**	**3.3**
0.18	**40**	**1.8**	**0.450**	**0.46**	**0.23**	**0.048**	**0.5**	**2.7**
0.13	**30**	**1.5**	**0.375**	**0.34**	**0.17**	**0.065**	**0.36**	**2.3**
0.10	**25**	**1.2**	**0.3**	**0.26**	**0.13**	**0.085**	**0.32**	**2**
0.07	**20**	**0.9**	**0.225**	**0.2**	**0.1**	**0.11**	**0.27**	**1.8**

D. Sylvester et al., "*Rethinking Deep-Sumbicron Circuit Design*", Proc. Comp. Nov.99

Contd., Main Disadvantages

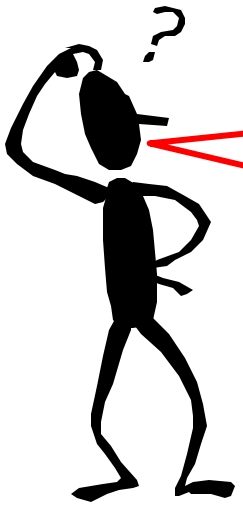
- Static power is increasing
- Increase of the digital noise
- Reduced drive current,

  $$I \approx C_{ox} W V_{sat} (Vdd - Vt)$$

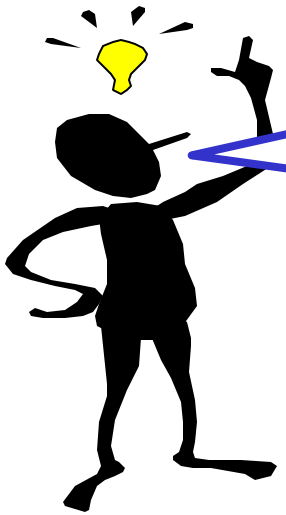
- Delay and power caused by the interconnect is getting more dominant
- Increased design-complexity

Disadvantages

Our approach to tackle DSM effects

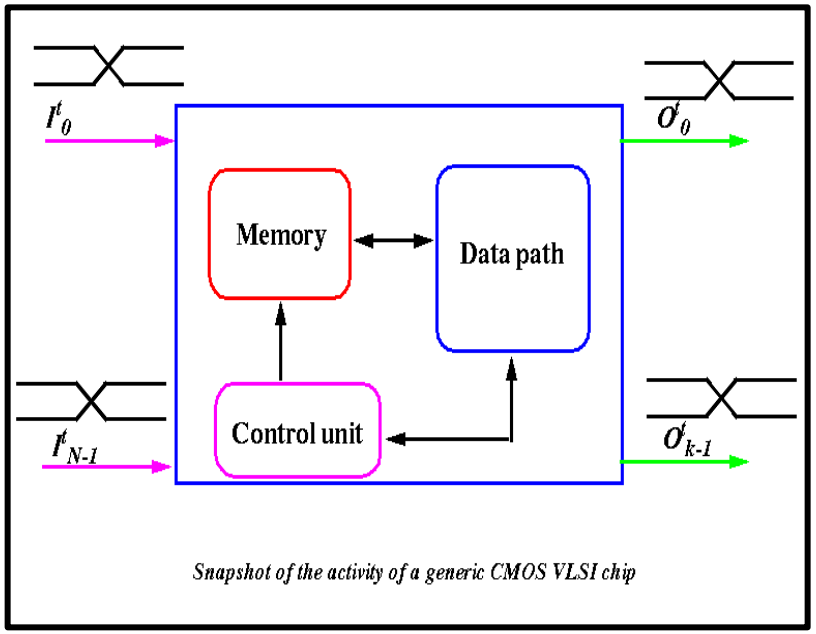


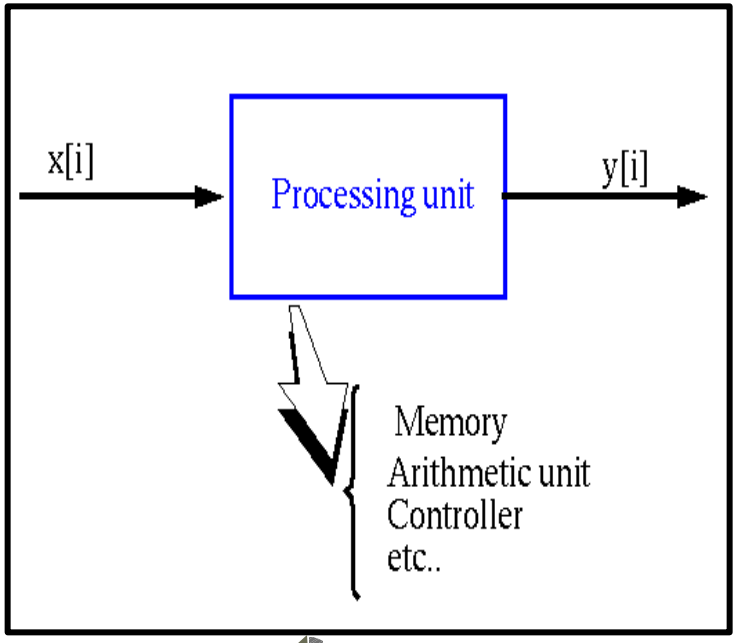
How can I get around DSM effects to achieve GSI ***without using expensive or special process***?



Use a ***signaling scheme*** that is *robust against DSM noise* and allows for ***low-power, high-speed*** communication between digital blocks!

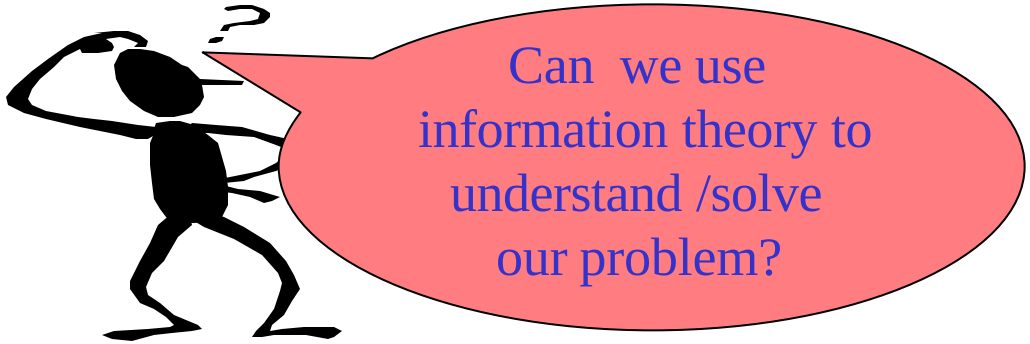
On-chip signaling in DSM



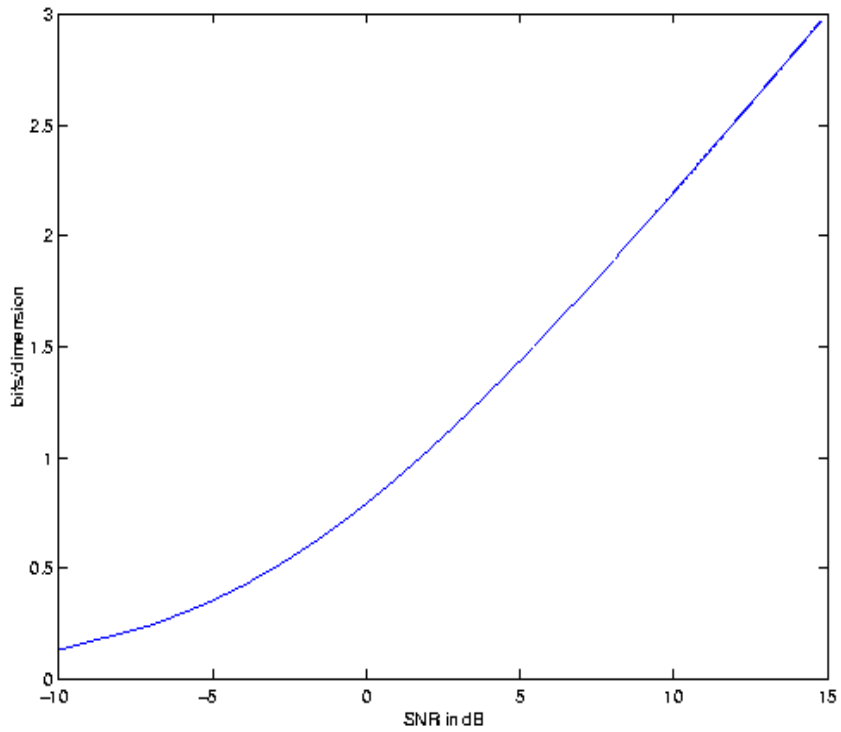


Is there a clever way to model the VLSI circuit?

Problem formulation



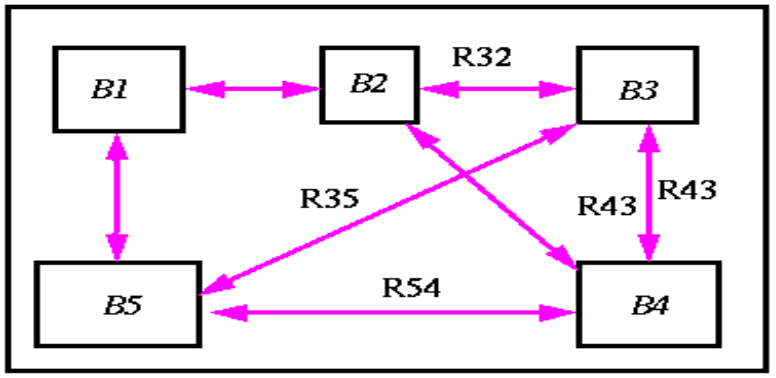
Information ***can be transmitted*** through a ***noisy channel*** at **a rate nearly equal to** the ***channel capacity***(j)



Shannon theorem (1948)

j ° $B\log_2(1+P/(BN_0))$, ***B: bandwidth, P: symbol power,*** N_0***: PSD of the AWGN***

Problem Formulation, Contd.



↔ : On-chip interconnect with finite bandwidth

Rij : signaling rate from *Bj* to *Bi*

OPT

Let $\gamma ij = Watts/Rij$, the quantity that measures the power efficiency.

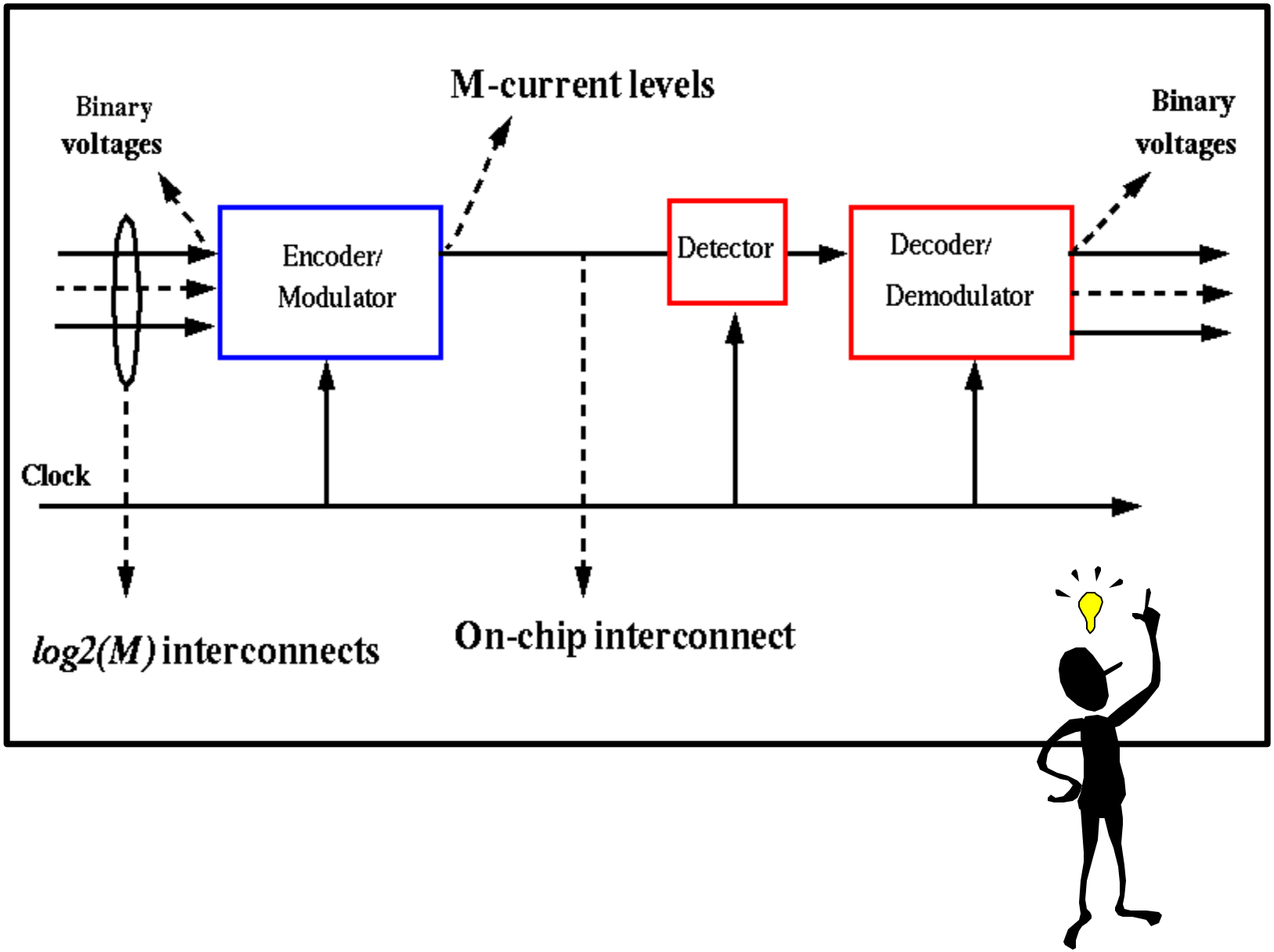
For each communication from *j* to *i* at a rate ***Rij***, our objective is to solve the following optimization problem.

Minimize γij ***subject to***

1) The achievable data-rate, from j to i, is equal to ***Rij***

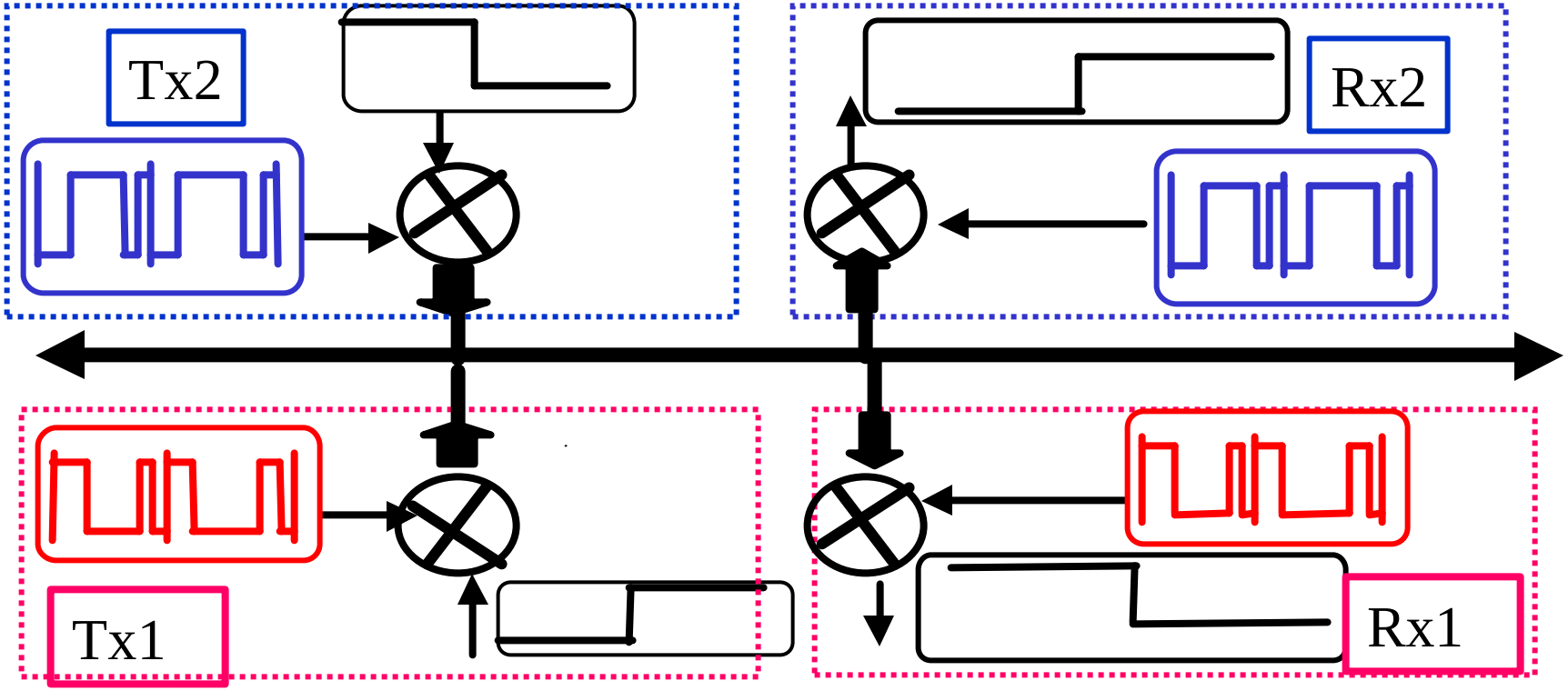
2) Bit-Error-Rate, $BERij <= \tau$

Our solution to solve ***OPT***



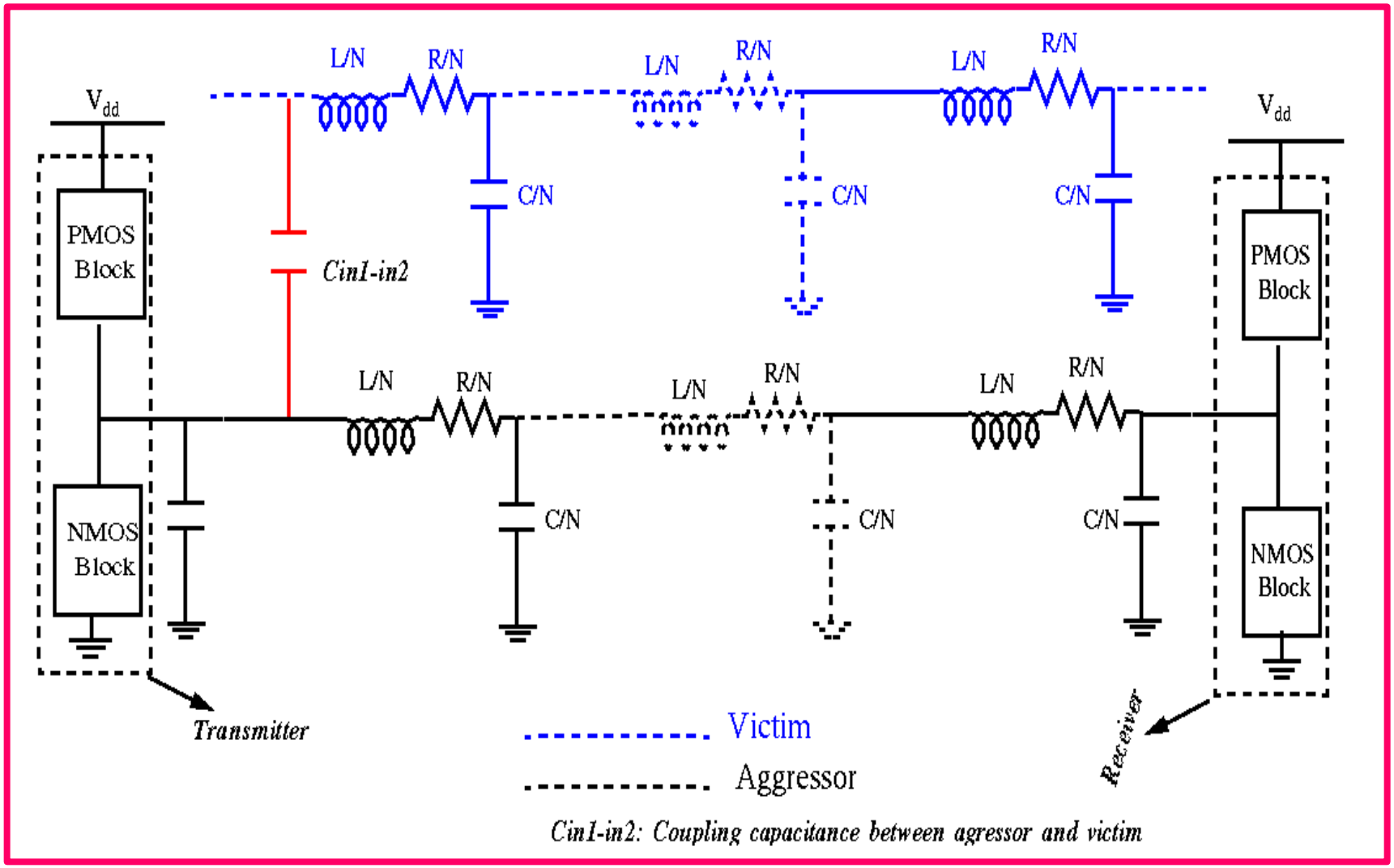
Related work

- Most reported techniques are based on reduced-voltage swing signaling with repeaters insertion.

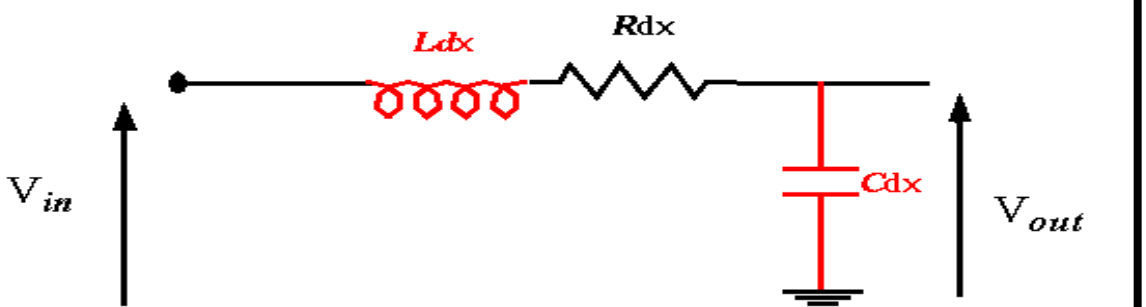


R. Yoshimura et al.,"*DS-CDMA Wired Bus With Simple Interconnection Topology for Parallel Processing System LSIs*", Proc. ISSCC, Feb.2000

On-chip interconnect (in DSM)



Modeling of the OCI



In our experiments, L and C were obtained using ***LINPAR***

(Matrix Parameters for Multiconductor Transmission Lines)

Resistance

ρ: resistivity

Skin effect depth, $\boldsymbol{f_d}$

$$R \equiv \begin{cases} \rho/(w \times h) & if \quad 0 \le f \le f_\delta \\ (\sqrt{f \times \pi \times \mu \times \rho})/(w \times 2) & if \quad f > f_\delta \end{cases}$$

$$f_\delta \approx \frac{\rho}{\pi \times \mu \times w^2}$$

Capacity of the OCI

$$\zeta(L, R, C, d) = Cd^2\sqrt{(R^2Cd^2 - 2L^2)^2 + 2.25L^2d^2}$$

$$\Delta(L, R, C, d) = 2LCd^2 - (RC)^2d^4 + \zeta(L, R, C, d)$$

$$B_2 = \frac{\sqrt{\Delta(L, R, C, d)}}{2.83\pi LCd^2}$$

$$\beta = 0.5(1 + sign(B_2 - f_\delta))$$

$$B = \beta\left[\frac{0.56w^2}{\pi^3 d^4 \pi\mu C^2}\right]^{1/3} + (1 - \beta)B_2$$

Shannon-Capacity of the OCI

$j \propto B\log_2(1+P/(BN_0))$, ***B: bandwidth, P: symbol power, N_0: PSD of the AWGN***

N_0 is a function of

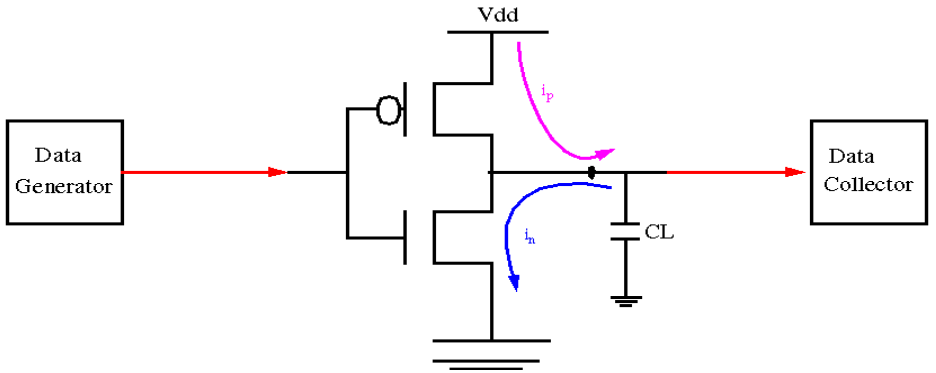
1) Fundamental noise
2) Cross-talk noise
3) Power-supply noise
4) Leakage noise,
5) Charge-sharing noise

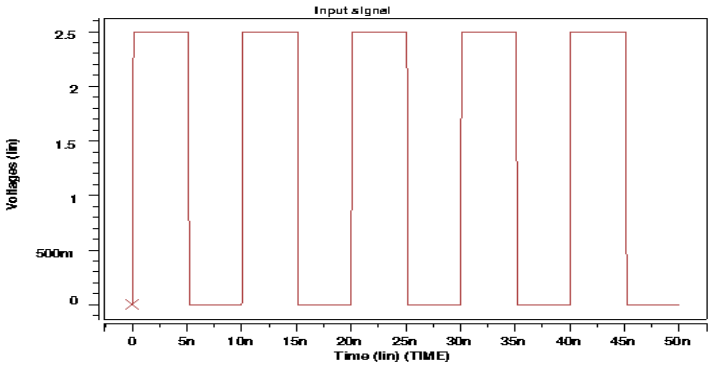
etc...

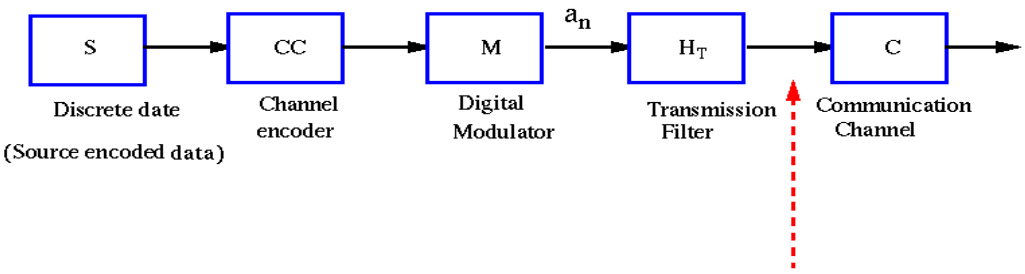
Upper-limit: $j \propto B\log_2(1+P/(BKT))$,

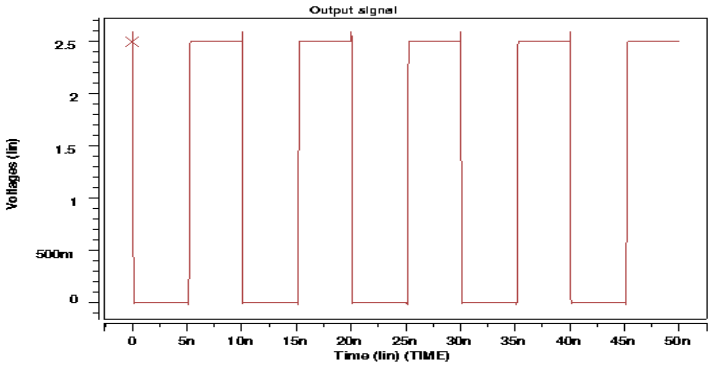
K: Boltzmann's constant, T: Device temperature

Voltage mode CMOS: Binary techniques

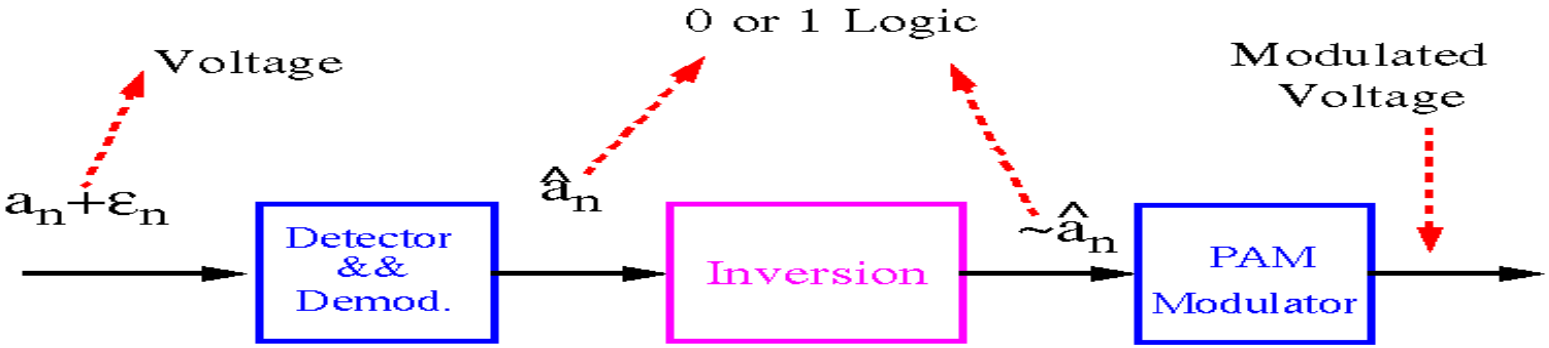




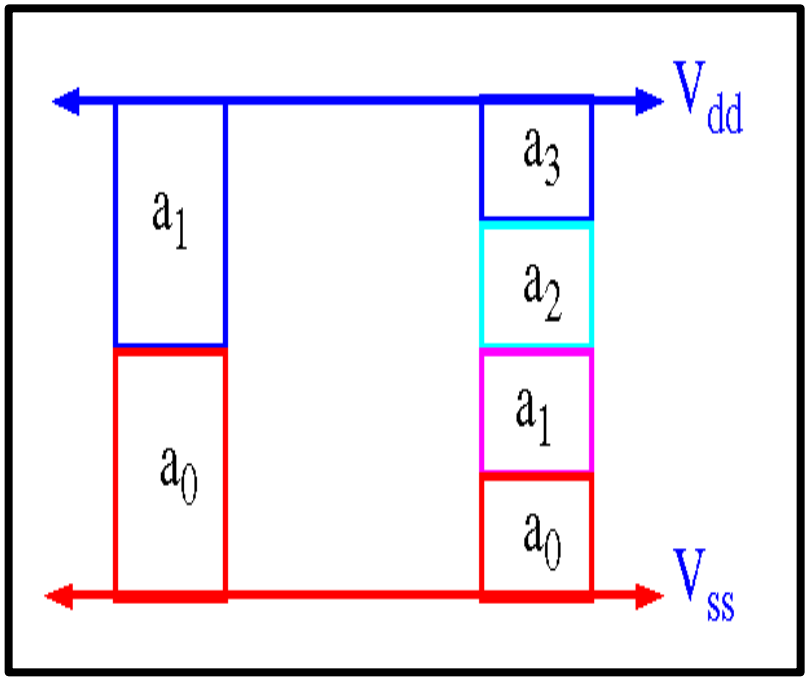


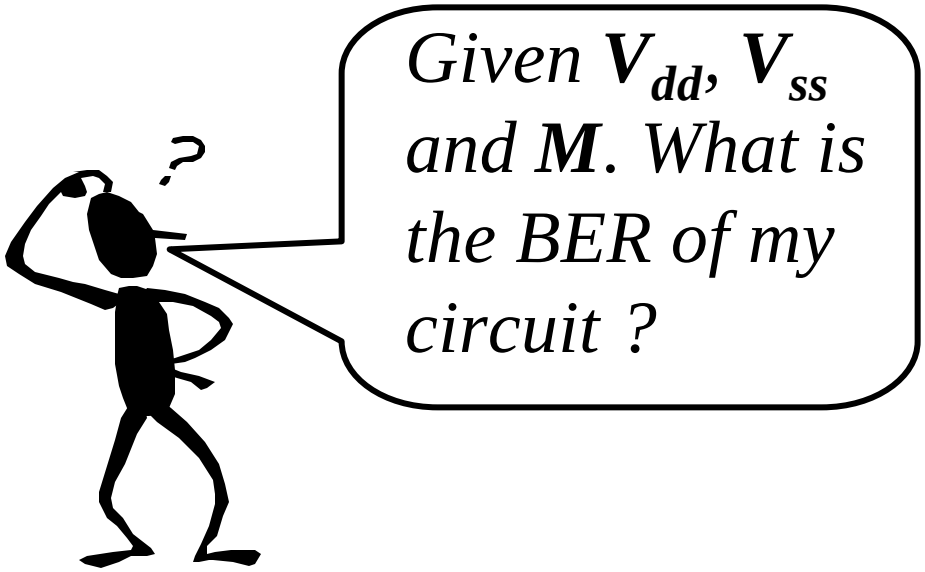


$$s(t) = \sum_{n=0}^{\infty} a_n \times h_T(t - nT)$$



Generalization: Multi-valued voltage mode

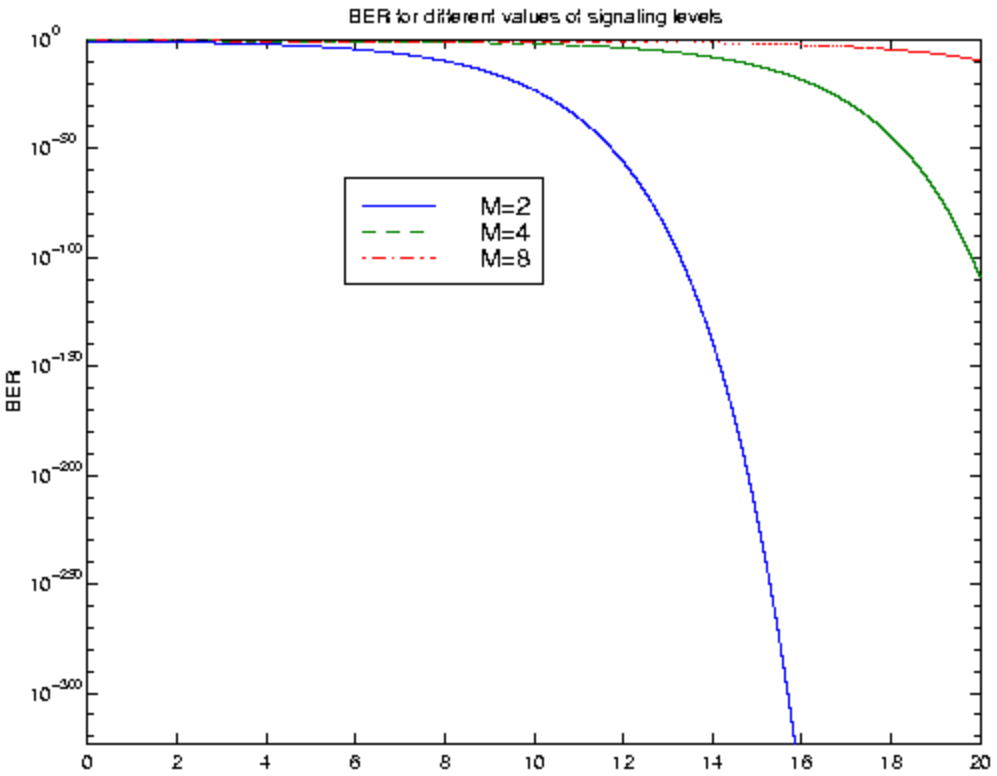




$$P_f = \frac{2(M-1)}{M\log(M)} Q\left(\sqrt{\frac{T_d V_{dd}^2 \log(M)}{(M-1)^2 N_0}}\right)$$

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{\left(-\frac{t^2}{2}\right)} dt$$

Why do we need to use higher values of M?



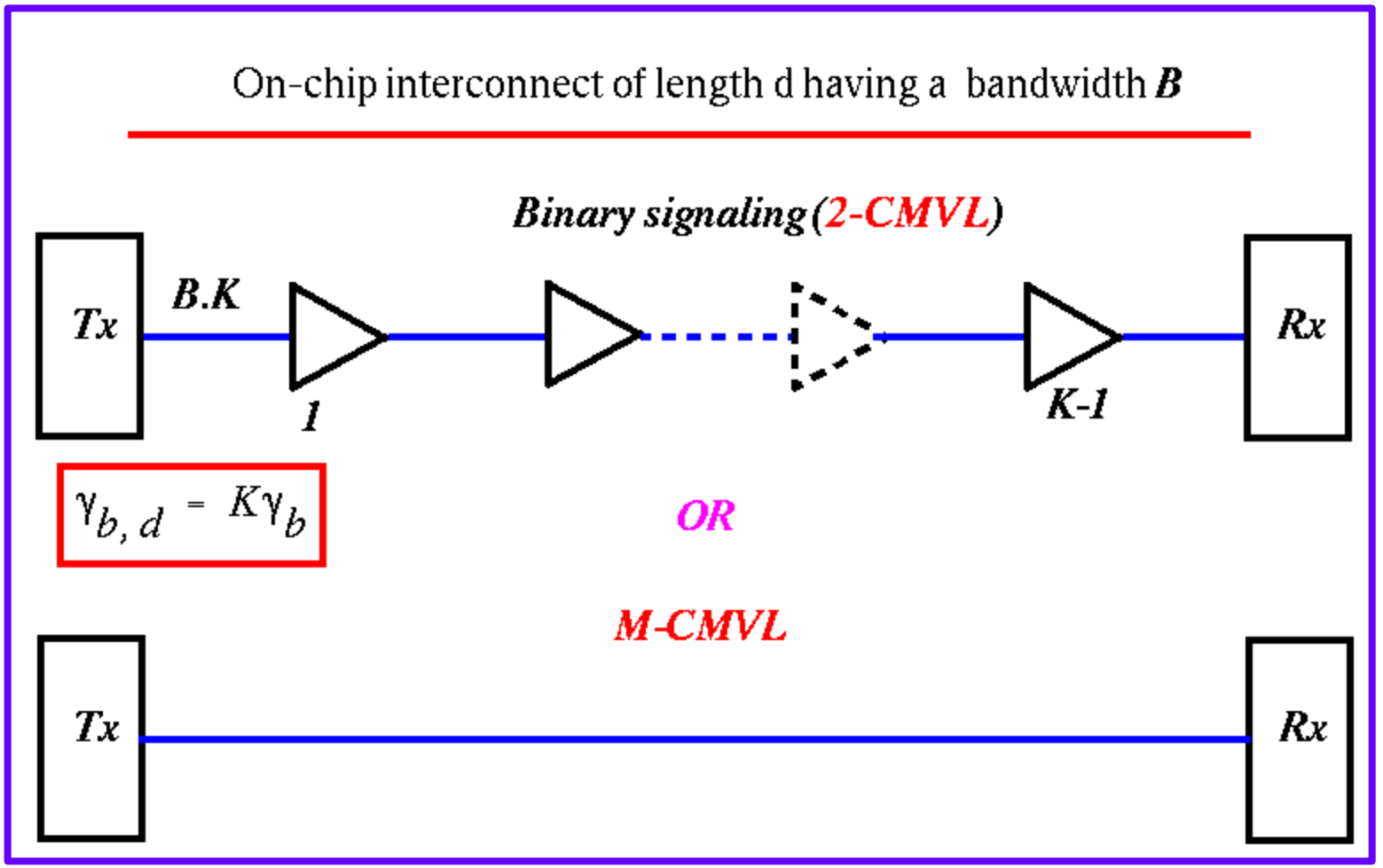
$$R_b = 2\log(M)\left[B = \beta\left[\frac{0.56w^2}{\pi^3 d^4 \pi\mu C^2}\right]^{1/3} + (1-\beta)B_2\right]$$

Robust signaling *(current vers. Voltage mode)*

- Robust against power supply noise
- It has lower g_{ij}
- Easy to generate multiple current sources without the need for DC-converters
- Better ***noise immunity***
- Lower delay
- **Widely used for off-chip signaling**
- ***But ….Mixed signal design***

Ref, W. J. Dally et al,"*Digital Systems Engineering*", Canbridge univ. press

Scenarios for high-speed signaling



E-VIJIM algorithm

For a given N_0, T_b, d, w, M_{max}, I, ρ, w, h, s, R_d, L and C

s=<>; /* The solution is initialized to NULL */
compute B
M=2, compute R_d denote this by R_b
if (Rb<= Rd)
    Compute d_{min} by setting R_d=R_b
    Compute K (number of regenerative repeaters)
    for k=1:K
        Compute I_{max}
        Compute $\gamma_{d,b}$
        Save the results to s
        Goto end-E-VIJIM
    Compute M
    Compute I_{max} and save the results to s
    Goto end-E-VIJIM
else
    compute I_{max} save the results to s
end E-VIJIM:
Select the minimum solution from S. If the value of I_{max} is more than I then print an error.

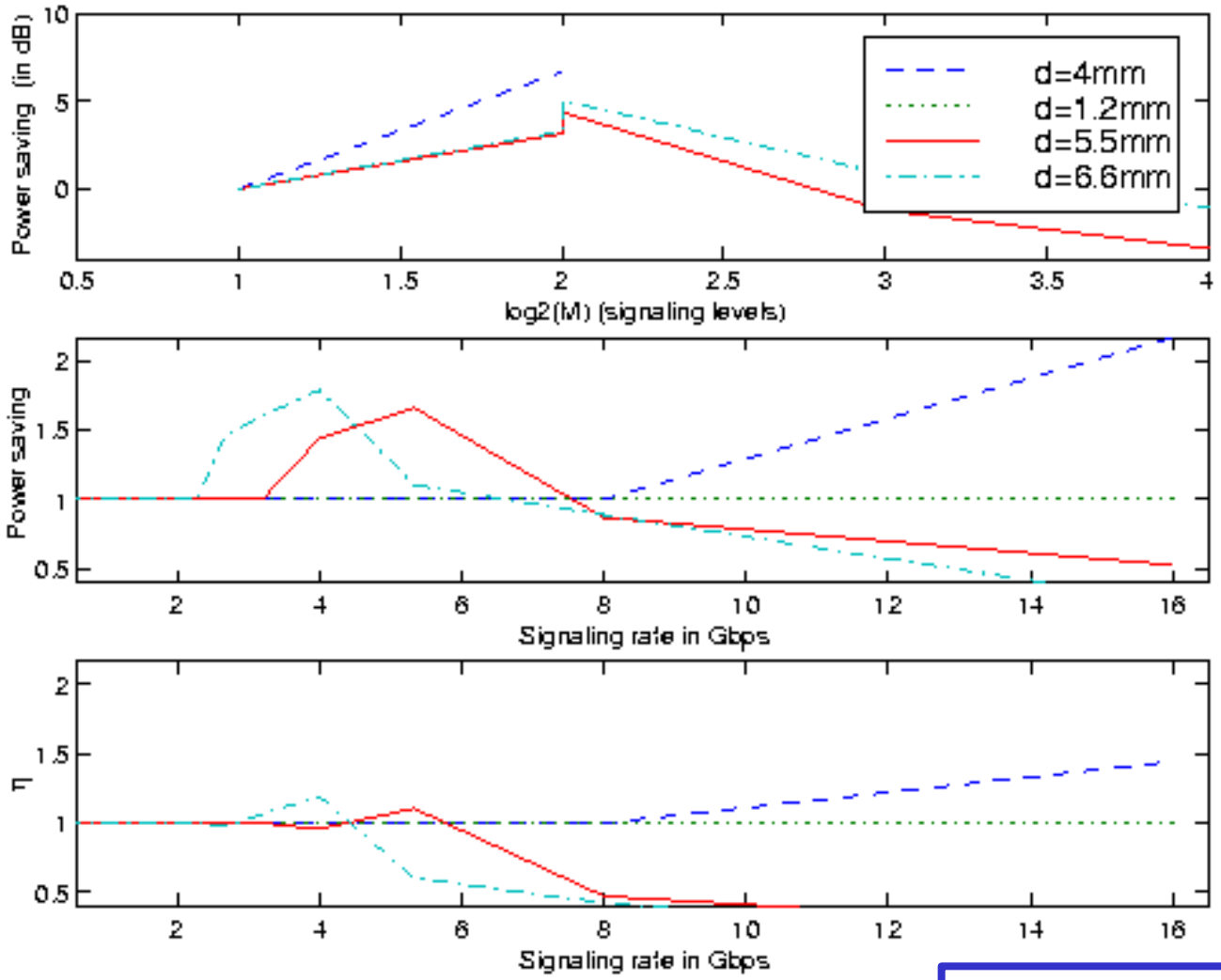
Experimental results (Metal-2)

conf.	w(μm)	h(μm)	s(μm)	L(H/m)	C(F/m)
CF1	0.13	0.26	0.13	3.30E-07	1.56E-10
CF2	0.86	1.72	0.86	1.92E-07	2.40E-10

d (mm)	fmaxh(GHz)	fmax(GHz)	error
0.1	250	248.3	0.68%
0.2	50	48.24	3.64%
0.4	11	10	10%
0.5	6.4	6.29	1.74%
0.6	4.4	4.32	1.85%
0.7	3.2	3.15	1.58%
0.8	2.5	2.4	4.16%
1	1.59	1.53	3.92%
2	0.3	0.38	21%
3	0.16	0.16	0%
4	0.09	0.09	0%
5	0.06	0.06	0%
6	0.042	0.04	5%
7	0.032	0.03	6%
8	0.024	0.023	4%
9	0.019	0.018	5%
10	0.0156	0.015	4%

Contd. (Metal-6)

d (mm)	fmaxh(GHz)	fmax(GHz)	error
0.1	348	477	27.00%
0.2	168	189.3	11.25%
0.4	80	75.12	7%
0.5	63	55.79	12.90%
0.6	50	43.75	14.28%
0.7	43	35.62	20.71%
0.8	37	29.81	24.11%
1	29	22.142	30.98%
2	12	8.78	37%
3	7	5.11	37%
4	4.14	4.12	0%
5	2.32	2.28	2%
6	1.45	1.45	0%
7	1	1	0%
8	0.73	0.74	1%
9	0.56	0.57	2%
10	0.43	0.46	7%



d<=1.2mm, 2-MVL is the optimum.

d=4mm, 4-CMVL is the opt. at 16GHz

d=5.5mm, f,600Mhz->5.33GHz,2-CMVL is the opt. From 5.33->8GHz, 4-CMVL is the opt.

Concluding remarks

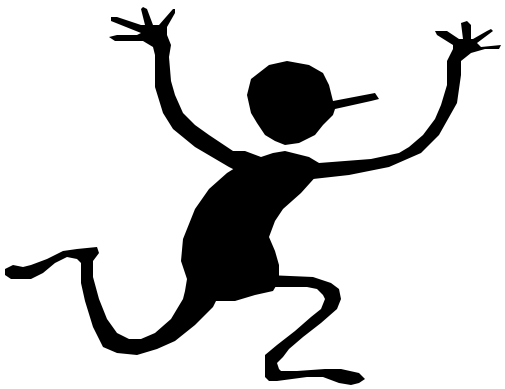
- Techniques for using M-CMVL current mode energy efficient high-speed signaling over on-chip interconnect were presented.
- An analogy between on-chip signaling and digital communication over band-limited channel was reported.
- A algorithm for computing channel capacity of the on-chip interconnect was derived. Our algorithm has an average error less than 10%
- A pseudo-code for fast searching of the energy efficient signaling was derived.

Contd.

- Implementation of E-VIJIM shows that up **to two times** improvement in power can be achieved if four current levels are used for on-chip signaling.
- Over 1.4 times area-improvement has been achieved.

4-CMVL is the most promising candidate for signaling over long-on chip interconnect.

- ***Bottleneck:*** Mixed Signal Design



Currently, encoder-decoder is being implemented. The results will be submitted to the special issue of "on-chip signaling in DSM", Journal of Analog Integ. Circ. And Sig. Process.