Discussion D2:

Gigascale Integration(GSI) Interconnect Limits and N-Tier Multilevel Interconnect Architectural Solutions

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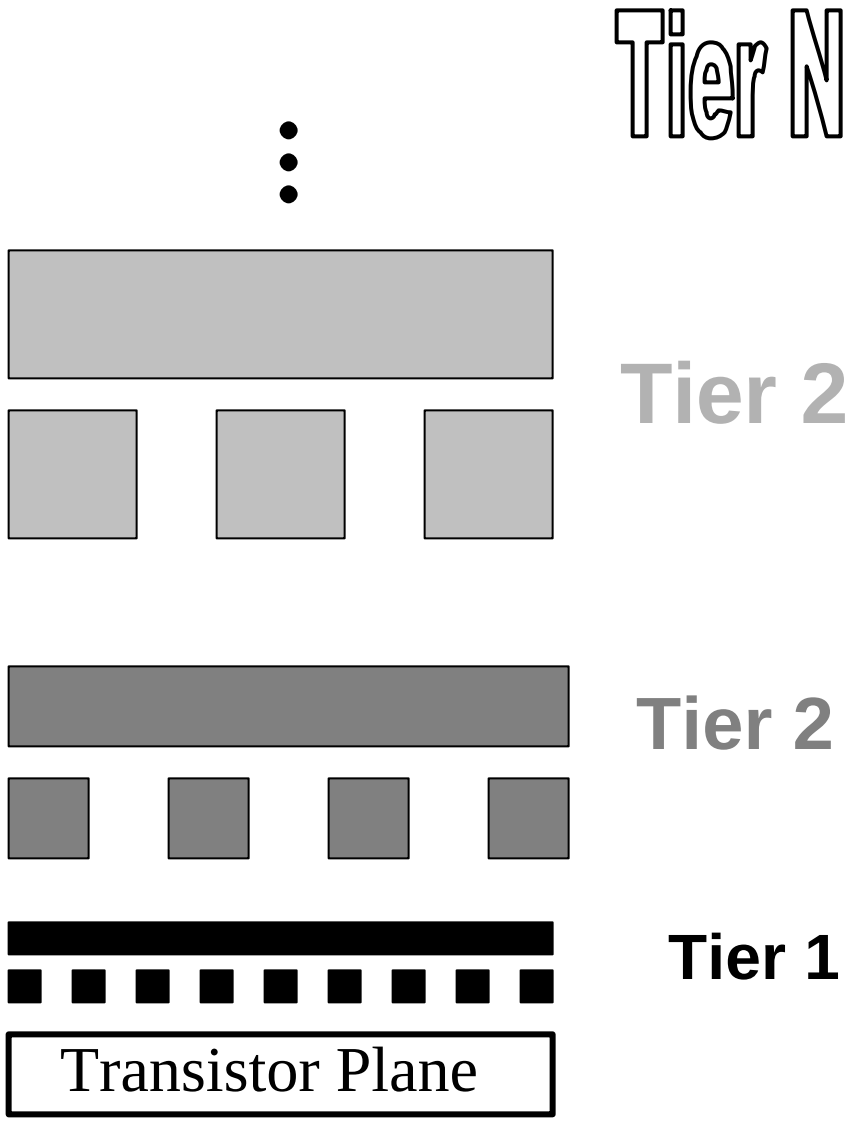
How extensively will interconnects limit future designs and what are the most feasible solutions to circumvent this problem?

The Interconnect Problem

Technology	MOSFET switching delay (t_d=CV/I)	Intrinsic delay of ***minimum scaled*** 1mm interconnect	Intrinsic delay of ***reverse-scaled*** 1mm interconnect	W/F
1.0μm (Al,SiO2)	~20ps	~5ps (RC = 1ps)	~5ps	1
0.1μm (Cu,low k)	~5ps	~30ps	~5ps	~2.4
35nm (Cu, low k)	~2.5ps	~250ps	~5ps	~7.0

Miniaturization does not enhance interconnect performance!!

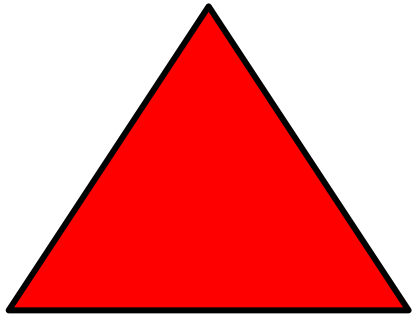
Reverse-Scaled N-Tier Architectures



*How will reverse scaling limit the **cost per function**??*

How do we explore future limits?

International Technology Roadmap for Semiconductors (ITRS)



Stochastic Wire-Length Distribution based on Rent's Rule

Compact Interconnect Models for delay, crosstalk, etc…

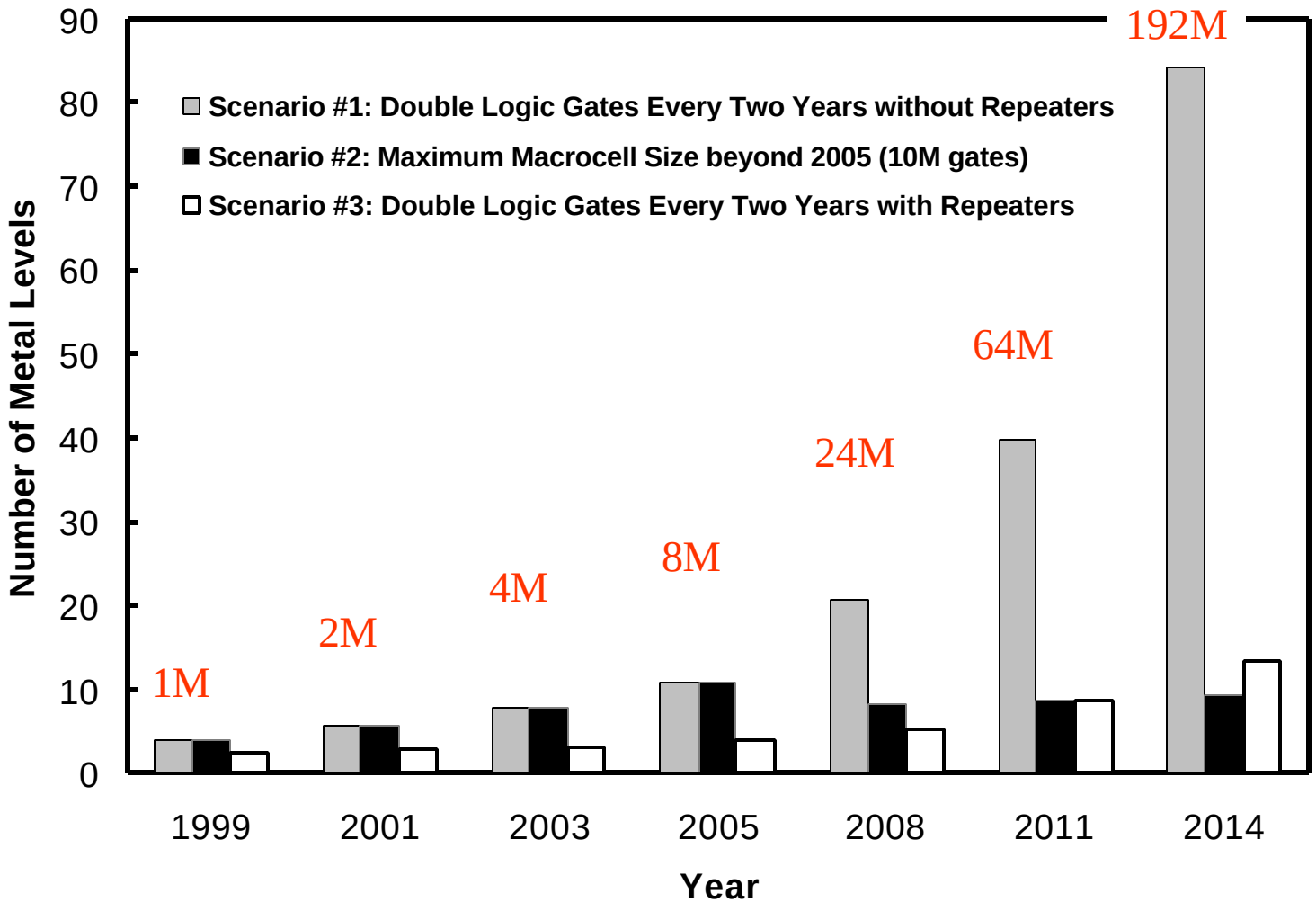
Assumptions for Projections of Limits

Maintain historical trends for:

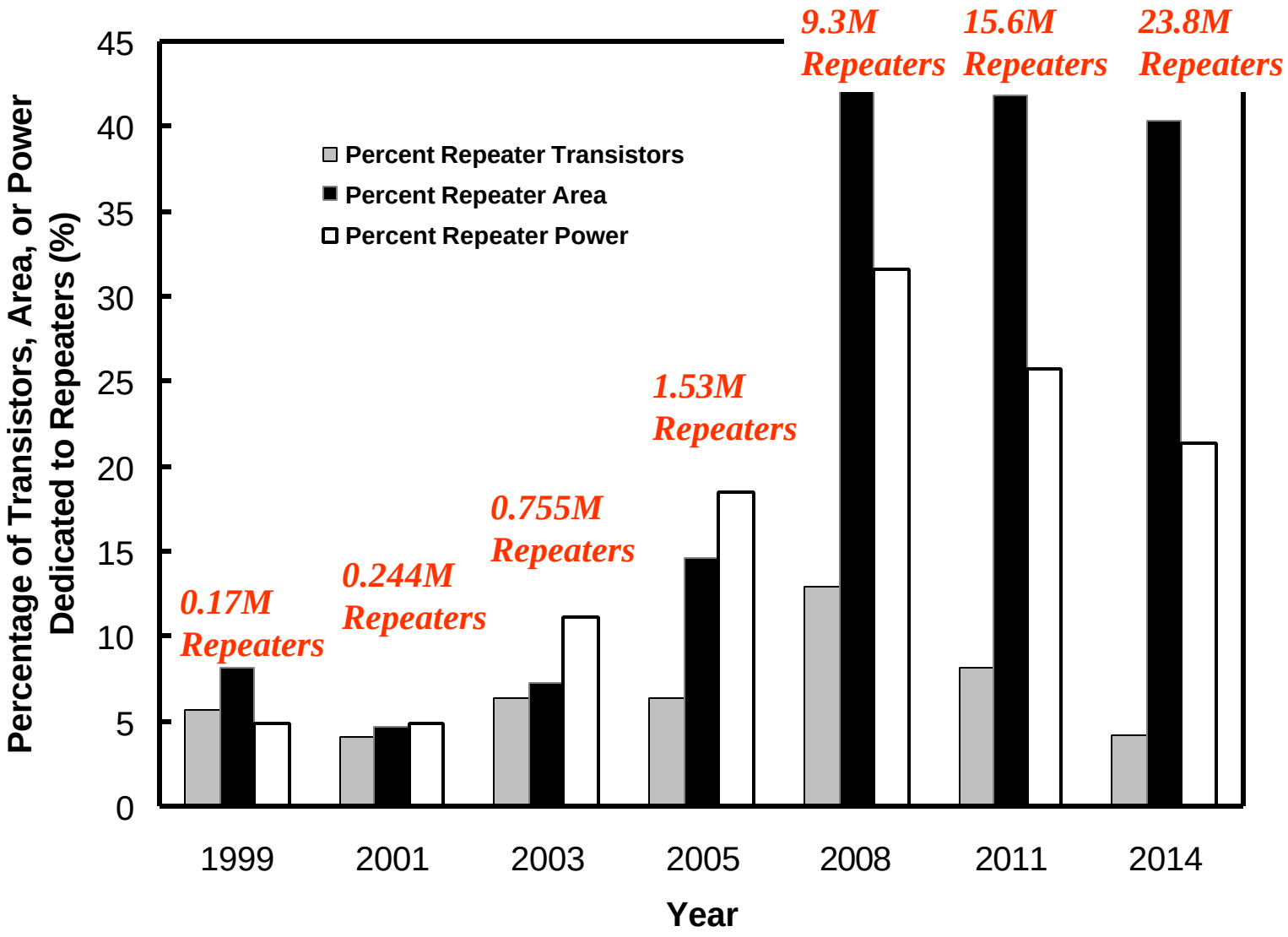
- **Cost per function!** (i.e. logic transistor density)
- **Performance!** (i.e. clock frequency)
- **Technology!** (e.g. minimum feature size)
- **System Complexity!** (Highly-connected logic gates)

Question: Can we wire systems with less than 10 metal levels?

…if history continues



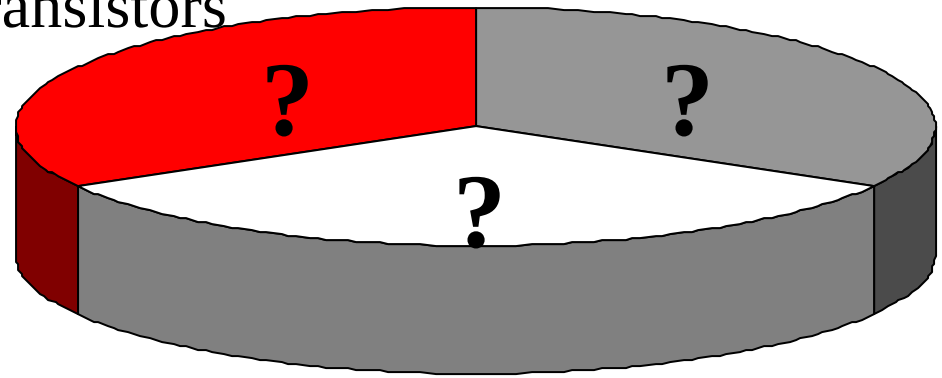
Repeater Architectures



Major shift in design strategies?

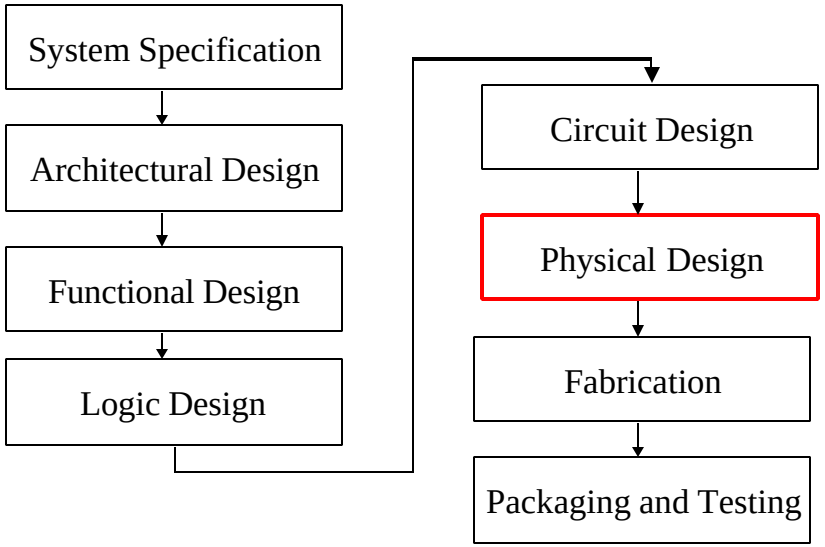
Interconnect Transistors

Memory Transistors



Logic Transistors

VLSI Design Cycle???



Questions to guide discussion:

- Is the repeater solution acceptable?
- What about via blockage?
- Can we effectively plan for repeaters in a design?
- Will system complexity increase or saturate?
- How feasible are other solutions (e.g. 3-D integration, optics, etc..)?
- What are some other major interconnect limits? (e.g. on-chip inductance, clock distribution, power distribution, etc…)