Power Supply Design Parameters Prediction for High Performance IC Design Flow

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Summary

- Introduction: noise in VLSI circuits
- IR drop and $L\frac{dI}{dt}$ causes, scale and consequences
- Proposed methodology to face these problems
- Power Supply Model
- Noise cost function
- Conclusions

Introduction: noise in VLSI circuits

Technology scaling down leads to:

- **increasing chip size**
- **increasing clock frequency**
- **increasing interconnect density**

$\Rightarrow$ **noise jeopardizes *UDSM* circuits functionality:**

- **crosstalk**
- **electromigration**
- **ground bounce**
- $L\frac{dI}{dt}$
- **IR drop**

IR drop causes

Transistor and interconnection scaling down causes

- increased gate number w/o area change
  - greater number of gates in a row
    - growing current on power supply lines
- increased line resistance

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- increased *GND* and *VDD* area for electromigration
- rise of **IR drop**

$L\frac{dI}{dt}$ causes

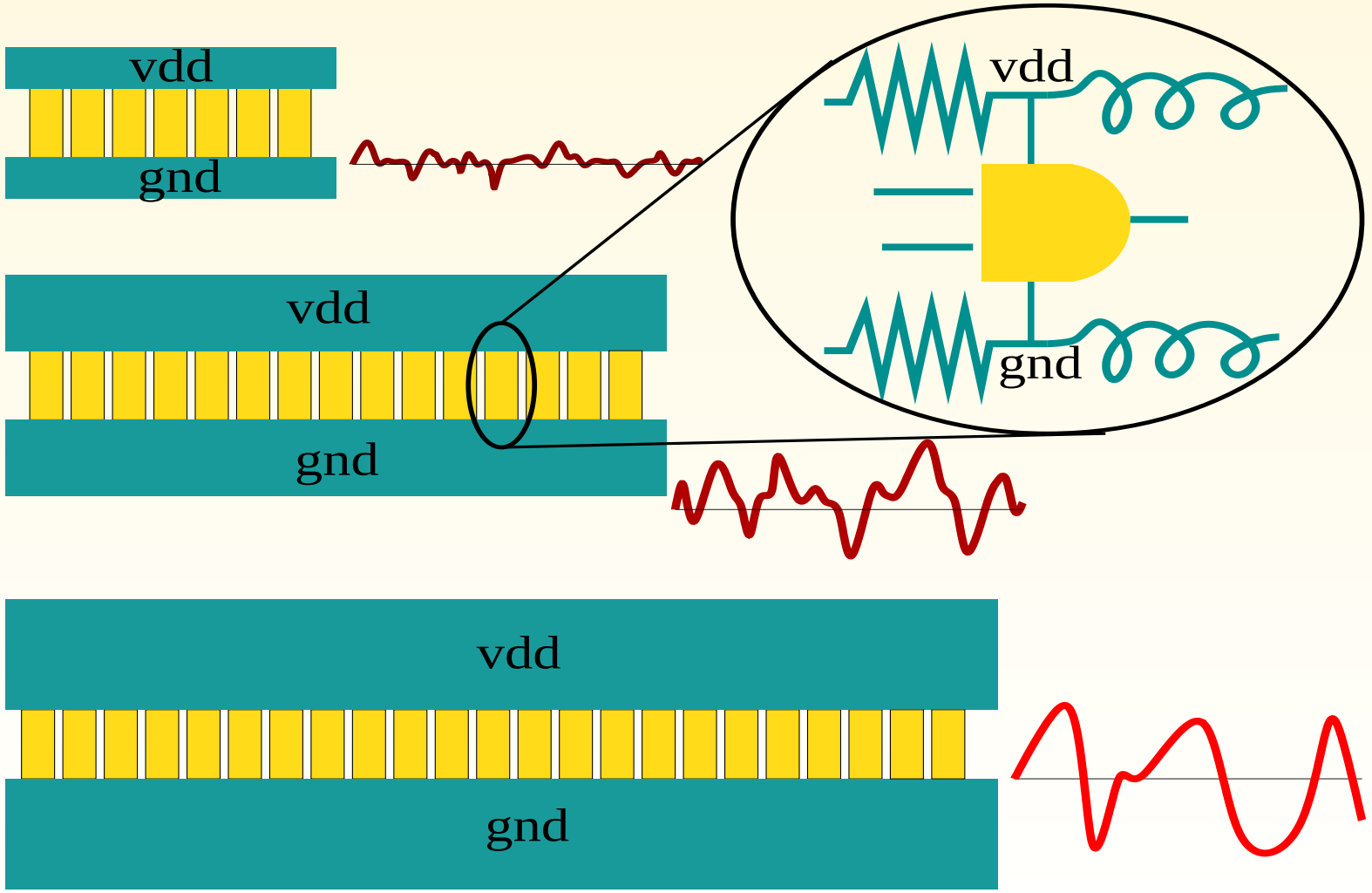
Transistor sizes scaling down causes:

- **increased frequency of the clock signal**
  - **higher gate switching activity**
    - **higher electromigration risk**
    - **decreased clock rise time: higher $L\frac{dI}{dt}$ for on chip and package inductances**

IR drop and $L\frac{dI}{dt}$ influences on Power Supply

- Higher sensibility of gates to noise spikes:
  delay, charge alteration, reduced V_t
- Crosstalk towards neighbor lines
- EMI problems towards neighbor circuits
- Ground bounce injected into the substrate

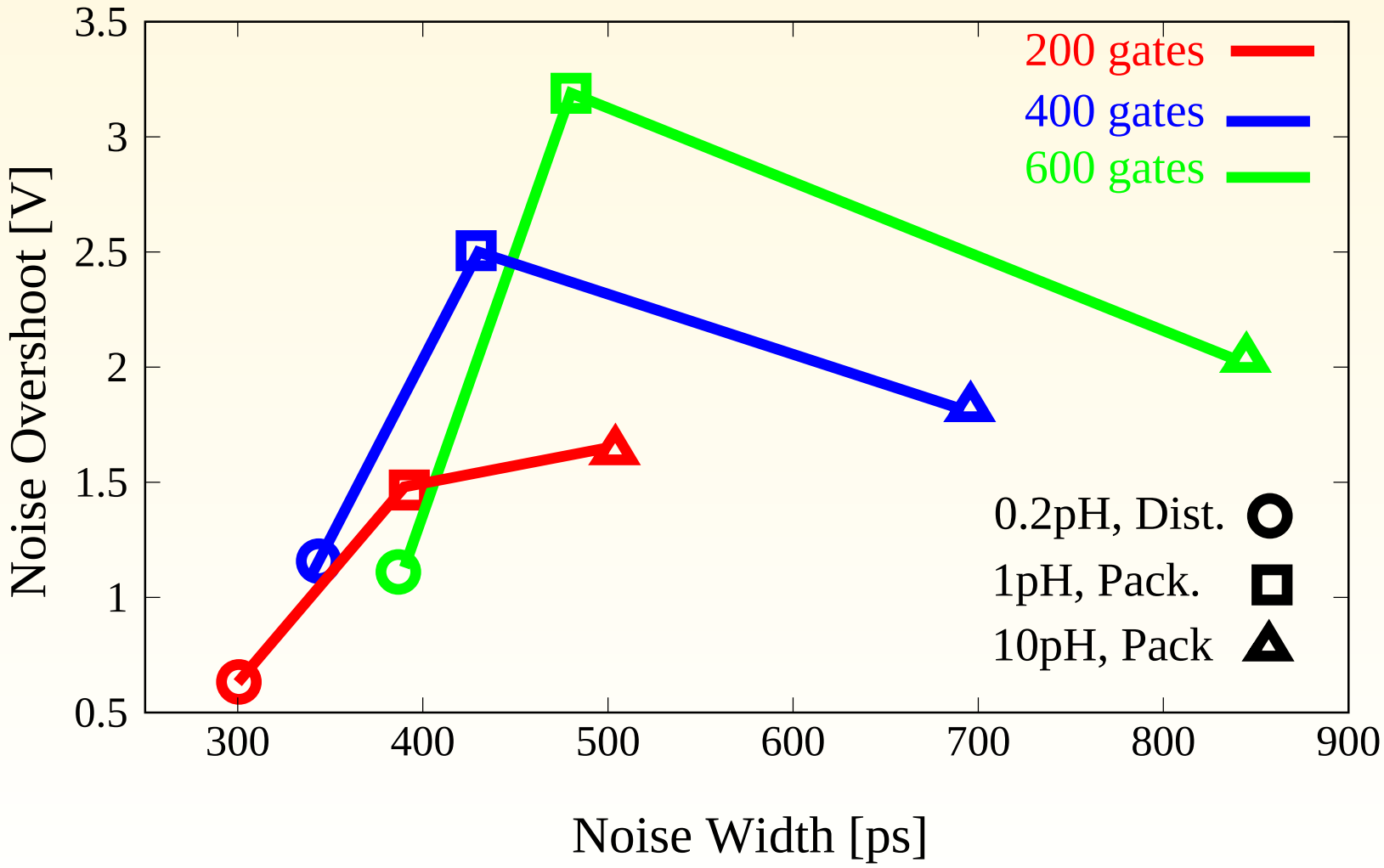
IR drop influence: simulations



IR drop: simulation parameters

- AND2 TSPC, 0.25μm, 2.5V, 1Ghz
- Growing number of cells: from 200 up to 600
- Different parasitic inductance conditions: on chip distributed (0.2pH), package (1pH – 10pH)
- Distributed parasitic resistance function of electromigration sizing

IR drop: simulations results

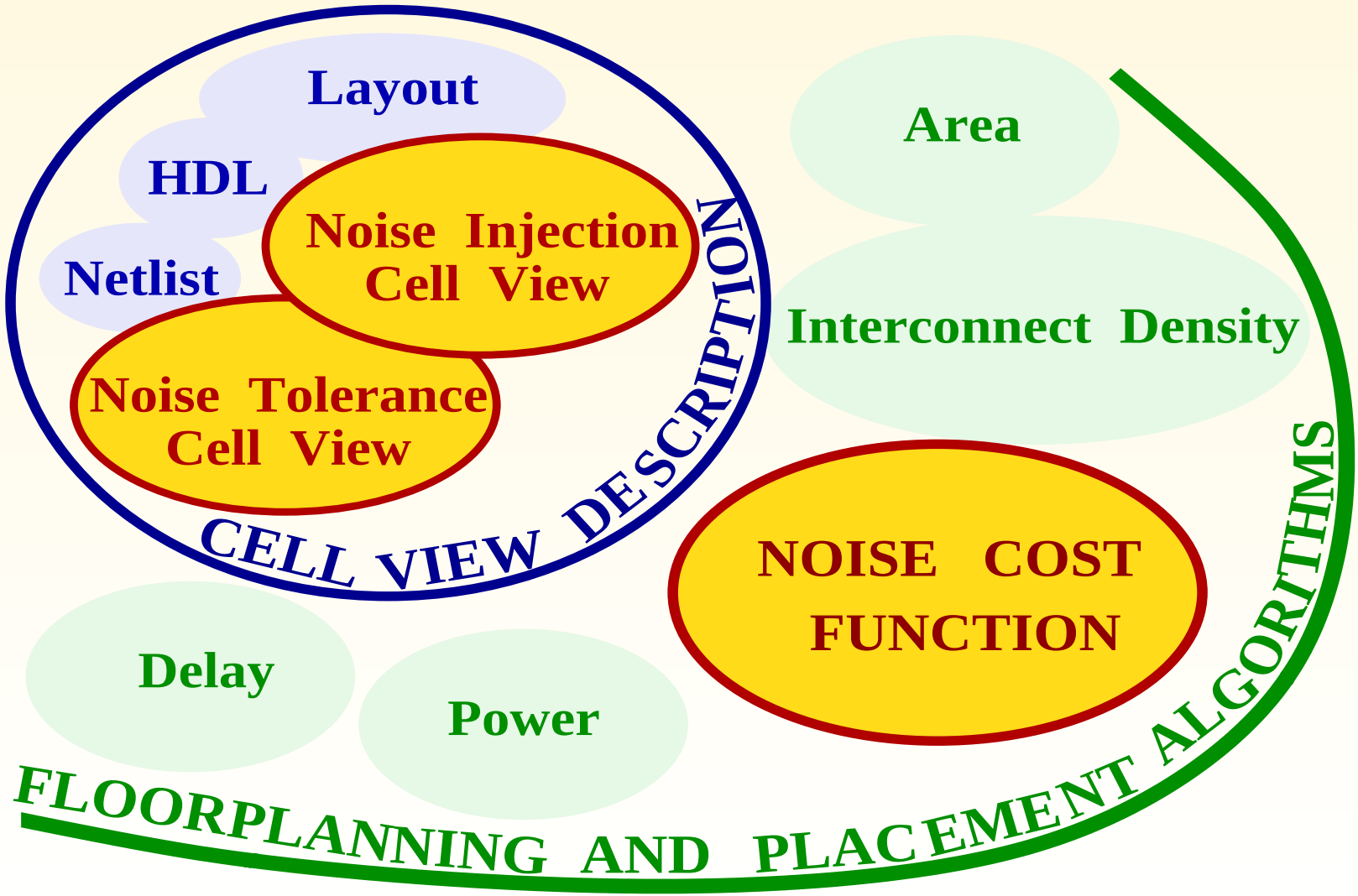


Verification or prediction?

- Verification of noise failures has expensive time-to-market aftereffects
- Countermeasures are strongly joined to designer intervention
- It's basic to develop design tools facing **early** in the design sequence the

  potential noise generation

Noise Cell Views and Cost Function

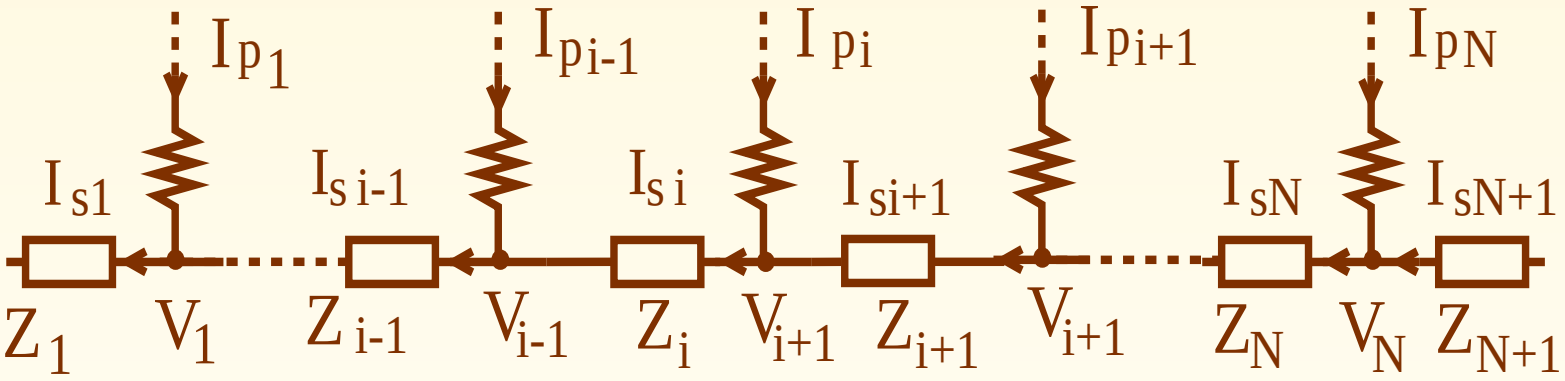


Methodology: instruments

Synergy among tools related to different design phases is needed:

- **transistor sizing optimization tool**
- **gate noise tolerance analysis**
- **cell model with noisy power supply references**
- **row of cells model: the influences between the cell and its environment**

Power Supply Model: uniform sizing



The maximum current is $I_{s1} = I_{sN+1} + N \cdot \mathbb{I}_p$

while the worst overvoltage is

$$V_N = V_0 + N\left(\mathbb{R}I_{sN+1} + \mathbb{L}\frac{d}{dt}I_{sN+1}\right) + \frac{N(N+1)}{2}\left(\mathbb{R}\mathbb{I}_p + \mathbb{L}\frac{d}{dt}\mathbb{I}_p\right)$$

Uniform sizing, noise prediction

Maximum noise overvoltage is known from the number of cells inserted on the line, or vice-versa

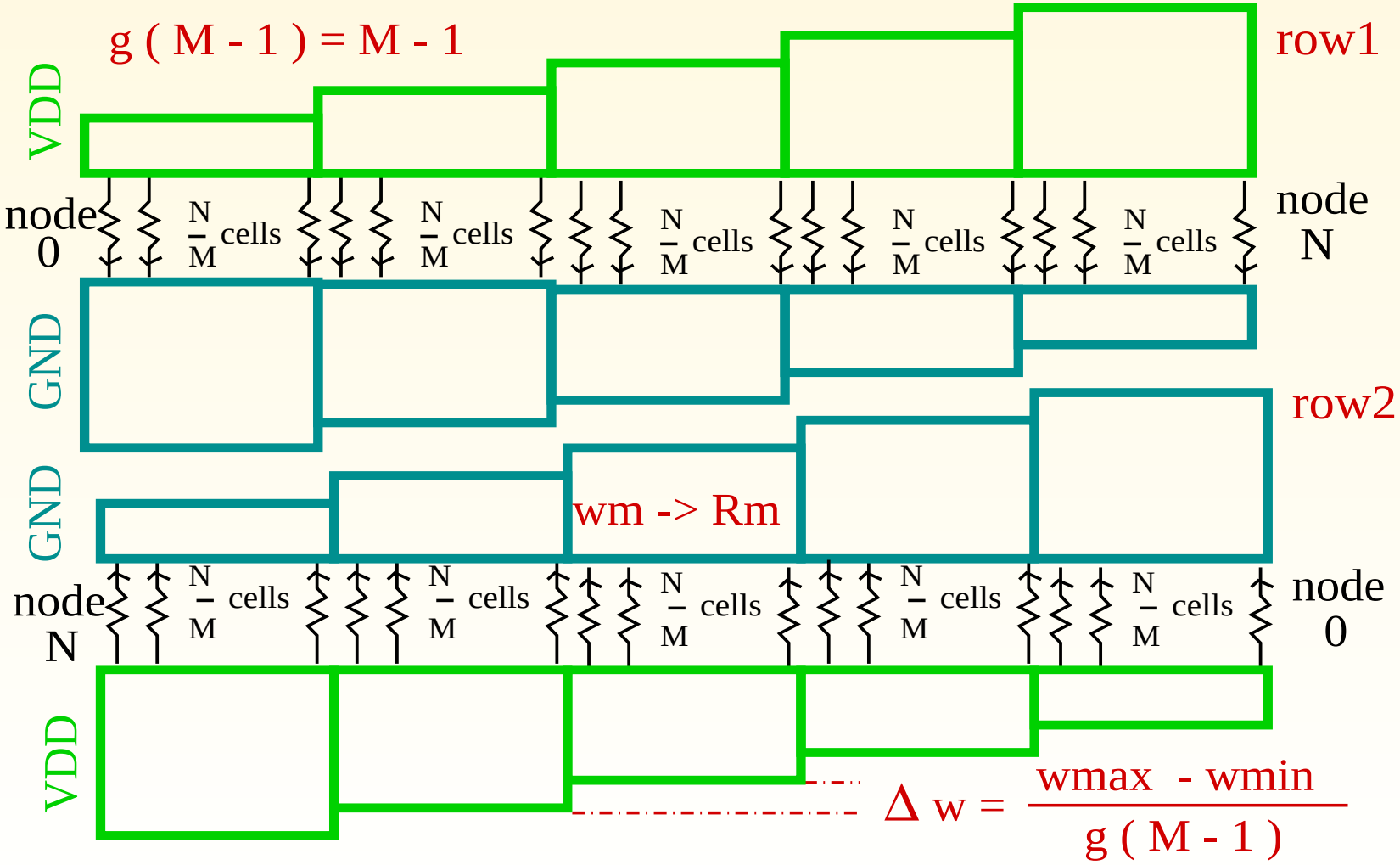
As a drawback the area of a *GND* line is:

$$A_{line} = N \cdot l_{gate} \cdot w_{MAX}$$

Area optimization without noise worsening

- Area waste due to worst current value used to dimension the whole line
- Ideal sizing: *GND* and *VDD* line width for cell i proportional to the maximum current at point i
- Real sizing: a controlled and optimized line segmentation is proposed

Optimized dimensioning



Optimized dimensioning: gain and loss

The area gain is $\Delta_A = -\frac{l_N}{2}\left(w_{MAX} - w_{MIN}\right)$

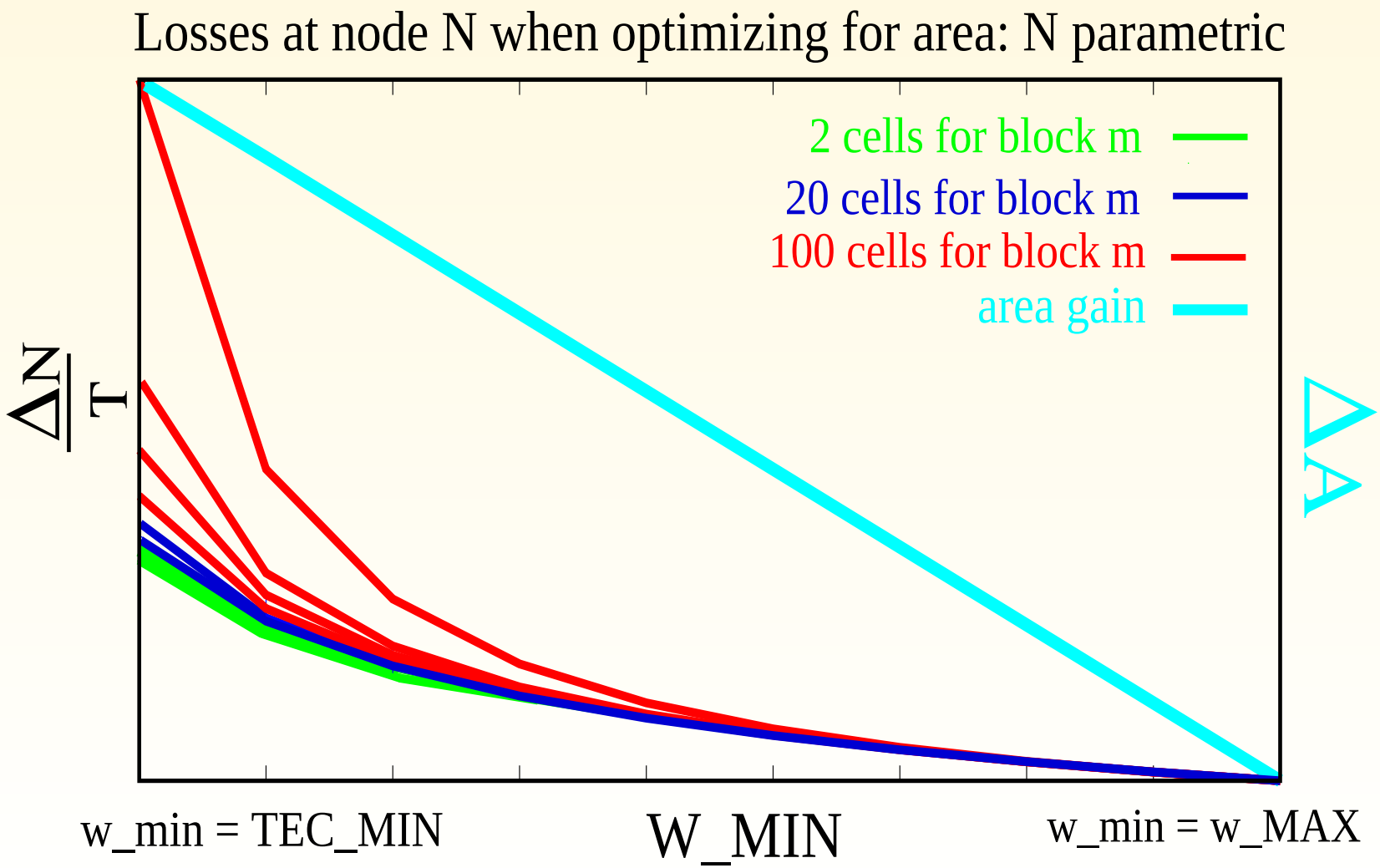
and the noise loss due to increased resistance is:

$$\frac{\Delta_N}{\mathbb{T}} = \left(\frac{I_{sN+1}}{I_{s1}}\left(\frac{1}{M}\sum_{m=1}^{M} f_m - 1\right) + \frac{\mathbb{I}_p}{I_{s1}} \cdot \left(\frac{1}{2}\frac{1}{M}\left(\frac{N}{M}+1\right) \cdot \right.\right.$$

$$\left.\left. \cdot \sum_{m=1}^{M} f_m + \frac{N}{M^2}\sum_{m=1}^{M}(M-m)f_m - \frac{N+1}{2}\right)\right)$$

where $R_m = \frac{\mathcal{R}_\square\, l_N}{N}\,\frac{1}{w_{MAX}}\, f_m\left(m, w_{MIN}, g(m-1)\right)$

Optimized dimensioning: overvoltage control



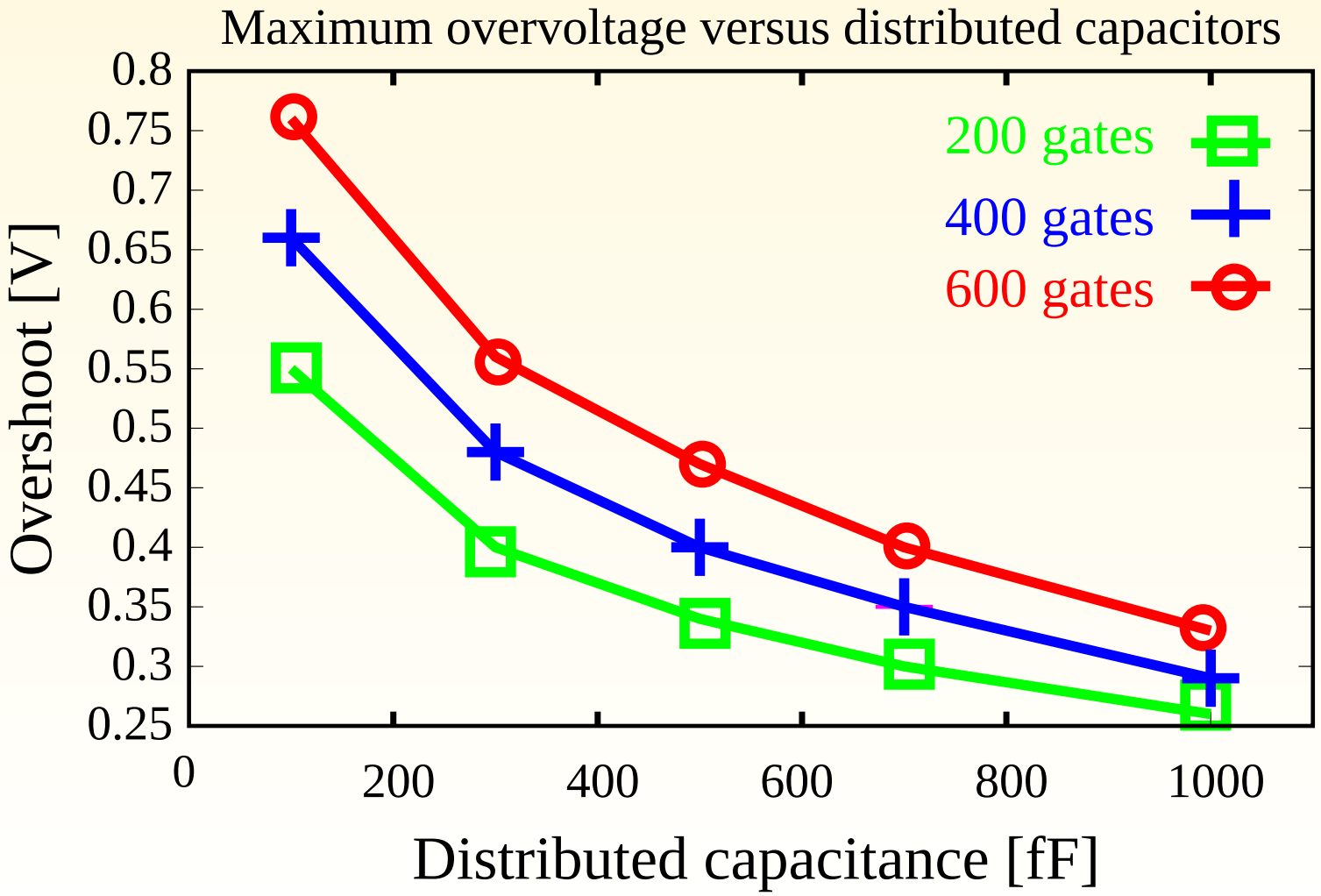
Optimized dimensioning: design parameters

Using a good number of segments with increasing dimensions the number of cells does not influence the loss in noise safety.

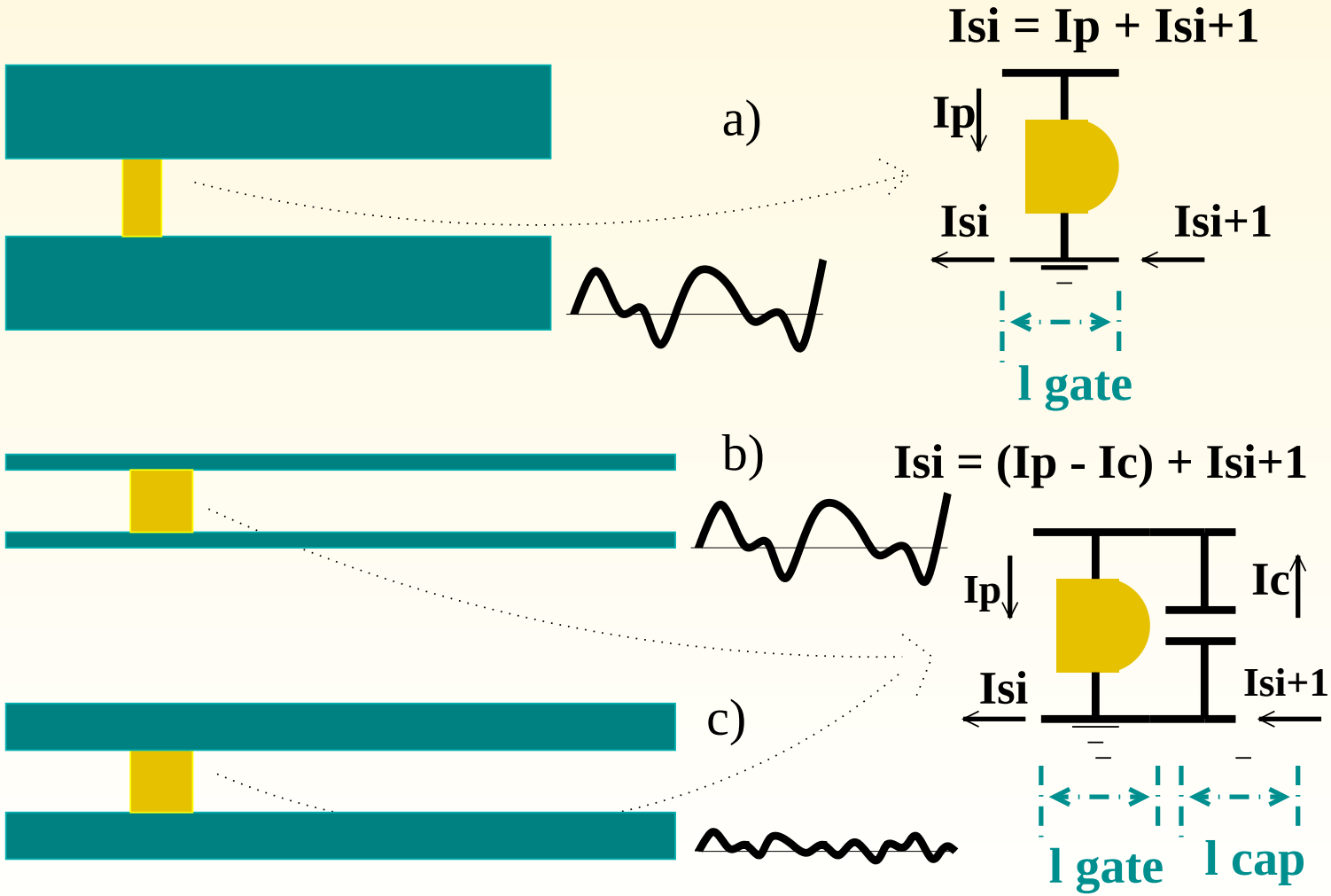
The designer has control on area and noise, varying

- **number of gates in a row** N
- **number of segments having different width** M
- **width at the line endpoints** w_{MAX}, w_{MIN}

Noise reduction: distributed capacitors



Decreased current to shrink resistance



Distributed capacitors: loss and gain

Noise overshoot variation

$$V_N\Big|_{cap}^{w_{\mathrm{MAX}}} - V_N = \mathcal{R}_{\square}\, t\, l_{cap} \cdot \frac{N}{2} - \mathcal{R}_{\square}\, t\, \frac{N}{2} \frac{\mathbb{I}_c}{\mathbb{I}_p} \left(l_{gate} + l_{cap}\right)$$

Area variation

$$A_{line}\Big|_{cap}^{w_{\mathrm{MIN}}} - A_{line} = \frac{l_{cap}}{t} N^2 \cdot \mathbb{I}_p - \frac{l_{gate} + l_{cap}}{t} N^2 \left(\mathbb{I}_p - \mathbb{I}_c\right)$$

Distributed capacitors design parameters

If the line width is chosen between

$$N\ (\mathbb{I}_p - \mathbb{I}_c)\left(1 + \frac{l_{gate}}{l_{cap}}\right) < w < \frac{N\ \mathbb{I}_p}{t}\frac{l_{gate}}{l_{gate} + l_{cap}}$$

and each cell in the library is connected to an optimized capacitor, a gain in noise and in area is assured with respect to the case w/o capacitors.

Future model developments

- conjunction of optimized dimensioning and of distributed capacitors insertions
- $\mathbb{I}_p = I_p(t)$ and $V_N = V_N(t)$
- clock skew modeling in the current superposition and overvoltage evaluation
- package influence on row model
- extension to S.O.C. designs

Noise Cost Function

A Noise Cost Function to be introduced in a placement algorithm is influenced as shown before by

- Noise overvoltage
- Power supply lines area
- Electromigration
- Number of cells in a row
- Distributed optimized capacitors
- Number of optimized segments

Conclusions

- The aim is to create a NOISE COST FUNCTION to be inserted in a placement algorithm
- it is based on:
  - a cell description with noise characteristics
  - a cell environment description with noise generation parameters
- it is of basic impact to face early in the design sequence the potential noise aftereffects