Hierarchical Power Supply Noise Evaluation for Early Power Grid Design Prediction

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Outline

- Power Supply Noise
- Power Supply Noise Analysis Approaches
- Proposed methodology
- Results and conclusions

Power Supply Noise

$$V_{suppy} \Rightarrow V_{ideal}$$

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$$\text{SSN} \Rightarrow L \cdot \frac{dI}{dt}$$

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$$V_{suppy} \Rightarrow V_{ideal}$$

$$\text{SSN} \Rightarrow L \cdot \frac{dI}{dt}$$

$$\text{Voltage Drop} \Rightarrow R \cdot I$$

$$\Downarrow$$

$$V_{suppy} = V_{ideal} + L\frac{dI}{dt} + R \cdot I$$

Resistance

Metal line shrinking

Skin effect

Temperature

Resistance

Metal line shrinking

Skin effect

Temperature

Copper

Fat wires

Inductance

Higher frequency

Complexity: return path

Inductance

Higher frequency

Complexity: return path

Shielding

Flip Chip technology

Current

Gate density increasing

$\Rightarrow$ higher currents

Higher frequency

$\Rightarrow \frac{dI}{dt}$ grows

Capacitance

Fat wires

$\Rightarrow$ interconnect capacitance increases

Reduced gate sizes

$\Rightarrow$ reduced intrinsic decoupling

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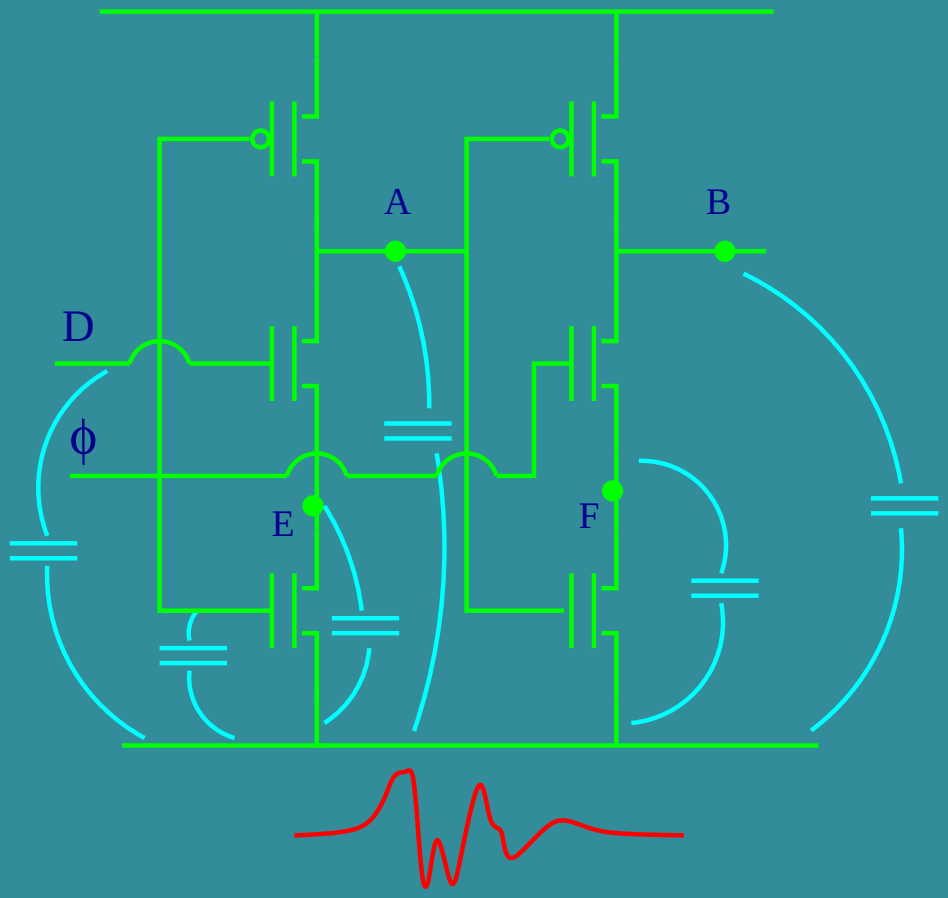
capacitance $\Rightarrow \frac{dI}{dt}$ grows

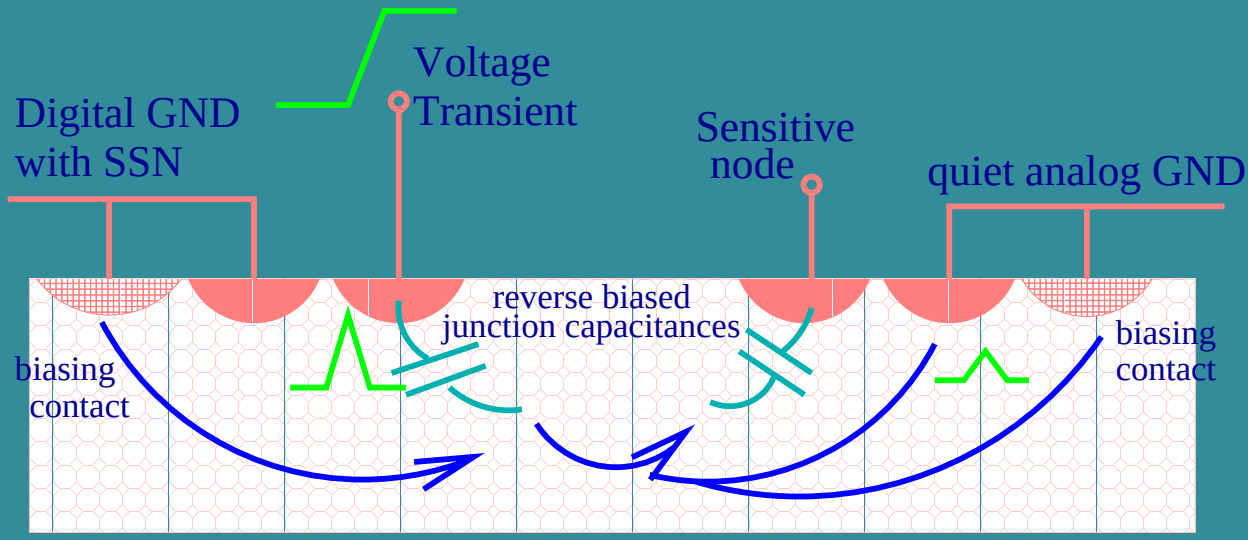
Low K materials

Effects: direct



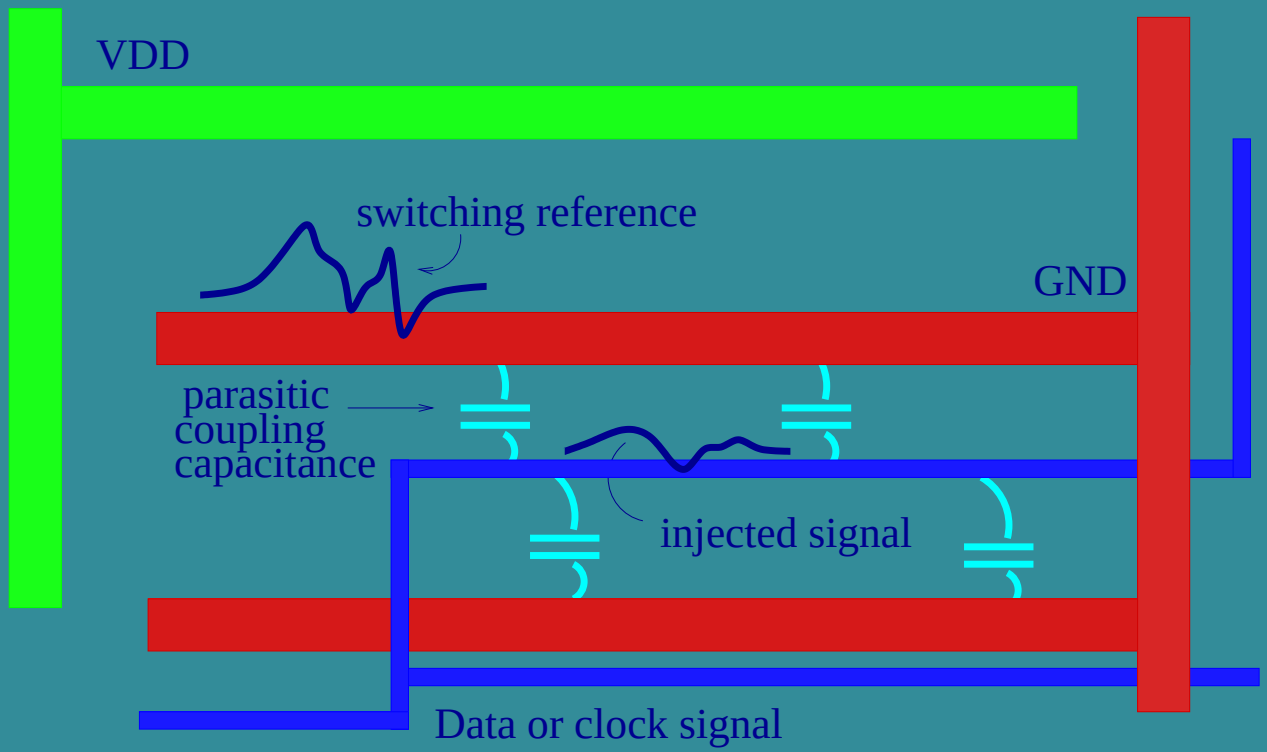
Gate delays, errors, failures

Effects: indirect



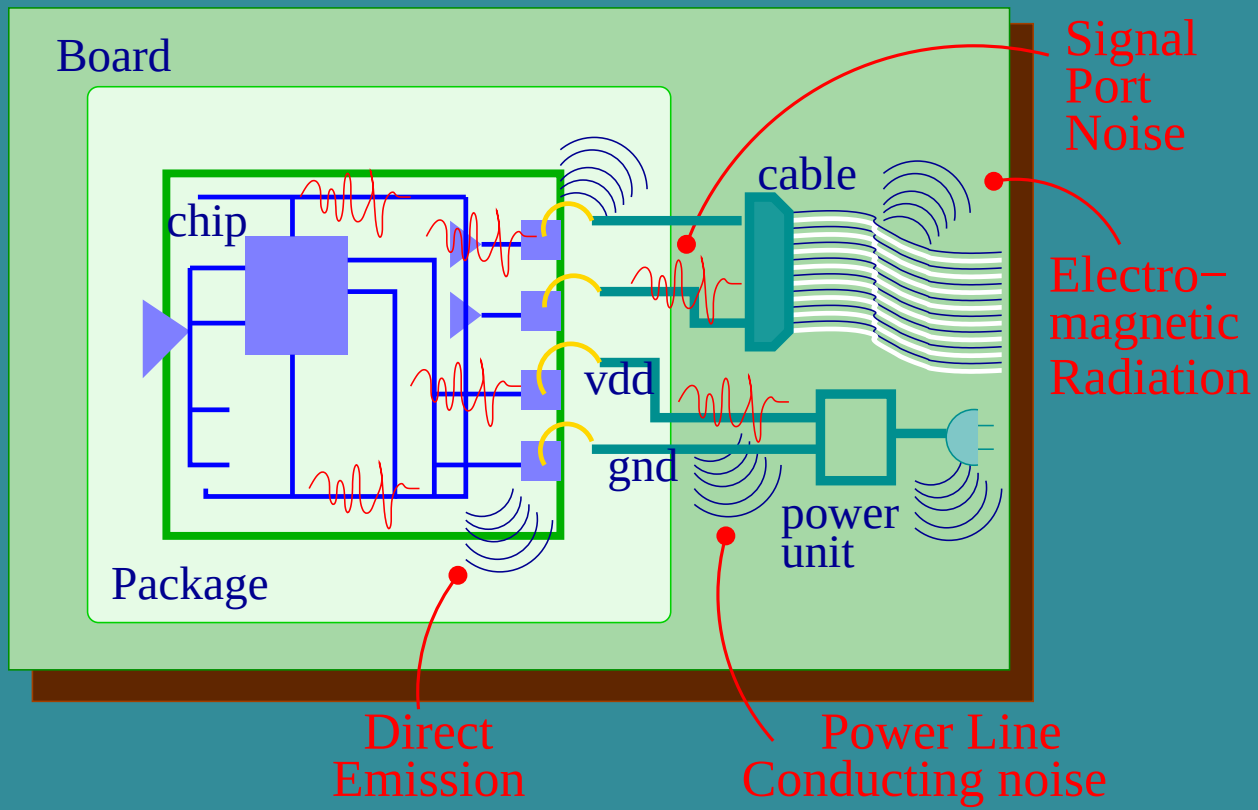
Substrate injection

Effects: indirect



Crosstalk against signal lines

Effects: indirect



Emi towards neighbours circuits

Countermeasures

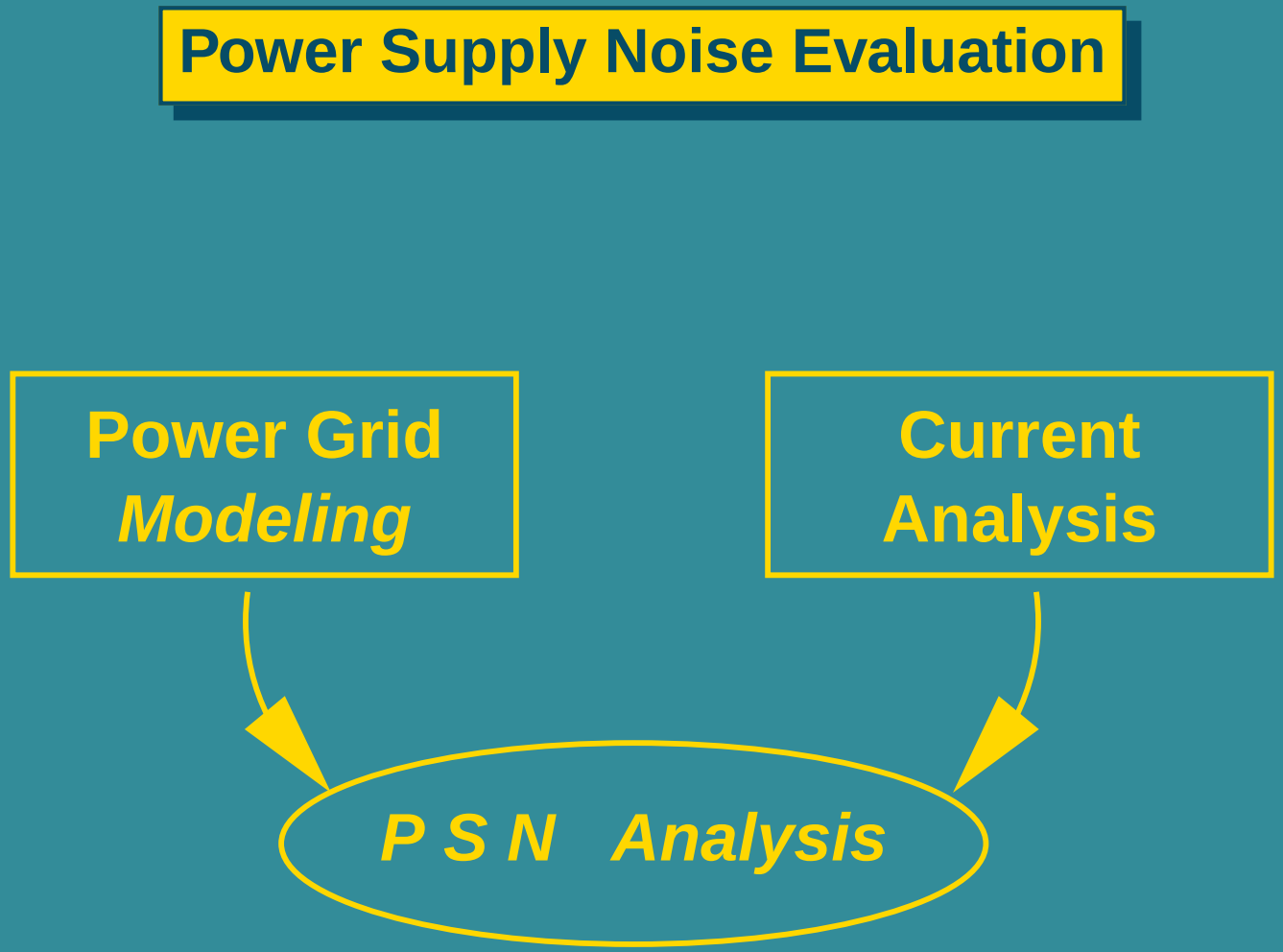
- Technologist: copper, Low-k, SOI, C4
- Circuit designer: decoupling capacitors, current limiters, logic family variation
- Physical designer: routing and placement strategies

$\Rightarrow$ early PSN evaluation

Power Supply Noise Evaluation Approaches

- Verification at the end of the design process: accurate but expensive
- Early analysis: has lower accuracy but gives a priori design parameters

PSN evaluation



Power grid analysis approaches

- Hierarchical analysis
  - Extract parasitics of a macro power grid
  - Simplify it in a concentrated model for that macro
  - Use it for the higher hierarchical analysis
  - Can be extremely inaccurate: the distributed effect is lost

Current analysis approaches

- Vector producing worst switching activity

  $\Rightarrow$ maximum switching $\not\equiv$ worst noise

- Simultaneous switching

  $\Rightarrow$ too pessimistic upper bound

- Static timing analysis for current skew evaluation

  $\Rightarrow$ too pessimistic: does not consider switching direction

PSN evaluation

Proposed method base on:

- Hierarchical current activity algorithm:
  - uses dynamic current informations (database)
  - consider switching direction
  - consider current skew
  - consider current in “no-switching” transitions
- Hierarchical Power Grid model
  - Infer distributed parasitic informations from lower to higher hierarchical levels
  - Include current informations for line sizing, parasitic evaluation and Power Supply Noise estimation

Proposed method

PSNA

1. **Define current activity (Current LUT, CAA, STA):**
2. **Define parasitics from line dimensions;**
3. **Compute power supply overvoltage (Model);**
4. **Define critical points;**
5. **Define possible solutions:**

5.1 **Increasing critical points line width or/and**

5.2 **Inserting decoupling capacitances or/and**

5.3 **Equalizing current injection (placement, TDP)**

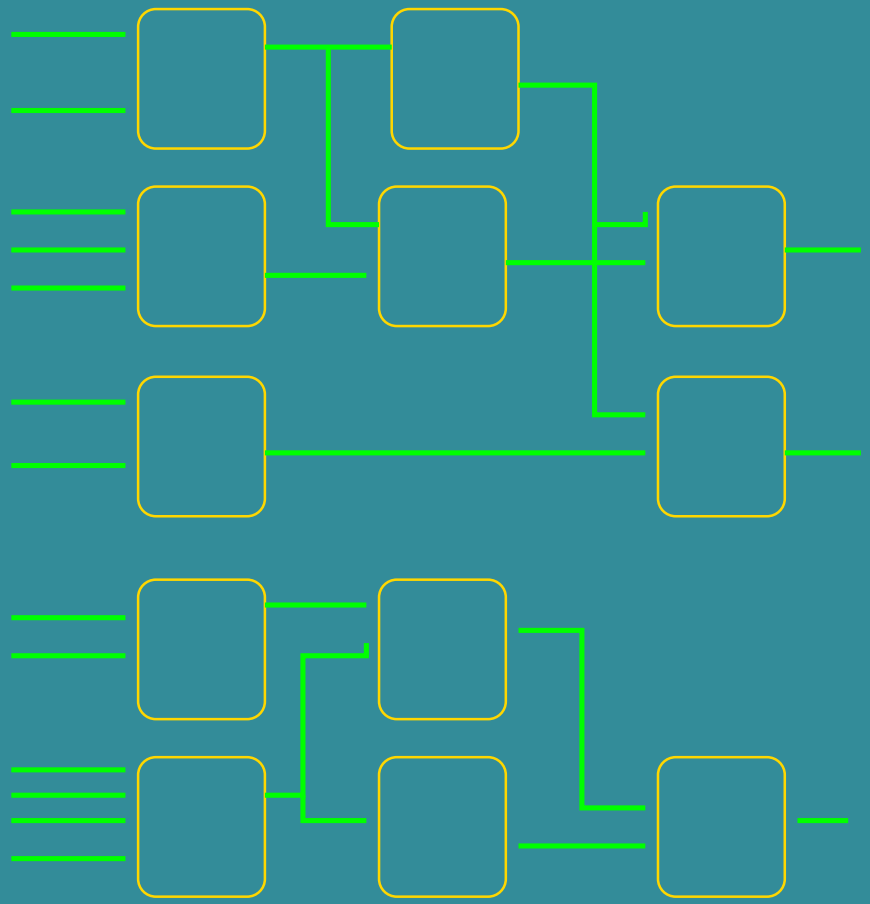
Currents: library database

- Each library cell is simulated in all possible input transition state (implying or not output transition): current is measured
- Current activity types are clustered, coded and a sample is found
- A Look-up-table is generated for each input transition state

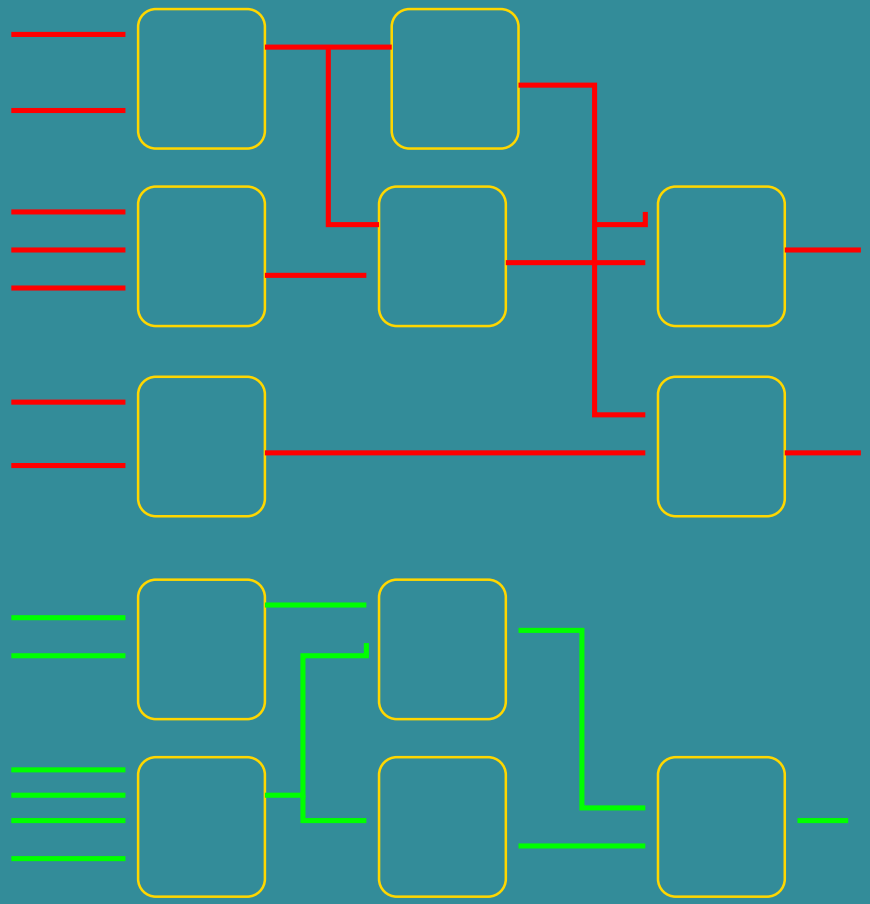
from $V_{in} \rightarrow V_{out}$

to $I_{in} \rightarrow I_{out}$

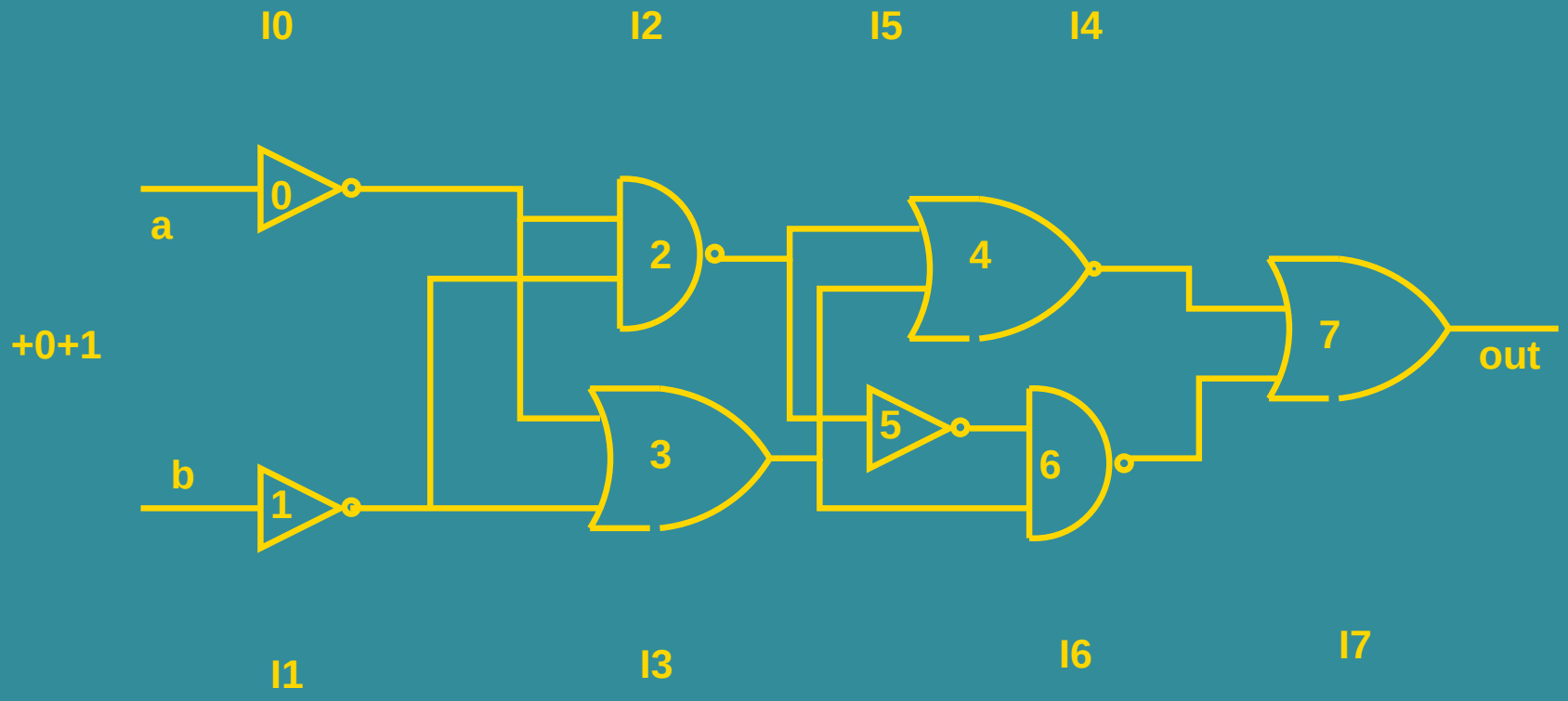
Currents: hierarchical analysis



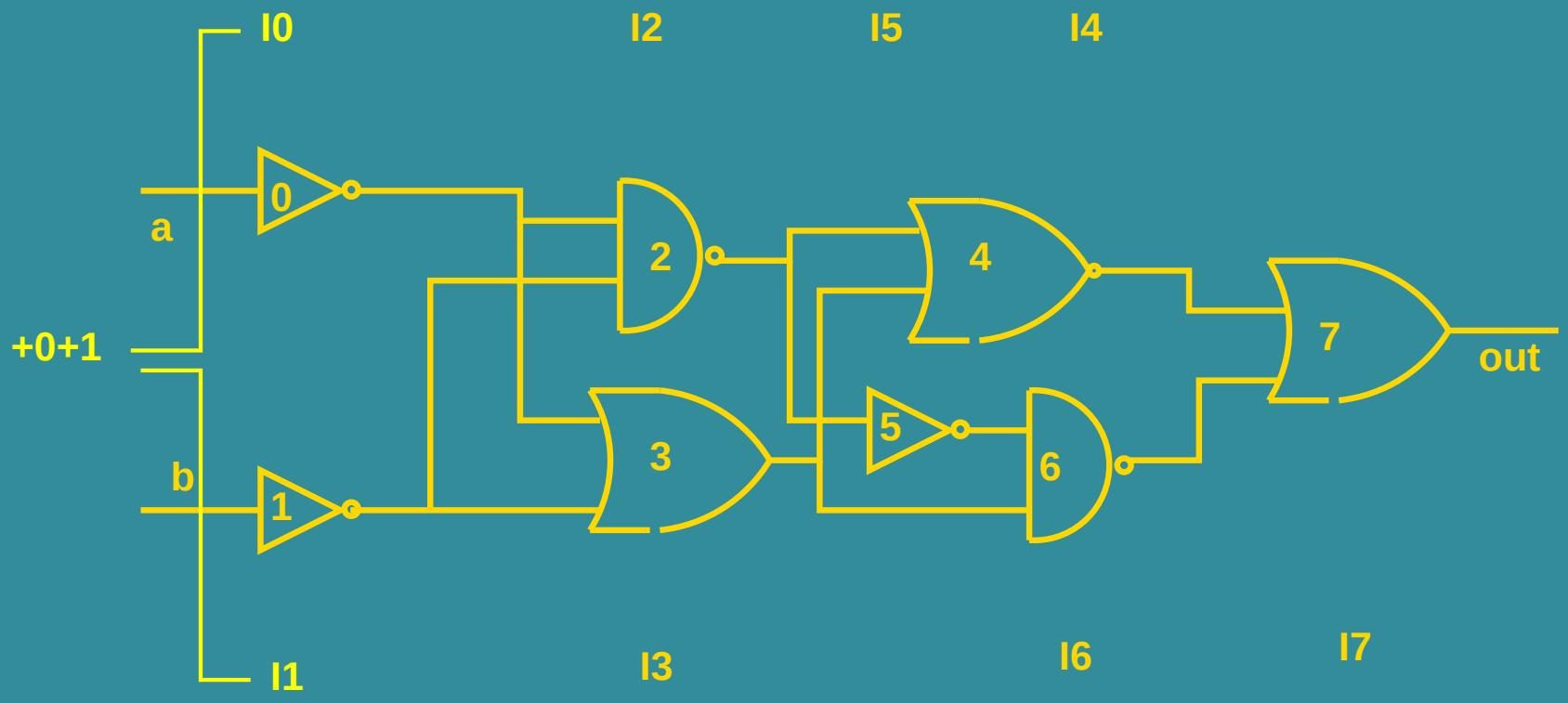
Currents: hierarchical analysis



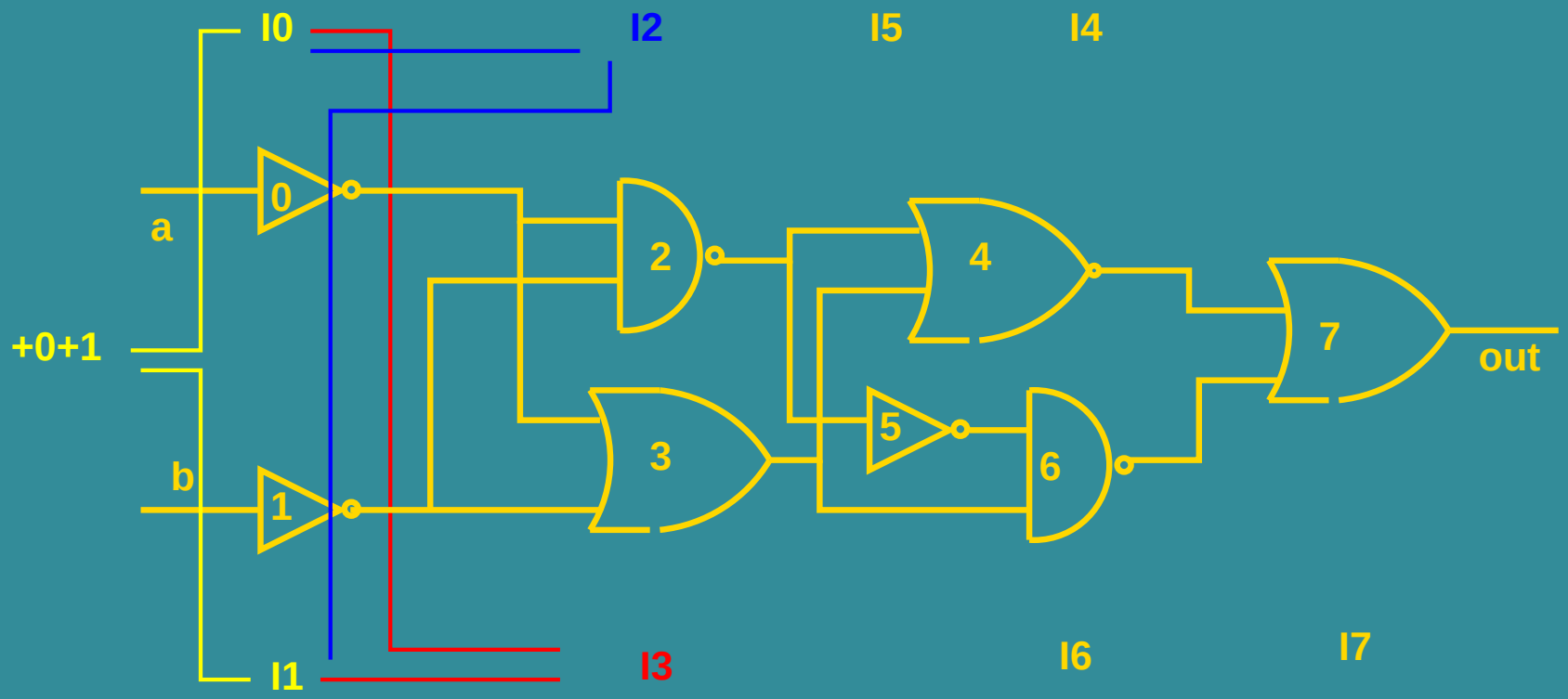
Currents: activity evaluation



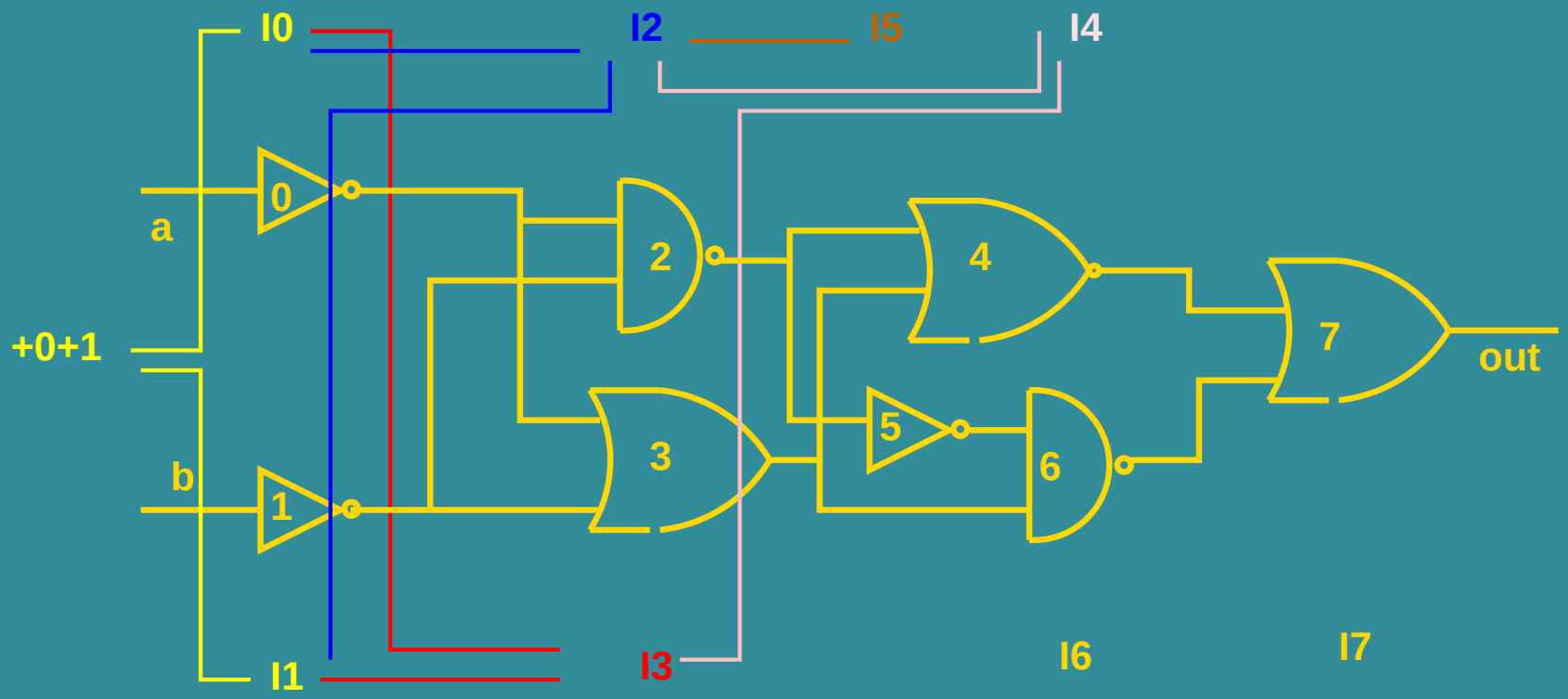
Currents: activity evaluation



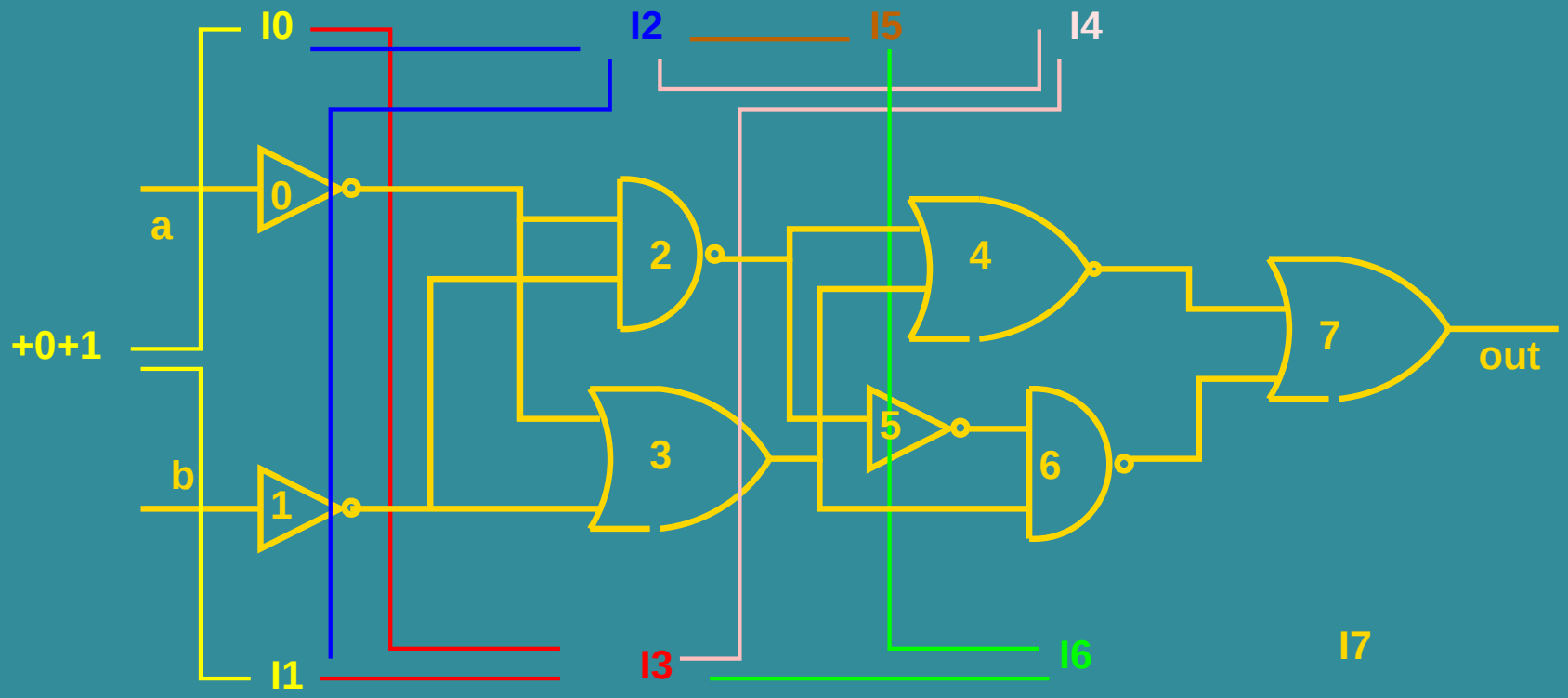
Currents: activity evaluation



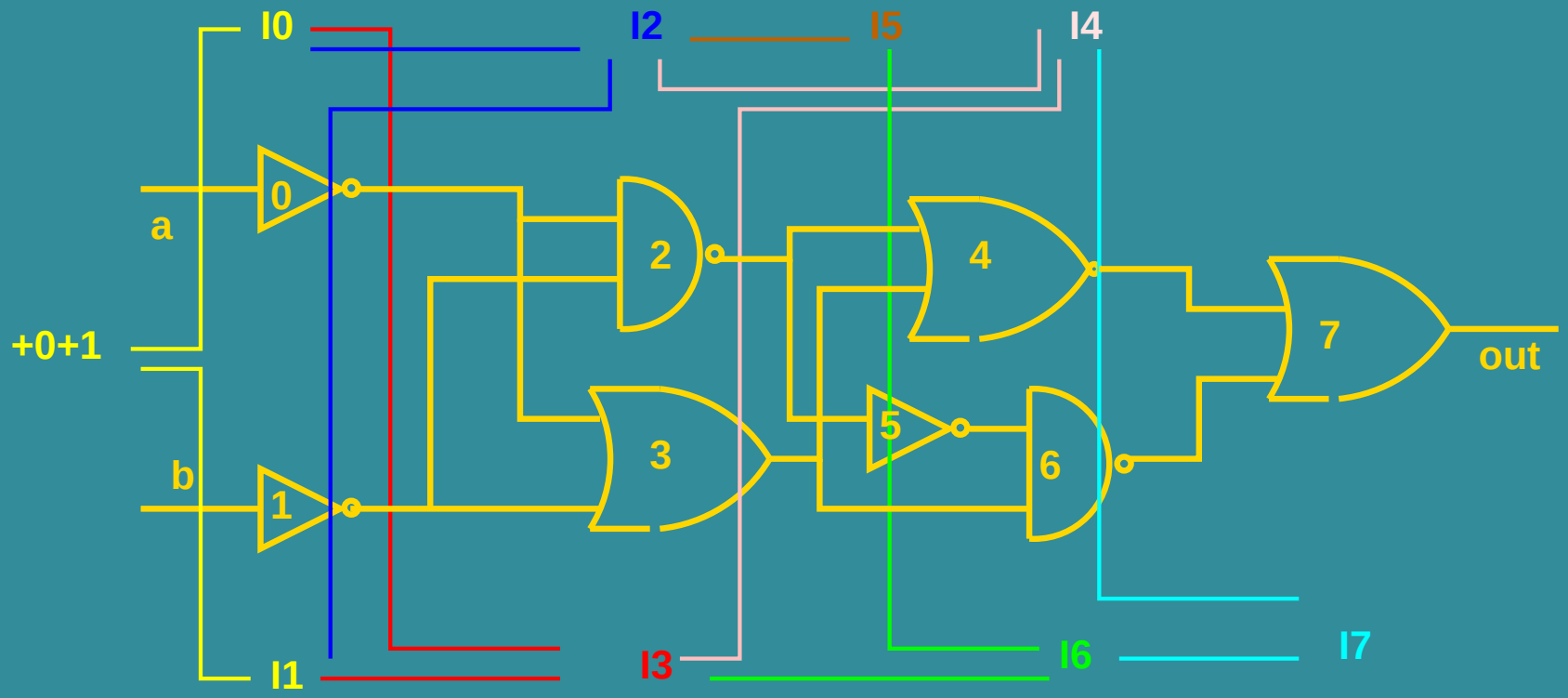
Currents: activity evaluation



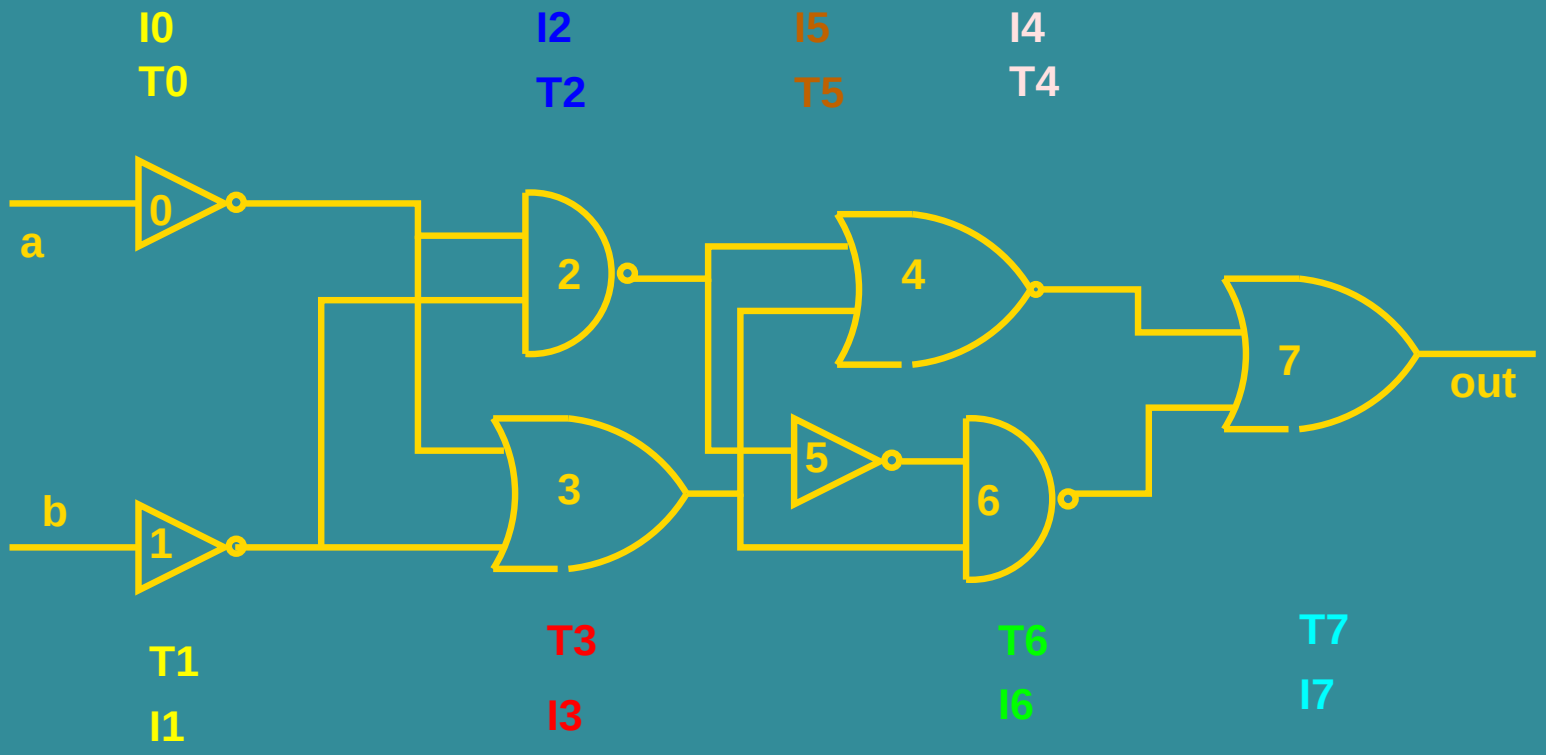
Currents: activity evaluation



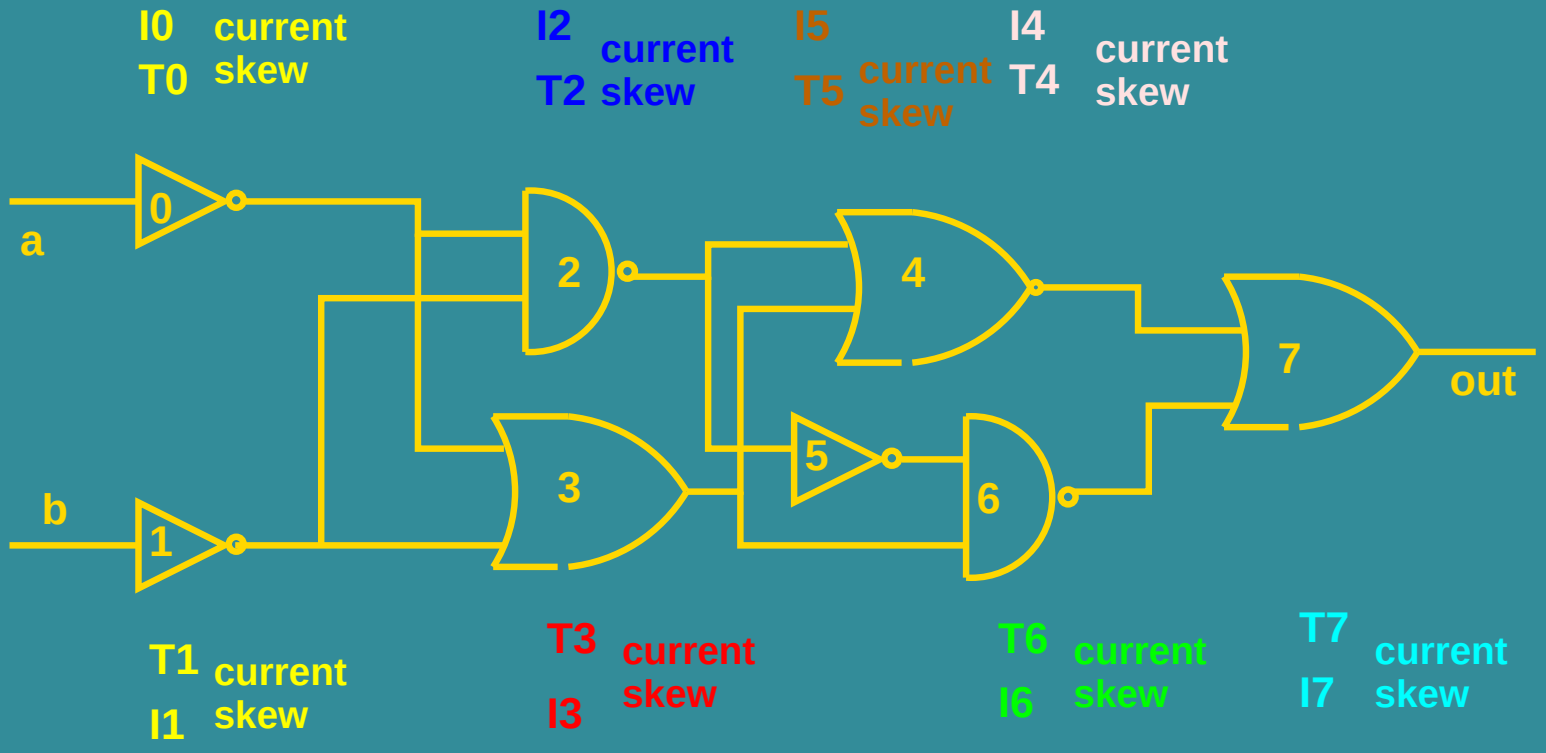
Currents: activity evaluation



Currents: activity evaluation

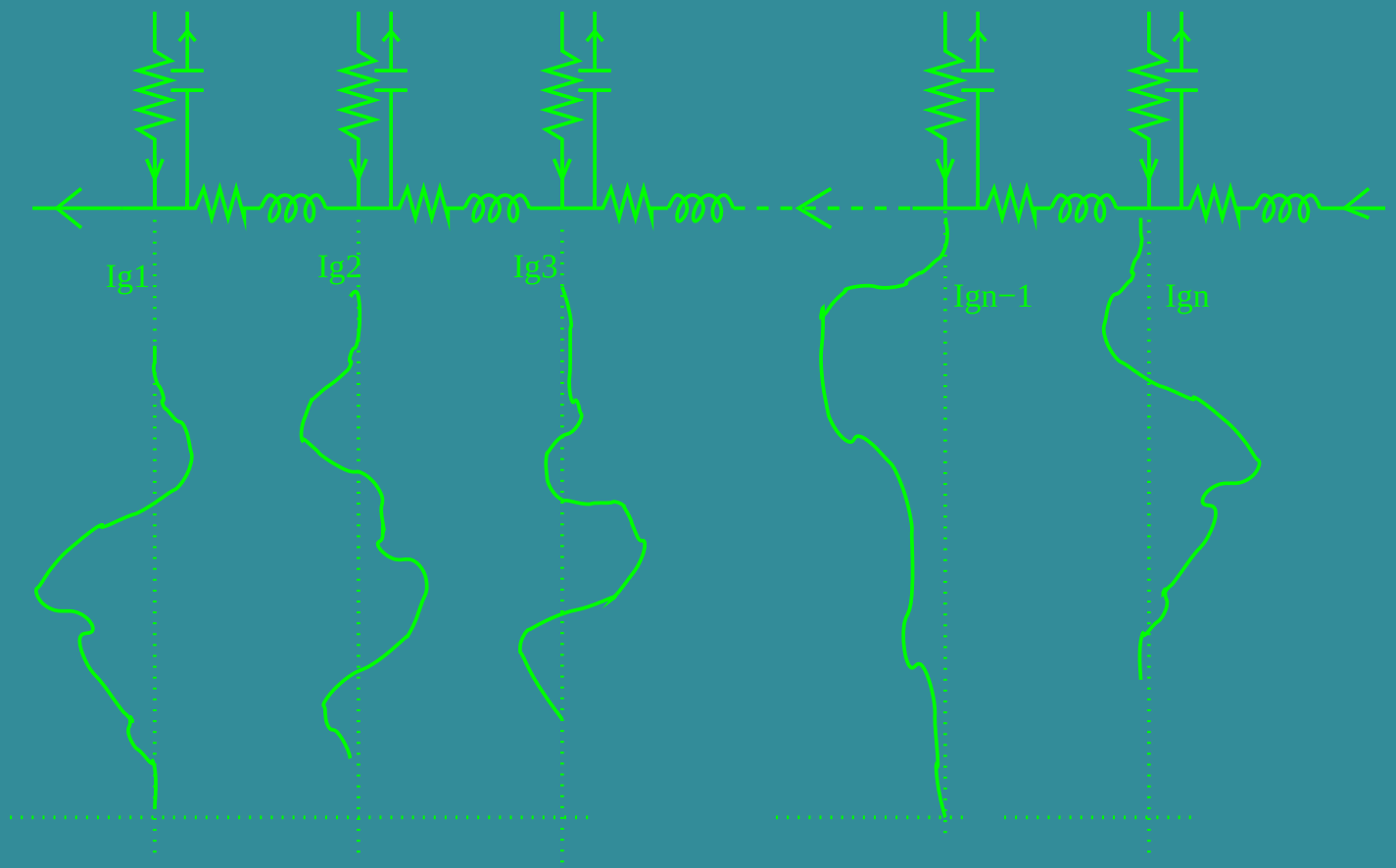


Currents: activity evaluation



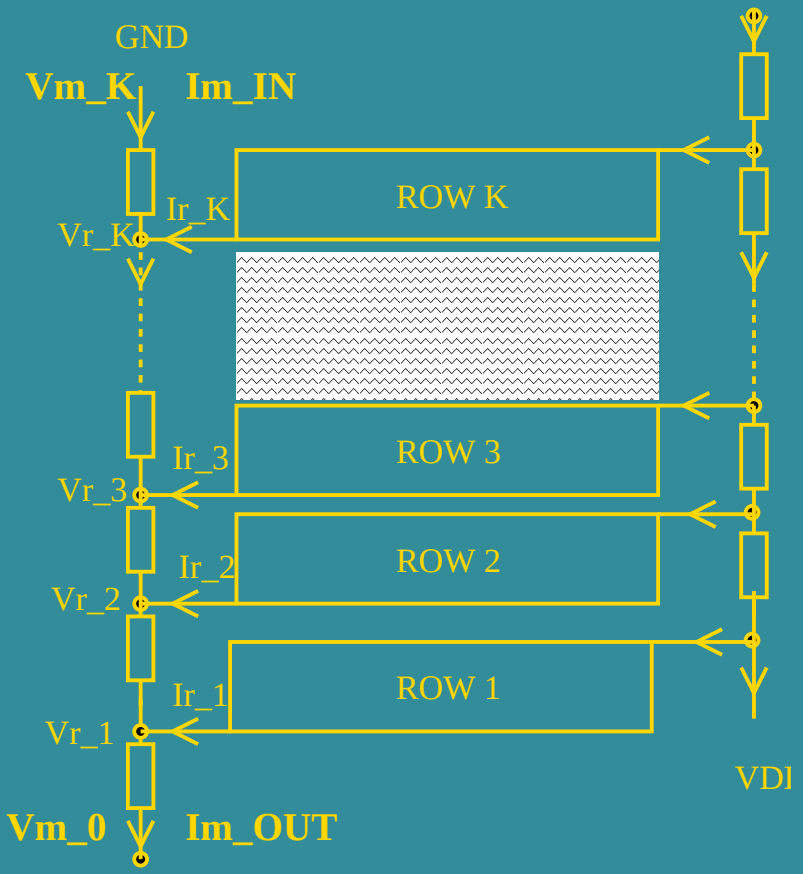
Proposed method

Power grid: ROW



Row r, N gates

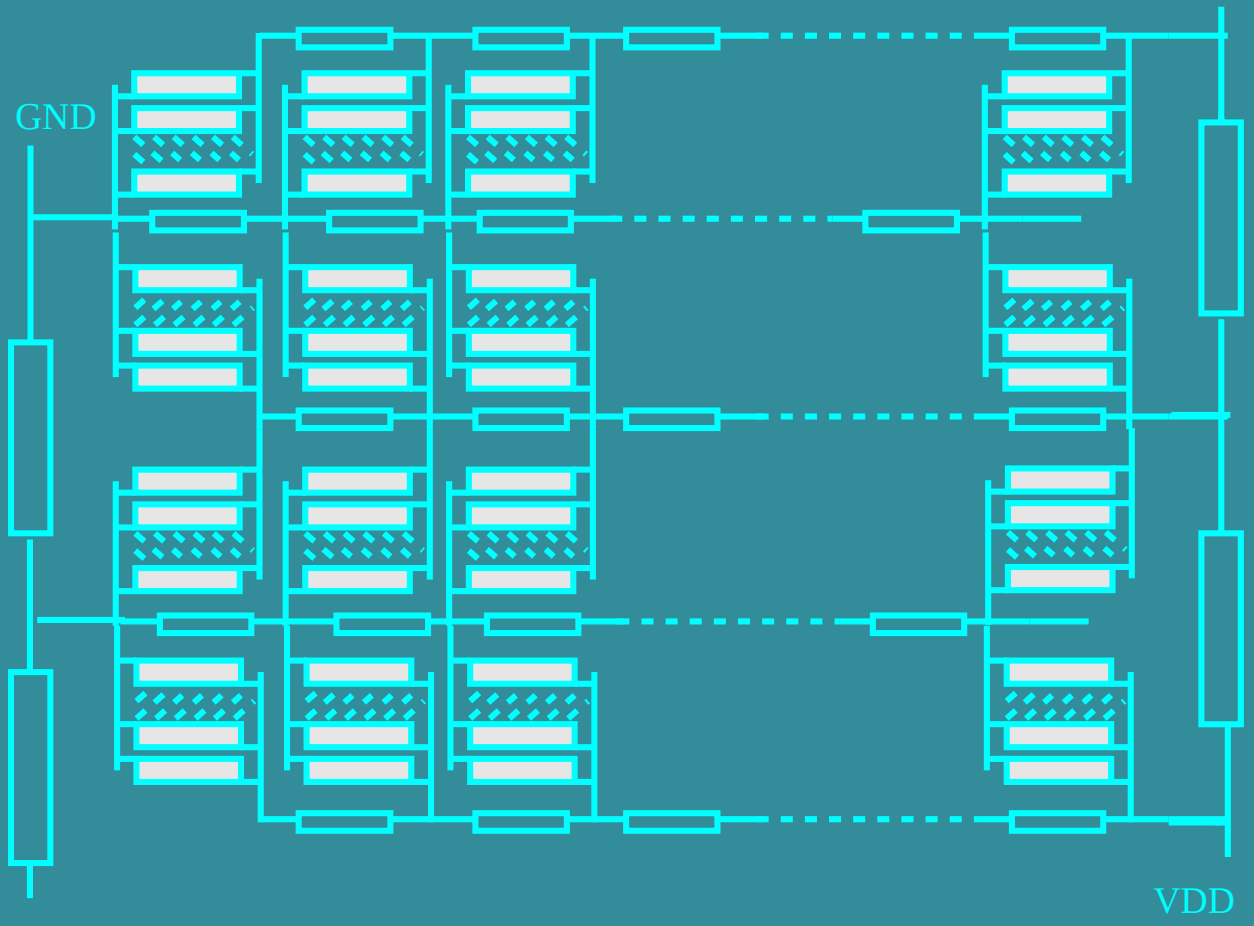
Power grid: MACRO



Macro m, K rows

Proposed method

Power grid: BLOCK



Block b, M macros

Power grid: ROW

$$V_{rN} = V_{r0} + N\mathbb{R}_r I_{rIN}$$

$$+N\mathbb{L}_r \frac{d}{dt} I_{rIN} + \mathbb{R}_r \sum_{i=1}^{N} \left(i\left(I_{gi} - I_{ci}\right)\right)$$

$$+\mathbb{L}_r \sum_{i=1}^{N} \left(i\frac{d}{dt}\left(I_{gi} - I_{ci}\right)\right)$$

Power grid: MACRO

$$V_{kK} = V_{k0} + K\mathbb{R}_k I_{kIN}$$

$$+K\mathbb{L}_k \frac{d}{dt} I_{kIN} + \mathbb{R}_k \sum_{i=1}^{K} \left(i\left(I_{gi} - I_{ci}\right) \right)$$

$$+\mathbb{L}_k \sum_{i=1}^{K} \left(i \frac{d}{dt} \left(I_{gi} - I_{ci}\right) \right)$$

Power grid: BLOCK

$$V_{mM} = V_{m0} + M\mathbb{R}_m I_{mIN}$$

$$+M\mathbb{L}_m \frac{d}{dt} I_{mIN} + \mathbb{R}_m \sum_{i=1}^{M} \left(i\left(I_{gi} - I_{ci}\right)\right)$$

$$+\mathbb{L}_m \sum_{i=1}^{M} \left(i\frac{d}{dt}\left(I_{gi} - I_{ci}\right)\right)$$

Methodology results and conclusions

- Results for non automated evaluations on a two macros block with 25 gates each showed with respect to HSPICE simulations
  - accuracy in current waveform evaluation of 98%
  - accuracy in worst power supply noise evaluation of 85% due to parasitic modeling
- Needs final implementation for managing complex circuits and benchmarks
- Need further improvements in parasitic modeling
- Expected good results in terms of accuracy and efficiency