Getting more out of Donath's hierarchical model for interconnect prediction

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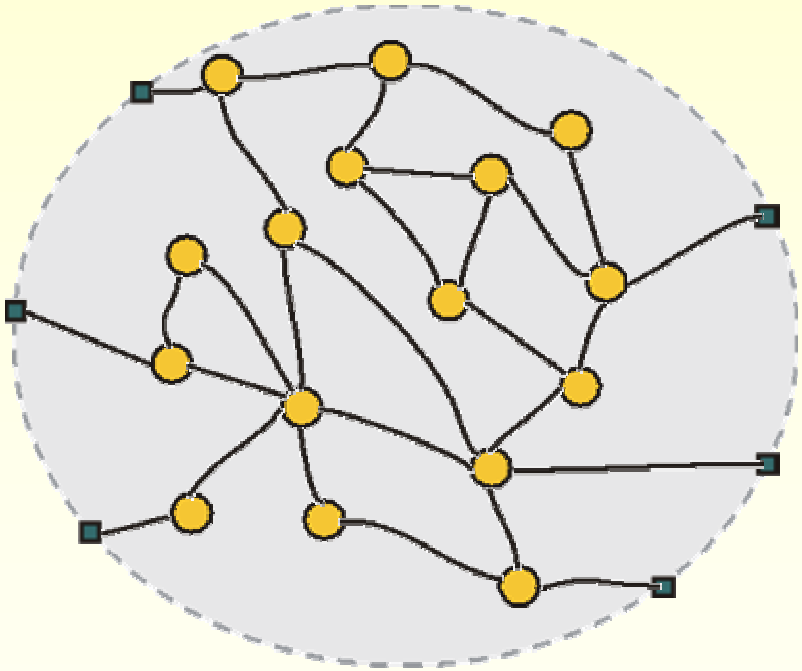
Presentation outline

- Introduction: Donath's technique
- The gap towards modeling real circuit placements
- Closing (part of) the gap
  - Placement based on bipartitioning
  - From Rent's rule to the Rent characteristic
  - Relaxing layout medium size and circuit size
  - Impact of rectangular layout grids and cell shapes
- Conclusions

Donath's placement model: circuit model



Circuit netlist,

consists of:

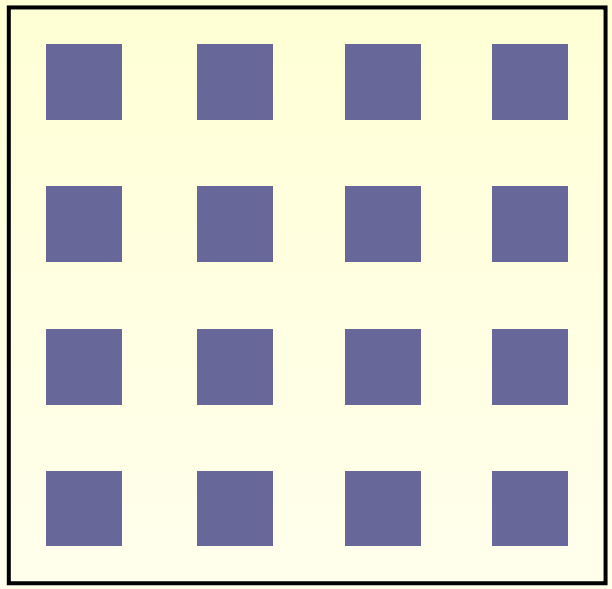
- 4^K gates
- Connections between gates (internal nets)
- Connections to circuit's exterior (external nets)

Only two-terminal connections considered !

Donath's placement model: architecture model

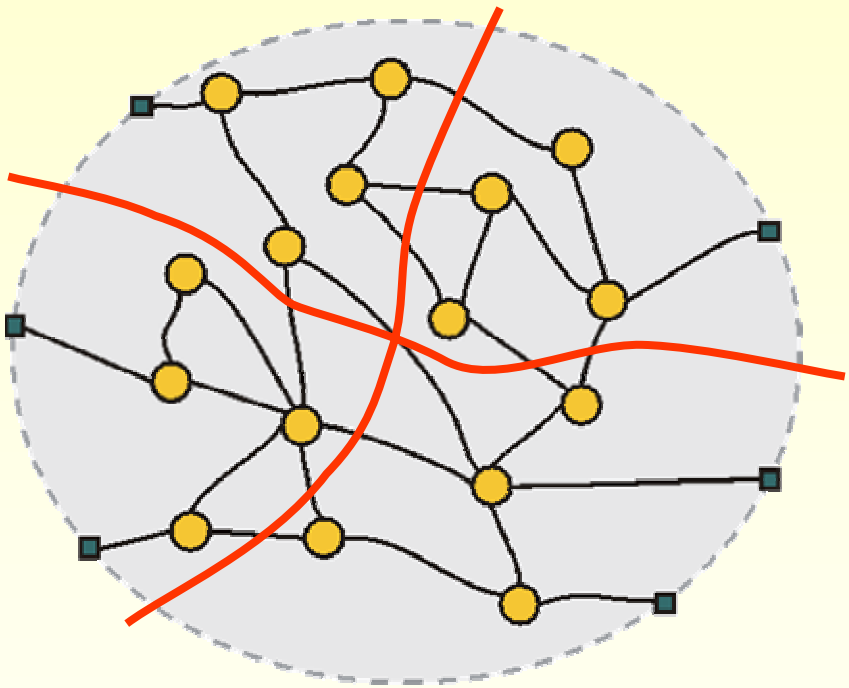
Architecture consists of:

- square grid of $2^K \times 2^K$ possible gate locations
- Manhattan distance metric: length = x-distance + y-distance
- with equal unit distances in both directions

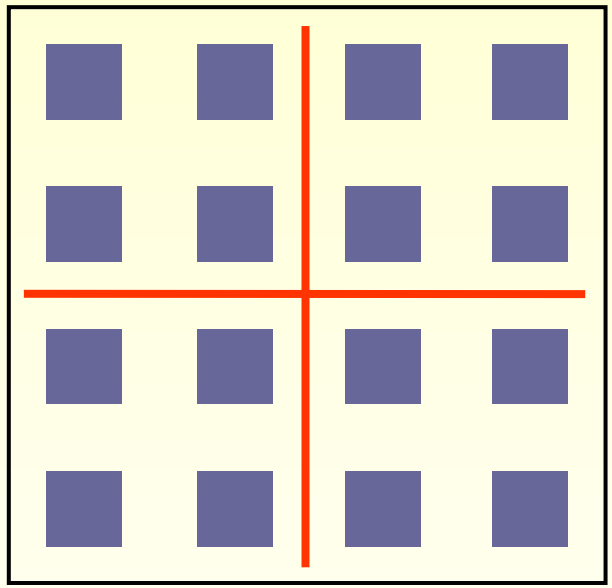


Donath's placement model

Perform 4-way partitioning of circuit and architecture

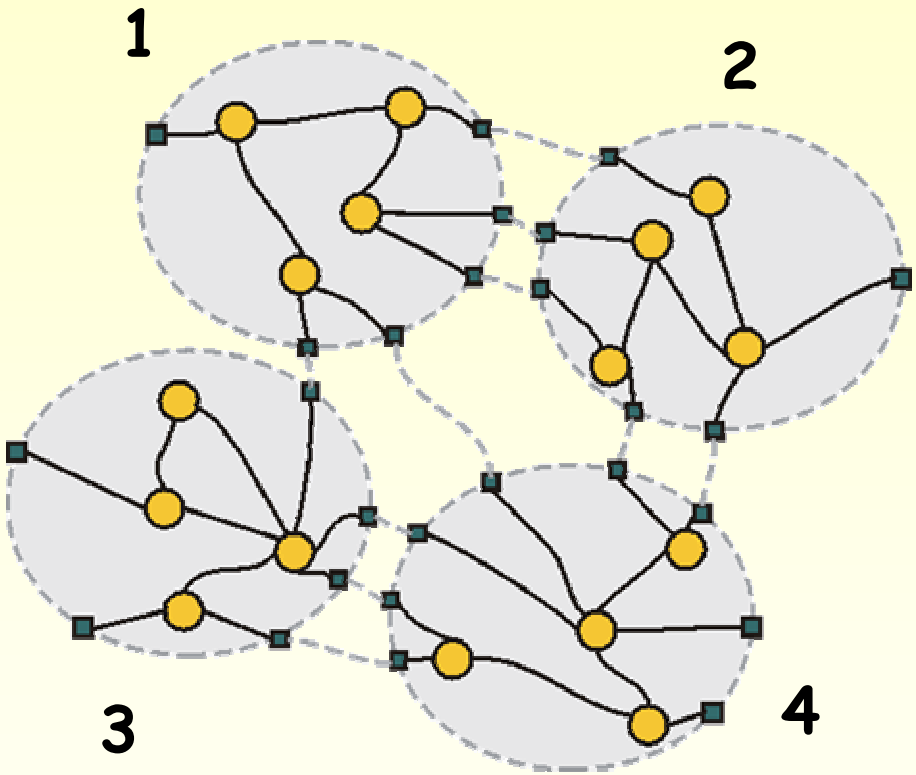


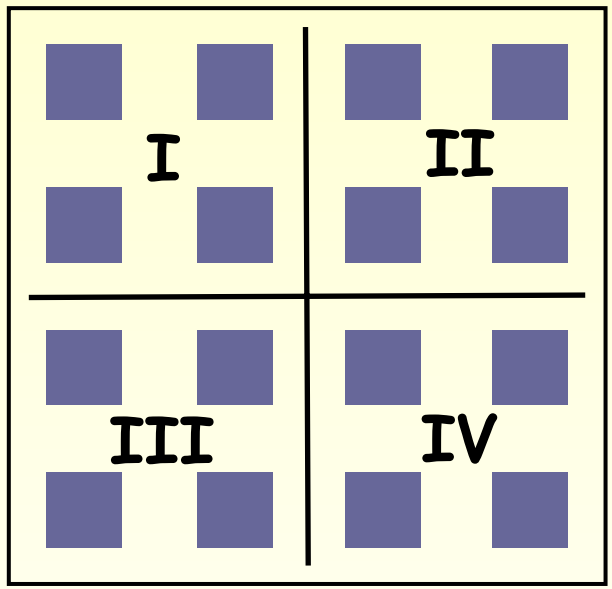
circuit



architecture

Donath's placement model

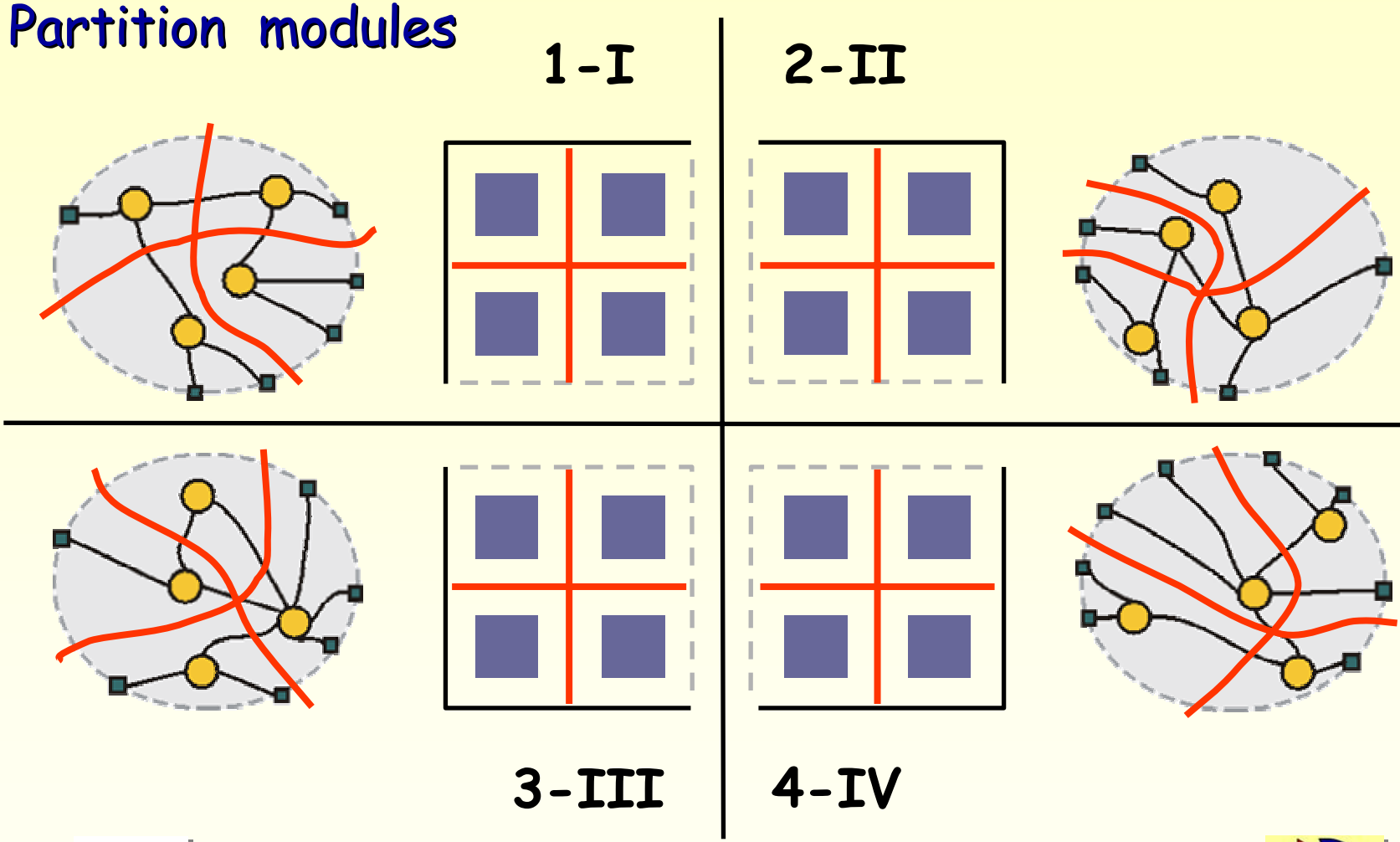




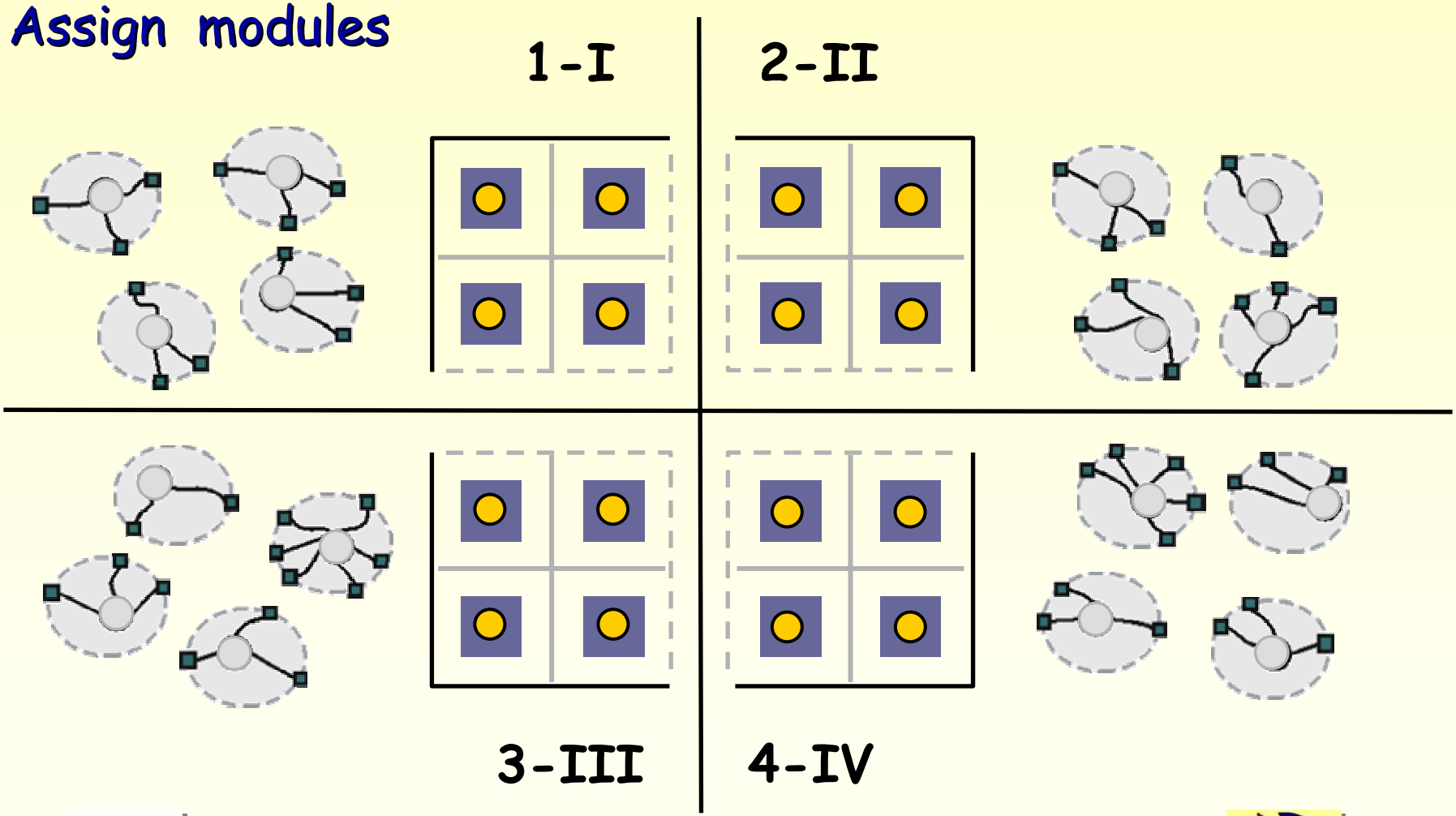
Randomly assign circuit modules to architecture modules

Donath's placement model

Partition modules

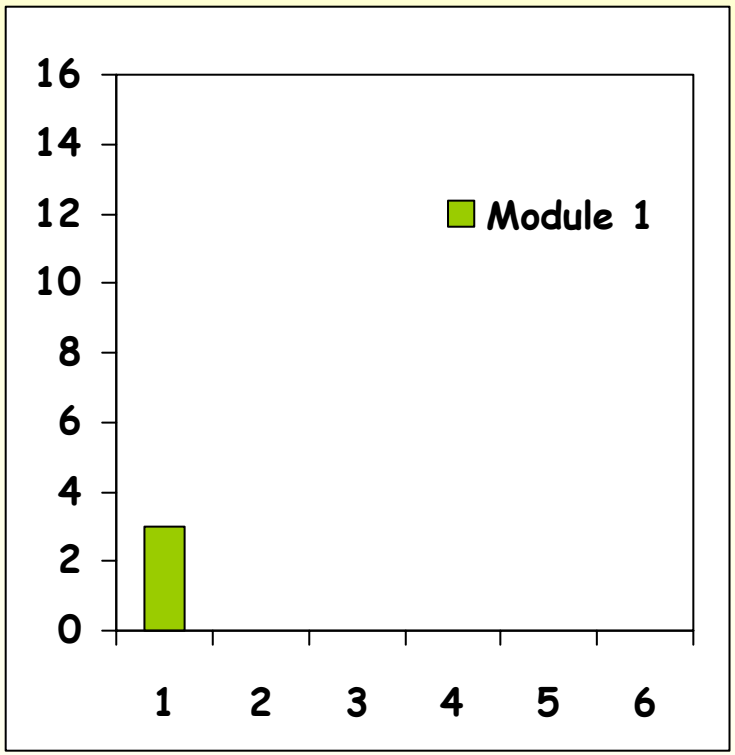


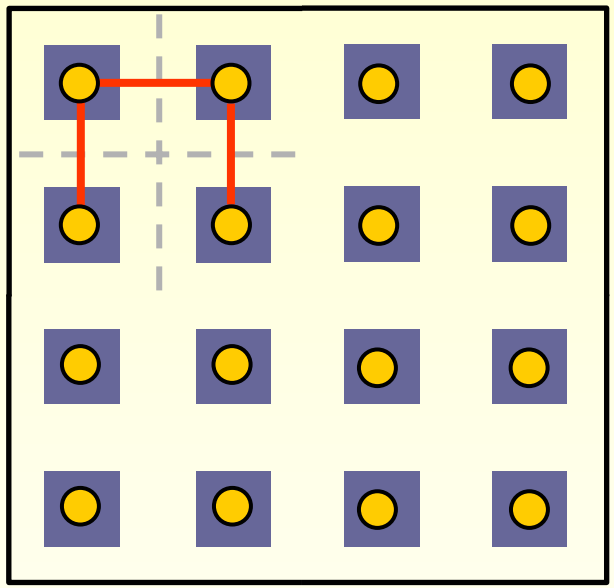
Donath's placement model



Donath's placement model

Count number of nets of each length (for every partitioned module) :





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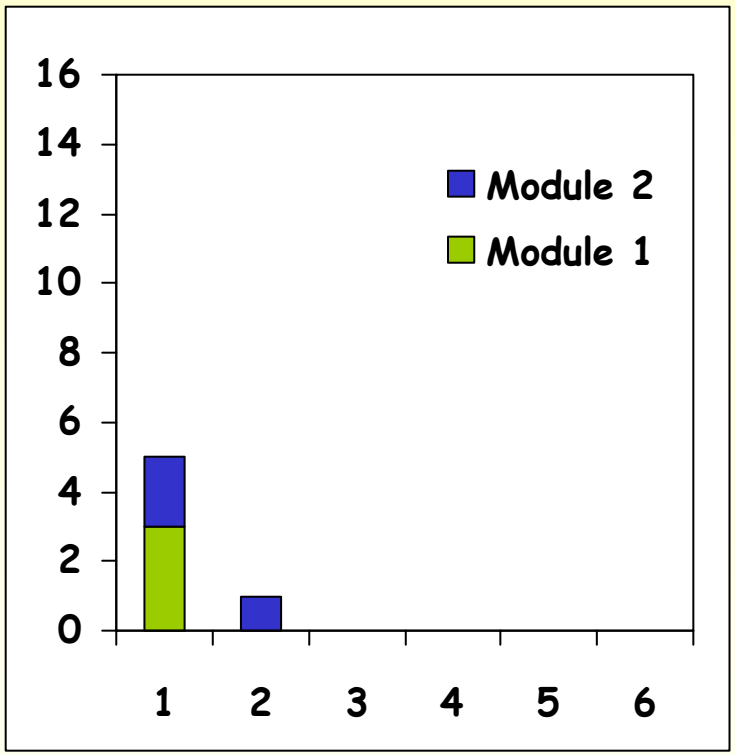

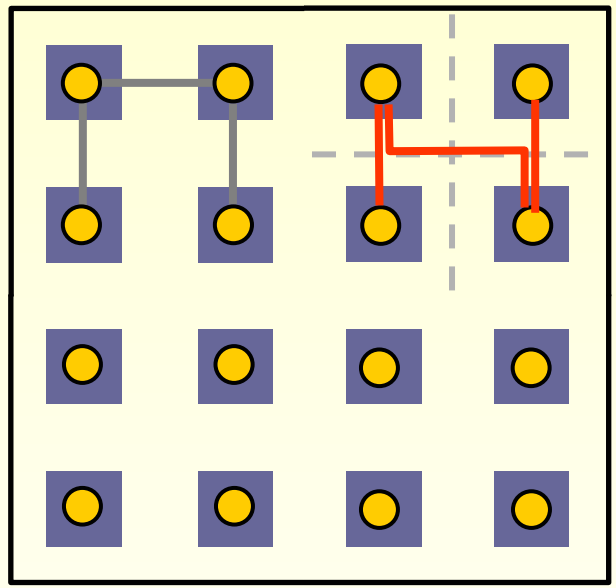

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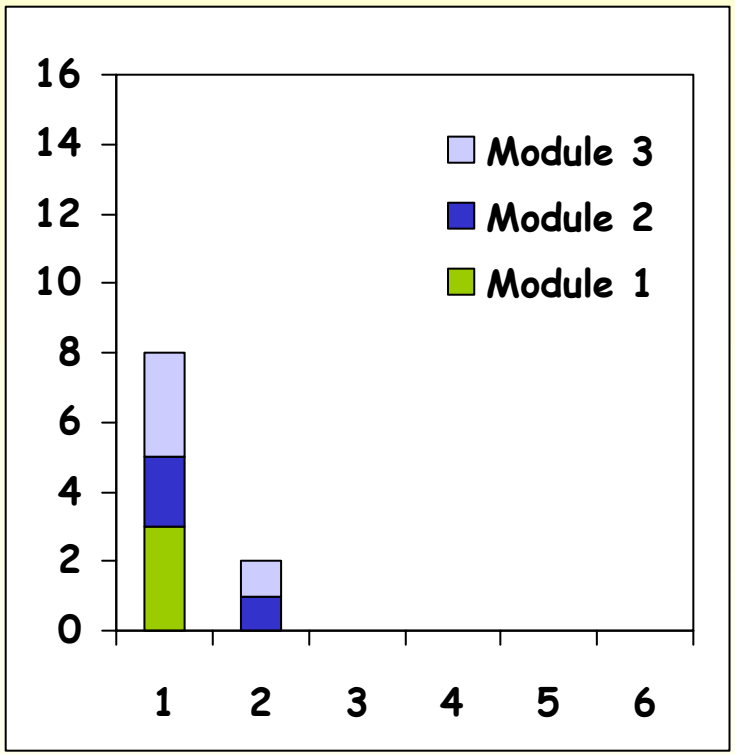

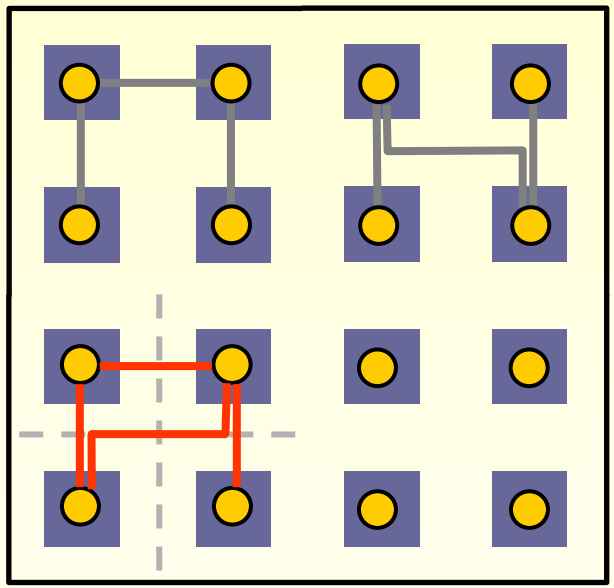

Donath's placement model

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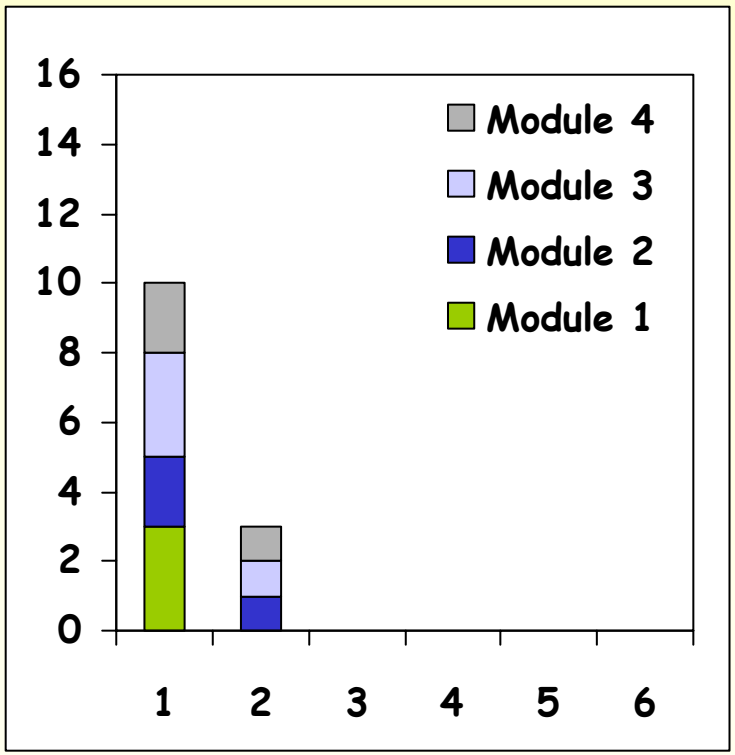

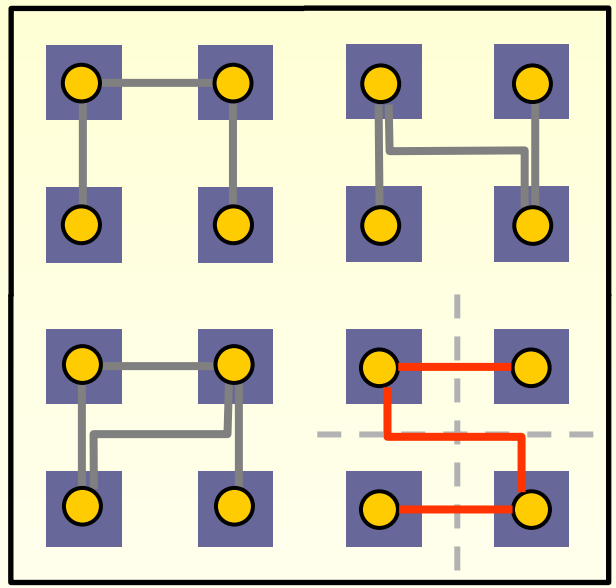

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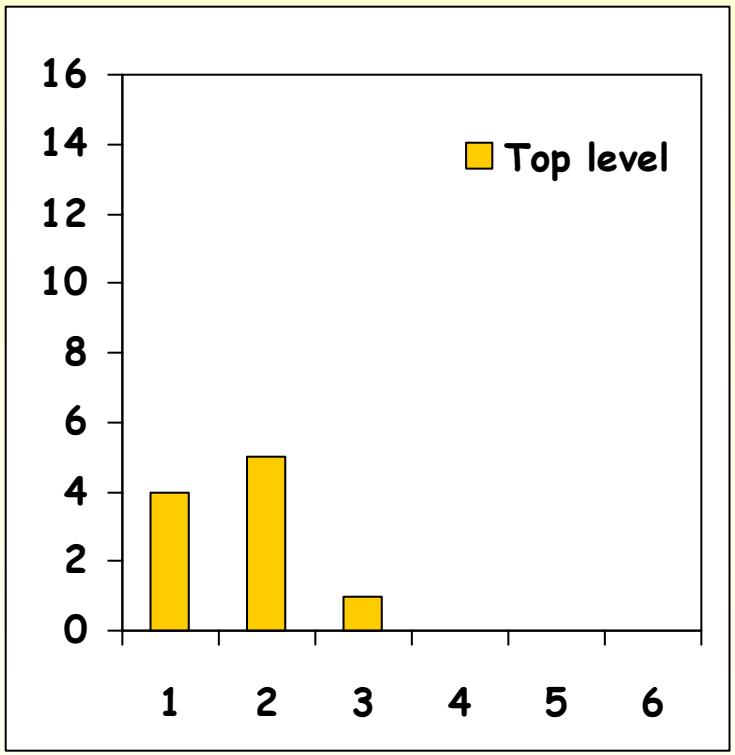

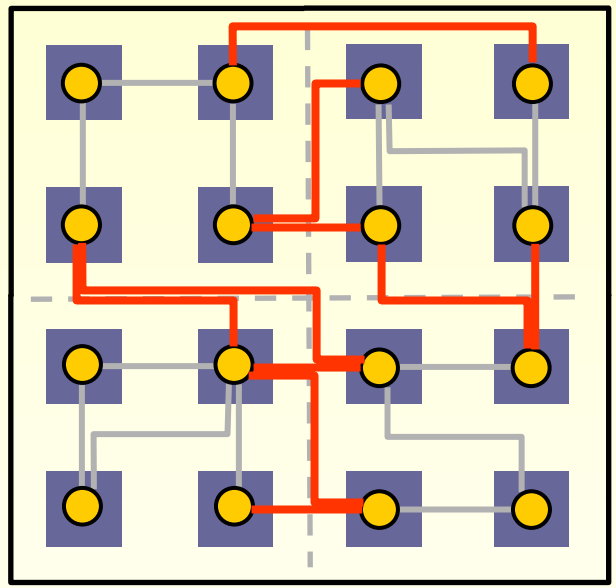

Donath's placement model

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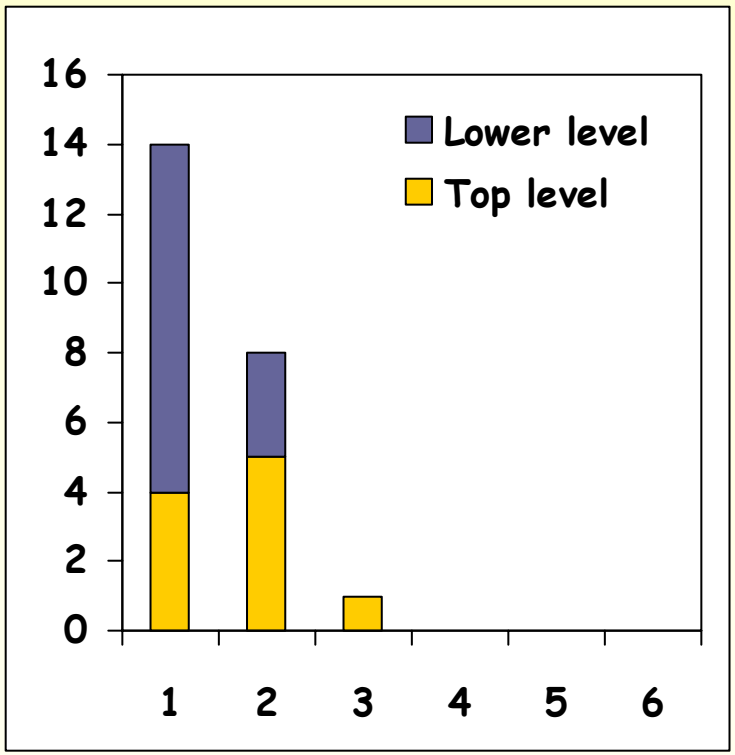
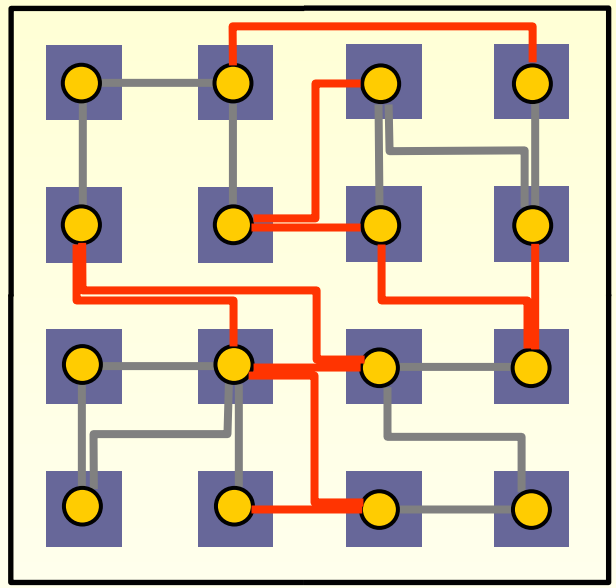




Only lengths of internal wires

Only minimal routing distance

Donath's wirelength distribution estimation technique

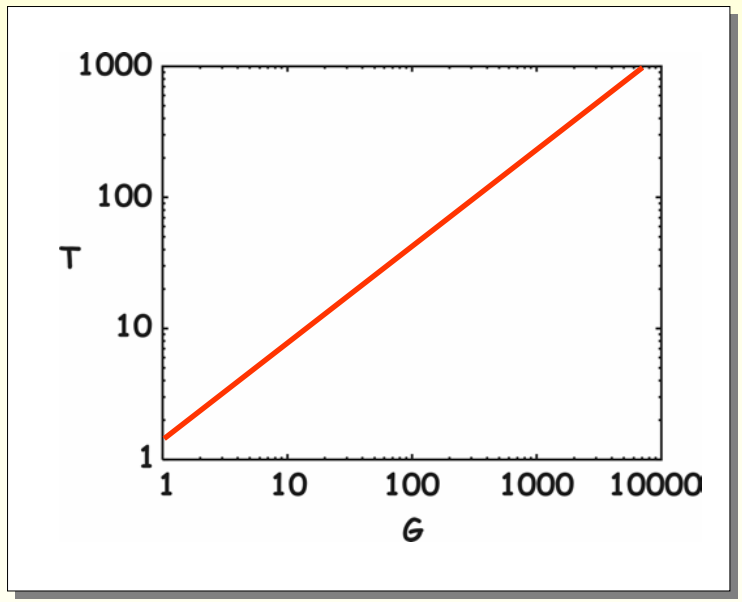
Number of nets that is cut at each level derived from Rent's rule:

$$T = tG^p$$

p: Rent exponent

t: Rent coefficient

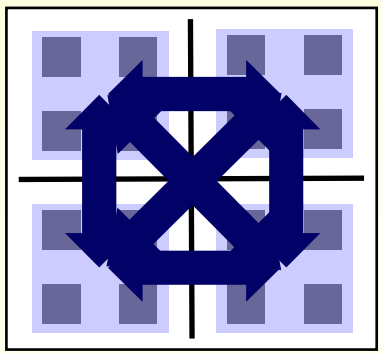
- **Empirical formula**
- Relates the **average** number of terminals T coming out of a circuit module to the **average** number of gates G in that module



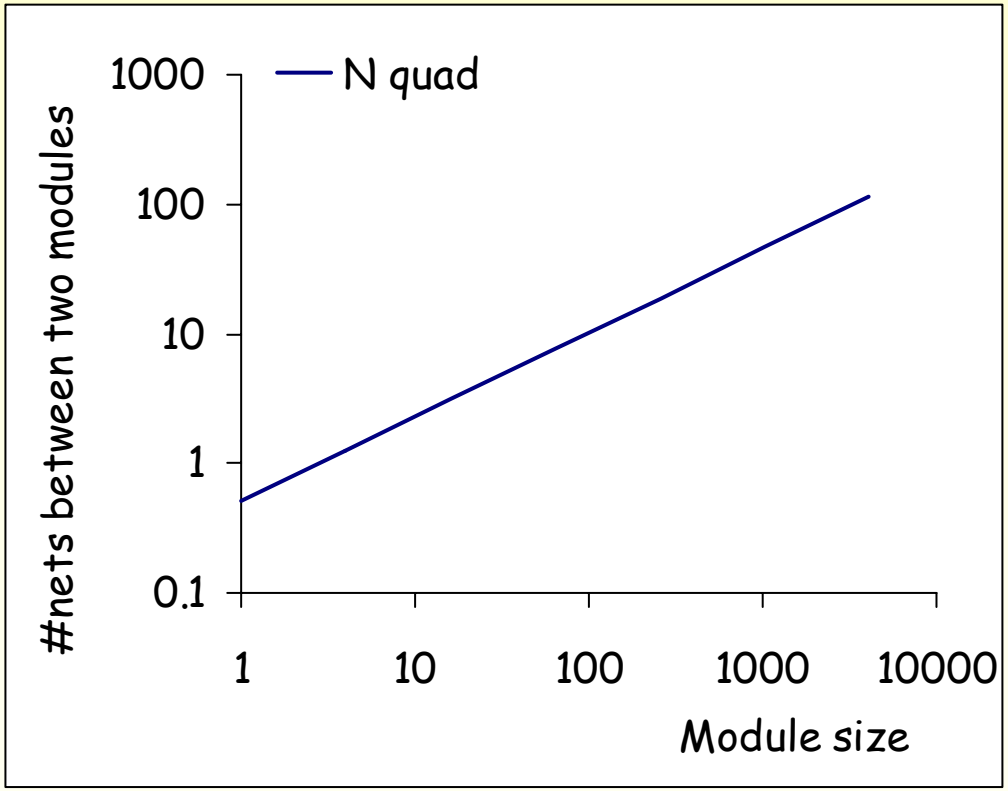
Donath's wirelength distribution estimation technique

Number of nets connecting each module pair (p=0.65, t=4) :

$$N_{quad} = \frac{t4^k}{6}\left(2 - 2^{2p-1}\right)$$



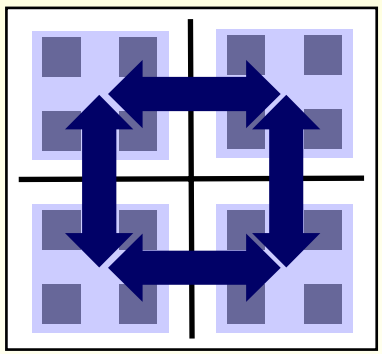
Equal for all module pairs !

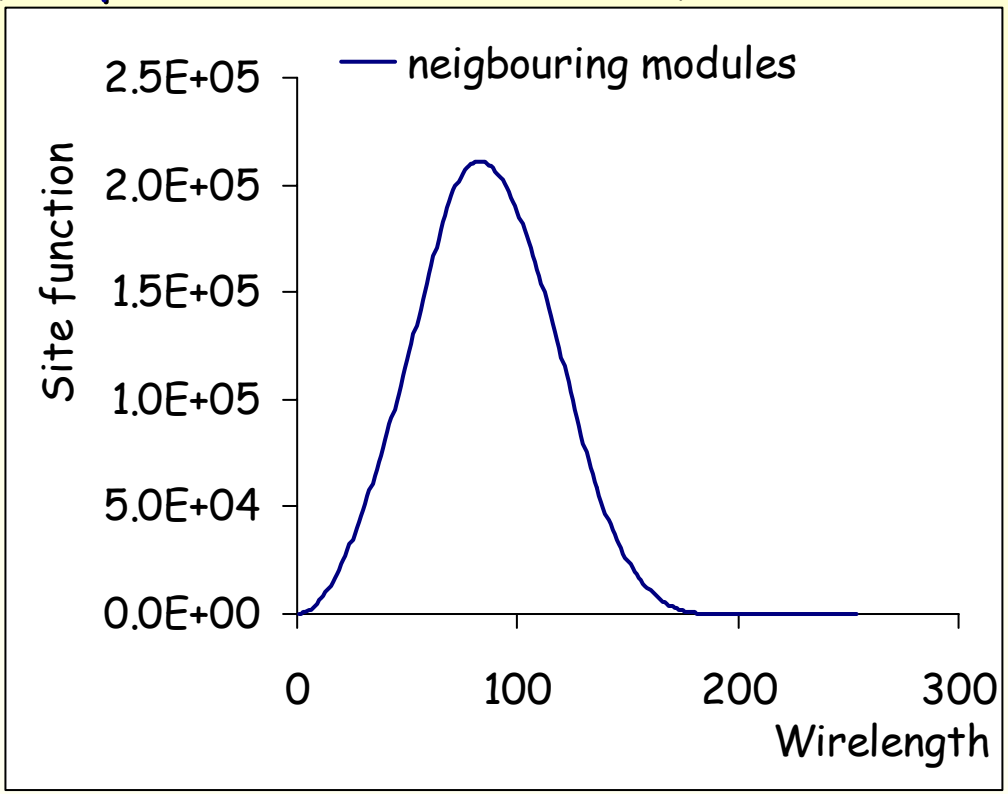


Donath's wirelength distribution estimation technique

Length distribution of nets connecting each module pair : random terminal positions (sampled from site function)

Neighbouring modules (64 x 64)

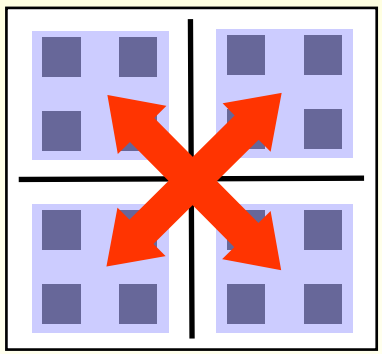


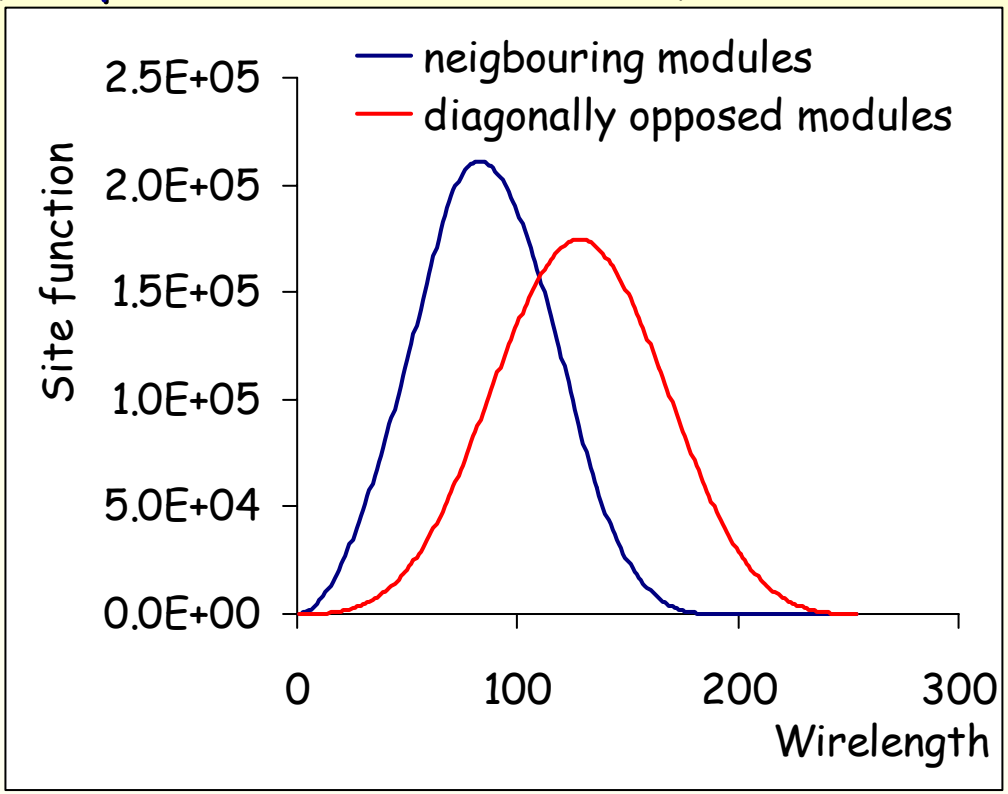


Donath's wirelength distribution estimation technique

Length distribution of nets connecting each module pair : random terminal positions (sampled from site function)

Diagonally opposed modules (64 x 64)



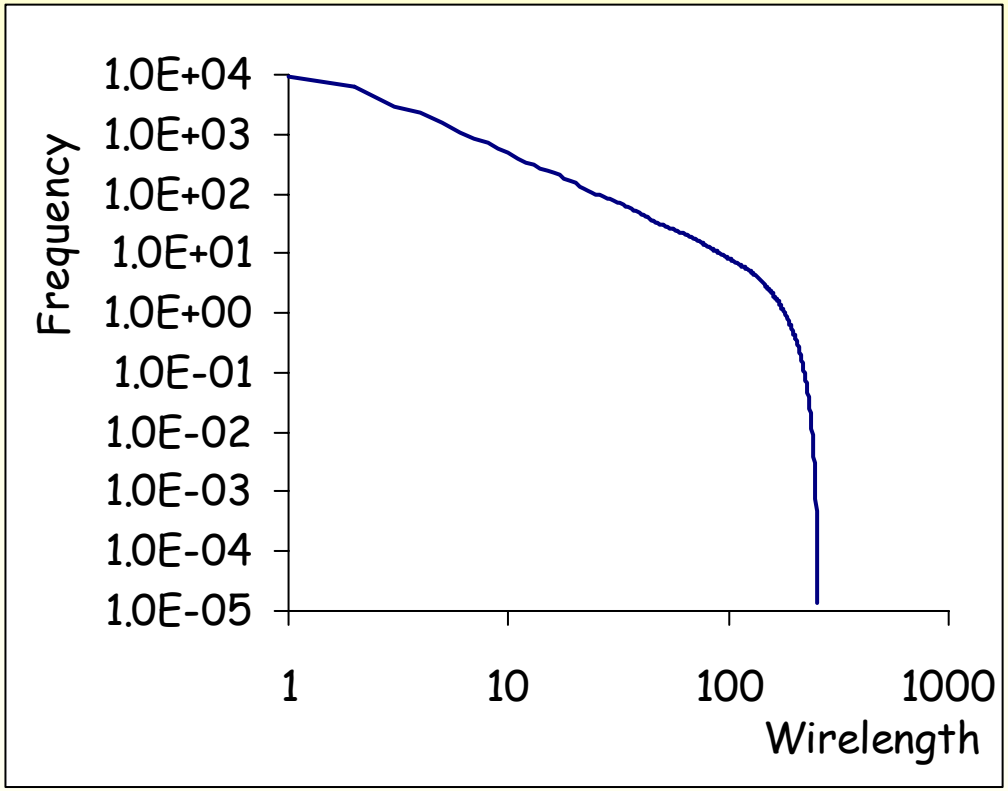


Donath's wirelength distribution estimation technique

Total wirelength distribution for:

- circuit of 16384 gates
- p = 0.65
- t = 4

Can be calculated analytically !



Underlying assumptions in Donath's model

1. Rent's rule applies for all module sizes
2. Number of gates $=4^K$ and equals architecture grid size
3. Architecture is square grid with square cells
4. Placement based on hierarchical 4-way partitioning
5. Only optimization during placement: minimization of number of nets cut during partitioning

Evaluation of Donath's placement model

All assumptions matched:

1. Synthetic benchmark circuits (`gnl`) with 4^7=16384 gates that follow Rent's rule almost exactly
2. Mapped onto square grid architecture with 4^7 square cells by Donath's placement procedure

High variance due to random module assignment: statistical average taken over 500 placement runs

Evaluation of Donath's placement model

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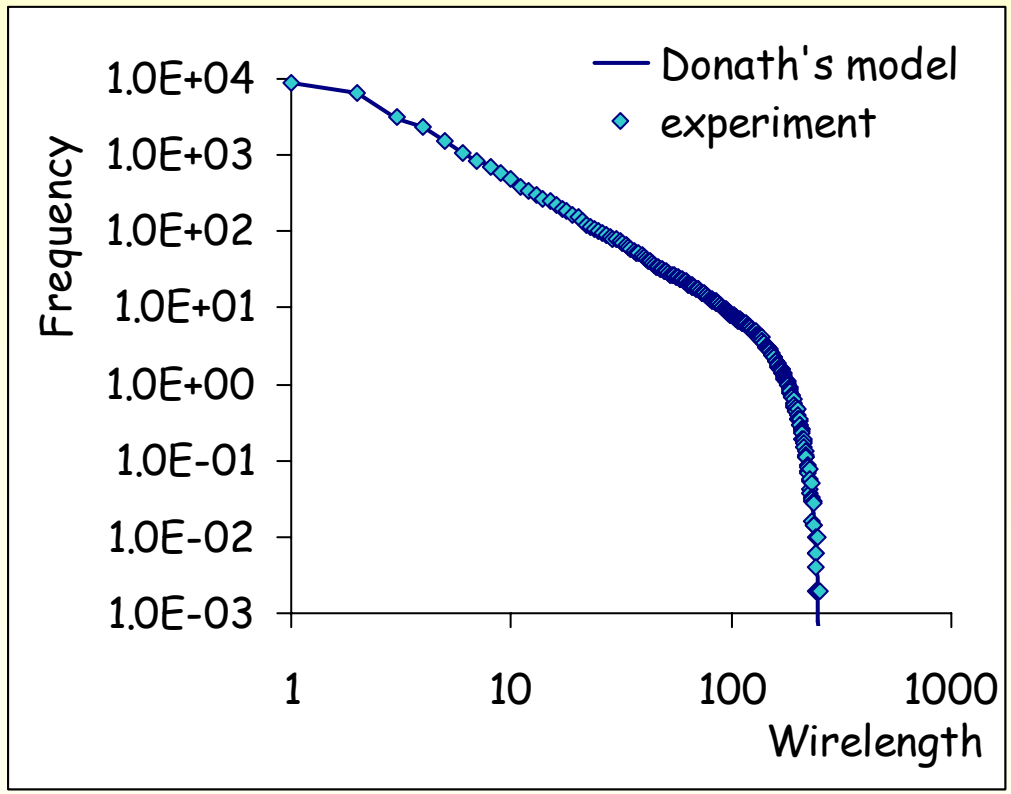
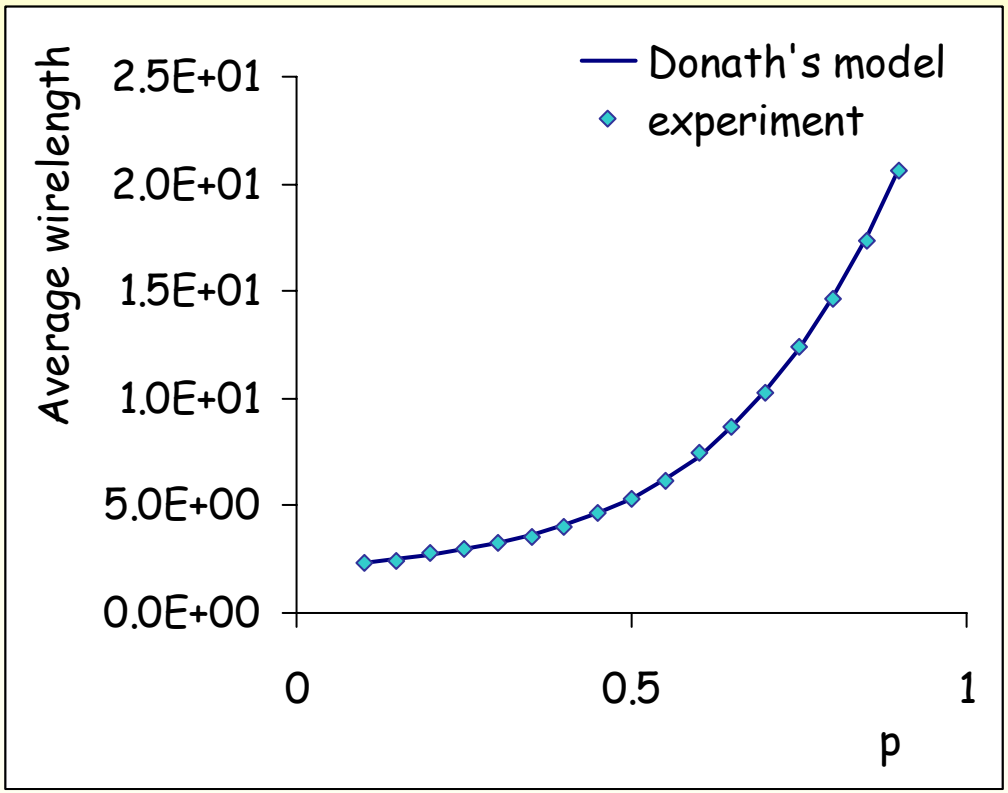


Evaluation of Donath's placement model

Average wirelength for:

- circuits of 16384 gates
- p from 0.1 -> 0.9
- t = 4
- 500 placement runs



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- Introduction: Donath's technique
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  - Impact of rectangular layout grids and cell shapes
- Conclusions

Difference with real circuit placements

Donath's method	Real placements
Rent's rule	
Gates = 4^K = grid size	
Square grid with square cells	
4-way partitioning based placement	
No optimization	

Difference with real circuit placements

Donath's method	Real placements
Rent's rule	Deviations: Rent characteristic
Gates = 4^K = grid size	
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Difference with real circuit placements

Donath's method	Real placements
Rent's rule	Deviations: Rent characteristic
Gates = 4^K = grid size	Gates != 4^K != grid size
Square grid with square cells	
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Difference with real circuit placements

Donath's method	Real placements
Rent's rule	Deviations: Rent characteristic
Gates = 4^K = grid size	Gates != 4^K != grid size
Square grid with square cells	Possibly rectangular grid and/or rectangular cells
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No optimization	

Difference with real circuit placements

Donath's method	Real placements
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Gates = 4^K = grid size	Gates != 4^K != grid size
Square grid with square cells	Possibly rectangular grid and/or rectangular cells
4-way partitioning based placement	Often bipartitioning based placement
No optimization	

Difference with real circuit placements

Addressed in this paper

Donath's method	Real placements
Rent's rule	Deviations: Rent characteristic
Gates = 4^K = grid size	Gates != 4^K != grid size
Square grid with square cells	Possibly rectangular grid and/or rectangular cells
4-way partitioning based placement	Often bipartitioning based placement
No optimization	Lots of optimization

Addressed by other authors

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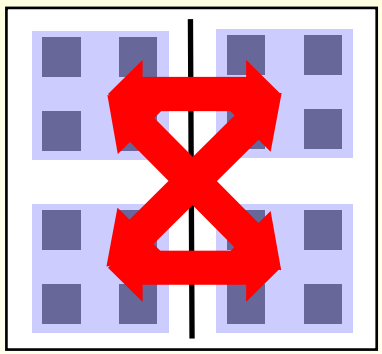
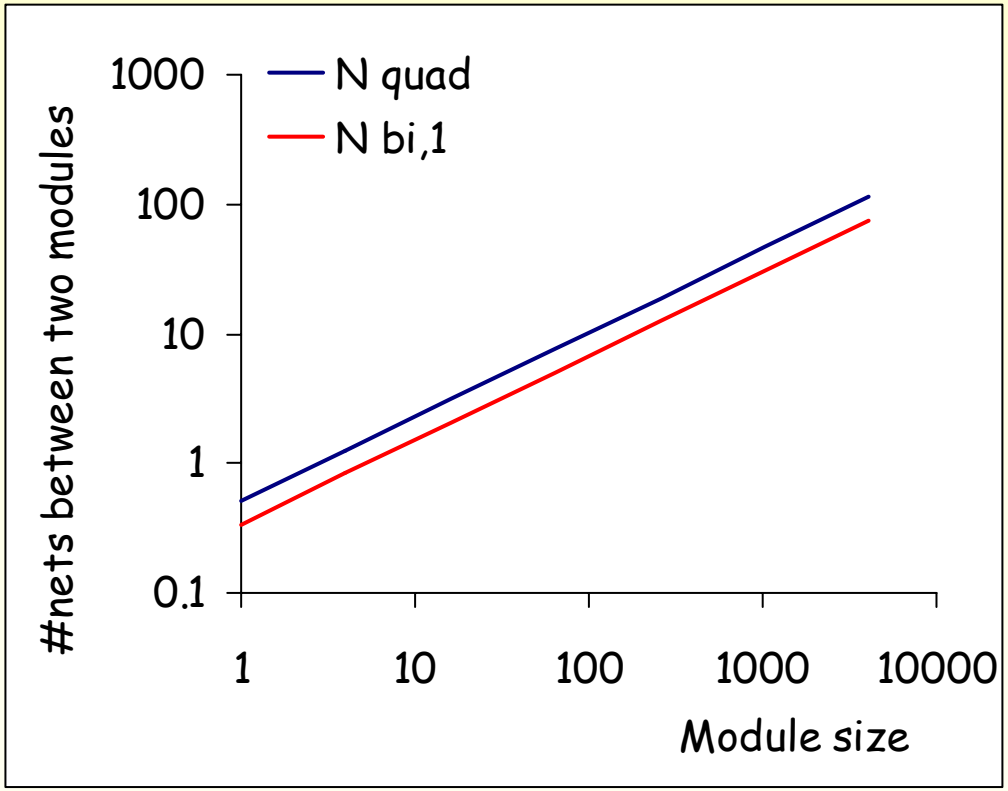
Bipartitioning vs. 4-way partitioning

Number of nets connecting each module pair that is separated during the first cut (p=0.65, t=4) :

$$N_{bi,1} = \frac{t4^k}{4}\left(2^p - 2^{2p-1}\right)$$



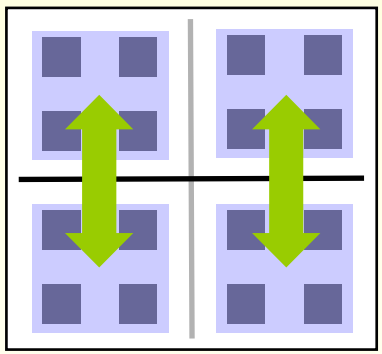
2 neighbouring and 2 diagonal module pairs



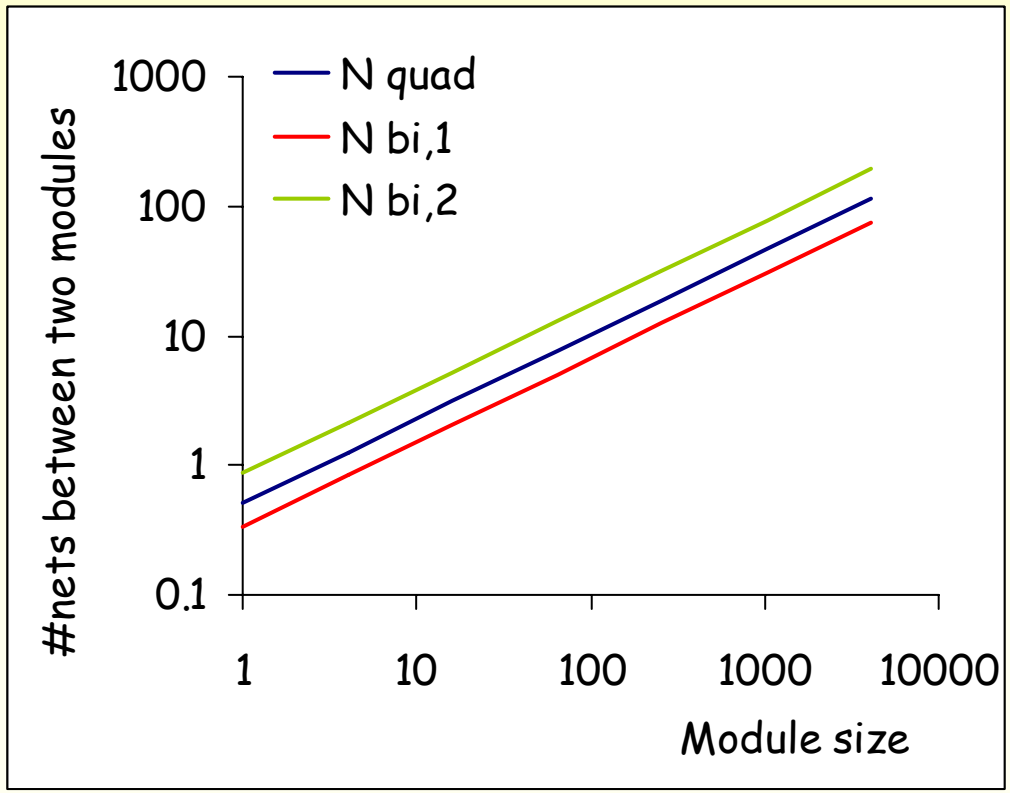
Bipartitioning vs. 4-way partitioning

Number of nets connecting each module pair that is separated during the second cut (p=0.65, t=4) :

$$N_{bi,2} = \frac{t4^k}{2}\left(2 - 2^p\right)$$



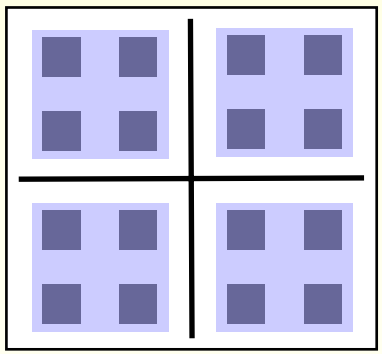
2 neighbouring module pairs

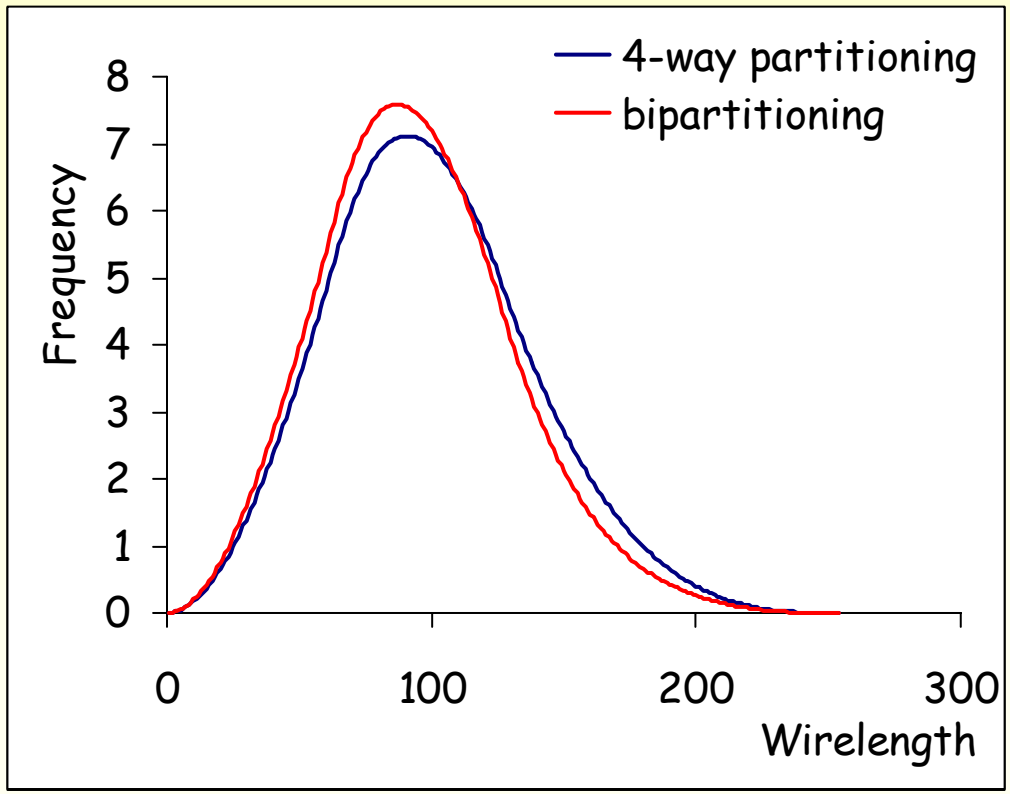


Bipartitioning vs. 4-way partitioning

Wirelength distribution corresponding to one hierarchy level for:

- modules of 64 x 64
- p = 0.65
- t = 4





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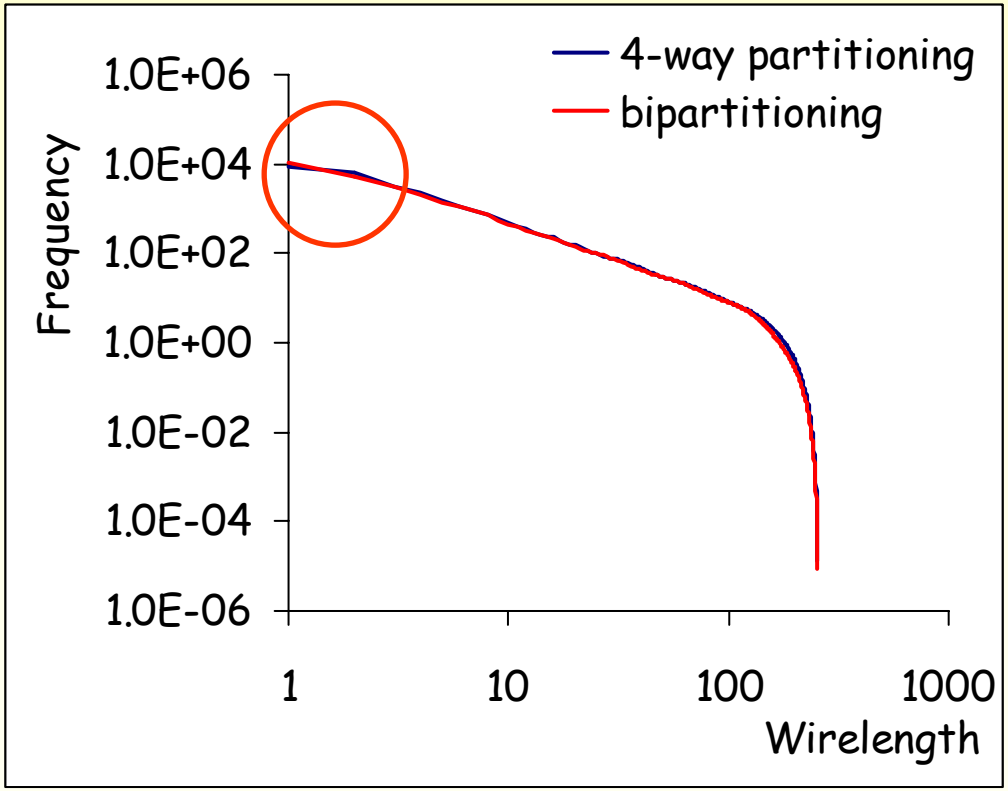
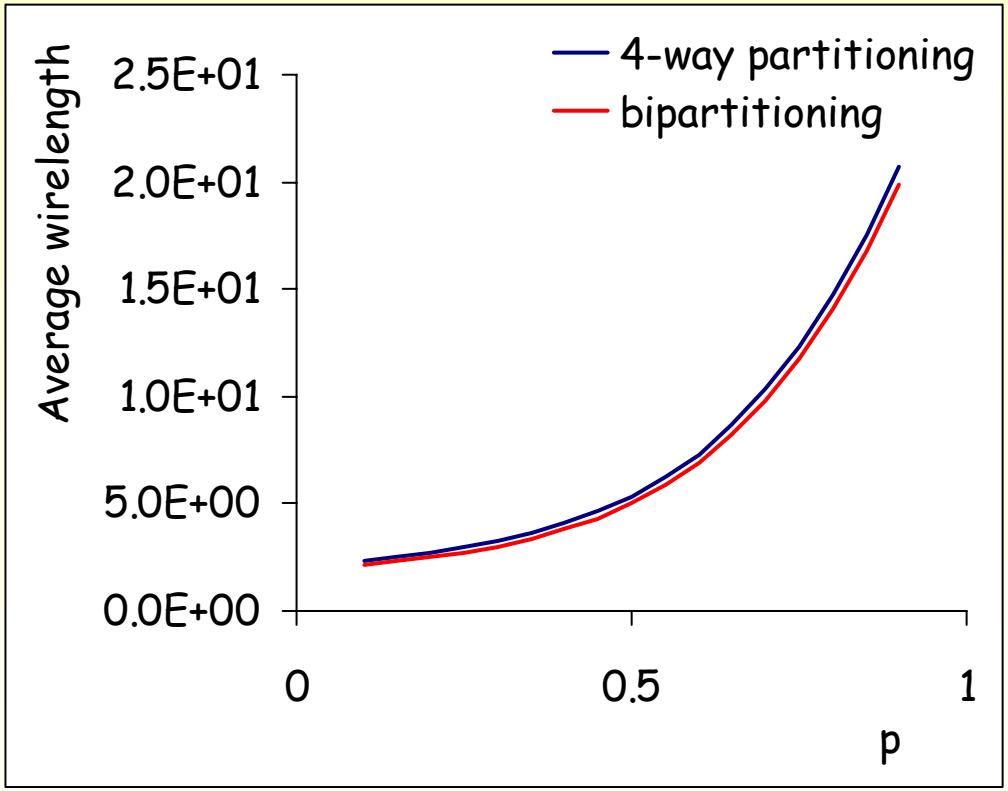


Can still be calculated analytically !

Bipartitioning vs. 4-way partitioning

Average wirelength for:

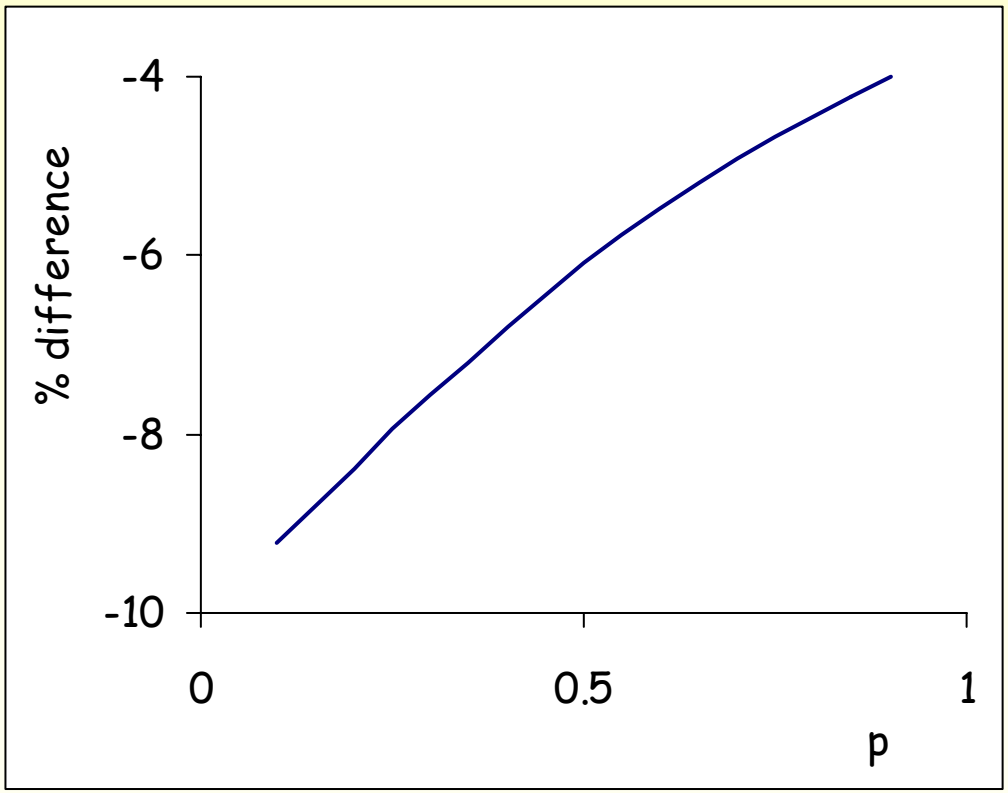
- circuits of 16384 gates
- p from 0.1 -> 0.9
- t = 4



Bipartitioning vs. 4-way partitioning

Relative difference between average wirelength using 4-way and bipartitioning for:

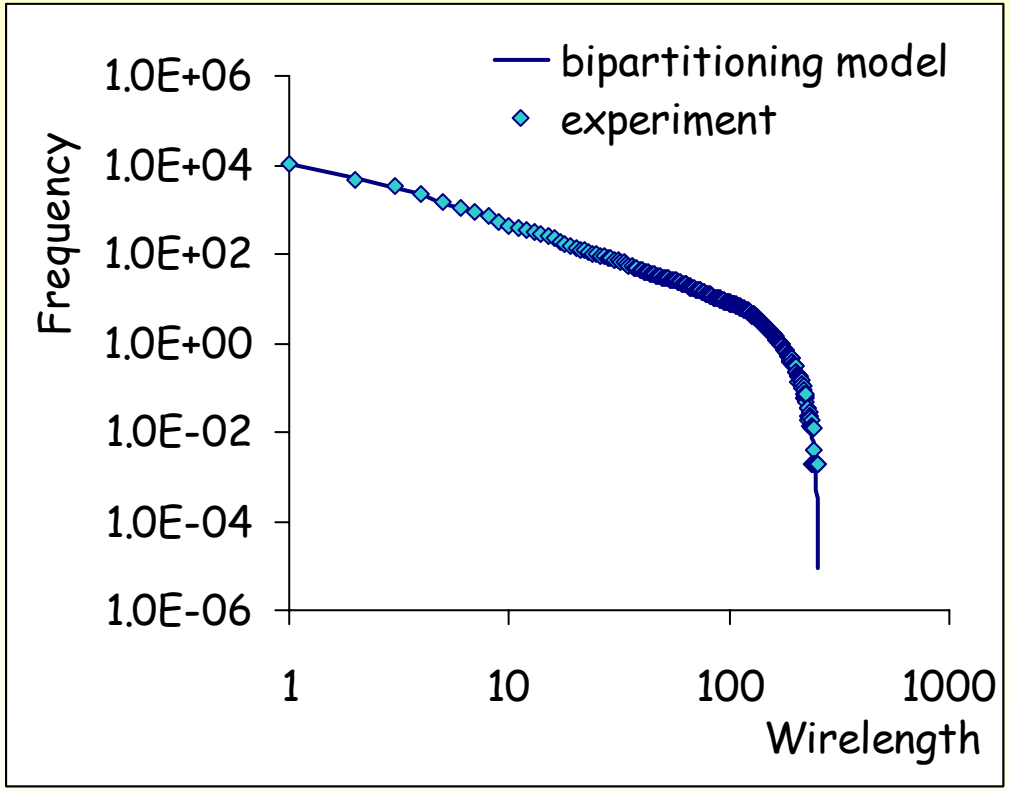
- circuits of 16384 gates
- p from 0.1 -> 0.9
- t = 4



Bipartitioning vs. 4-way partitioning: validation

Wirelength distribution for:

- circuit of 16384 gates
- p = 0.65
- t = 4
- 500 placement runs



Bipartitioning vs. 4-way partitioning: validation

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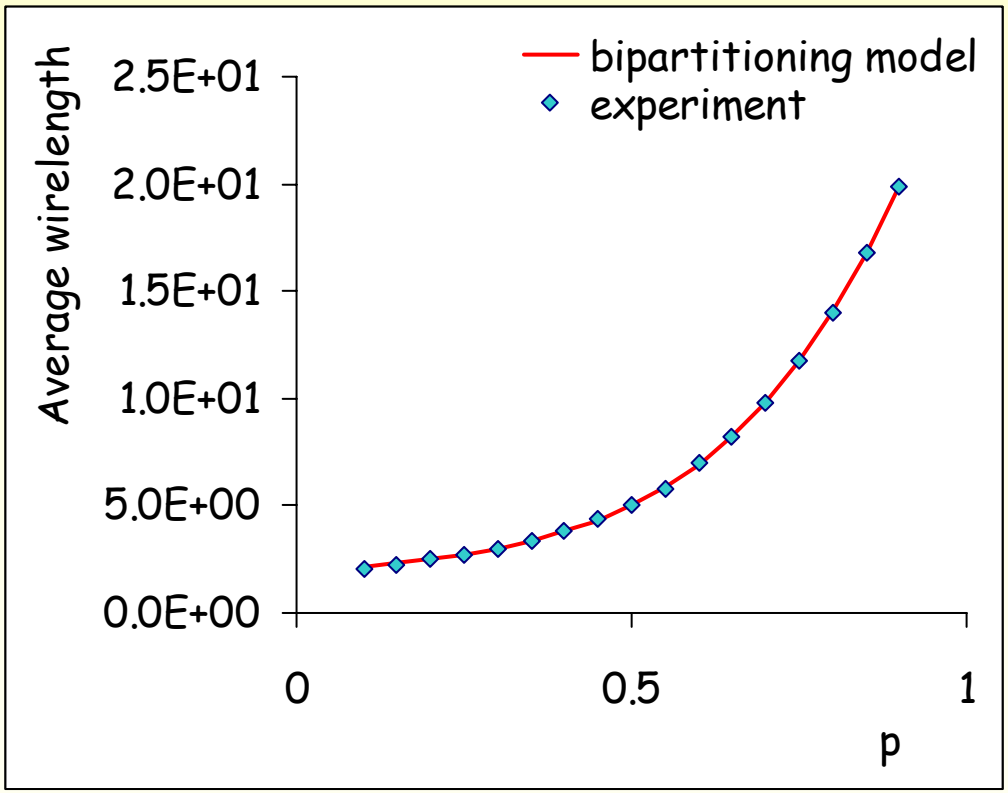

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From Rent's rule to the Rent characteristic

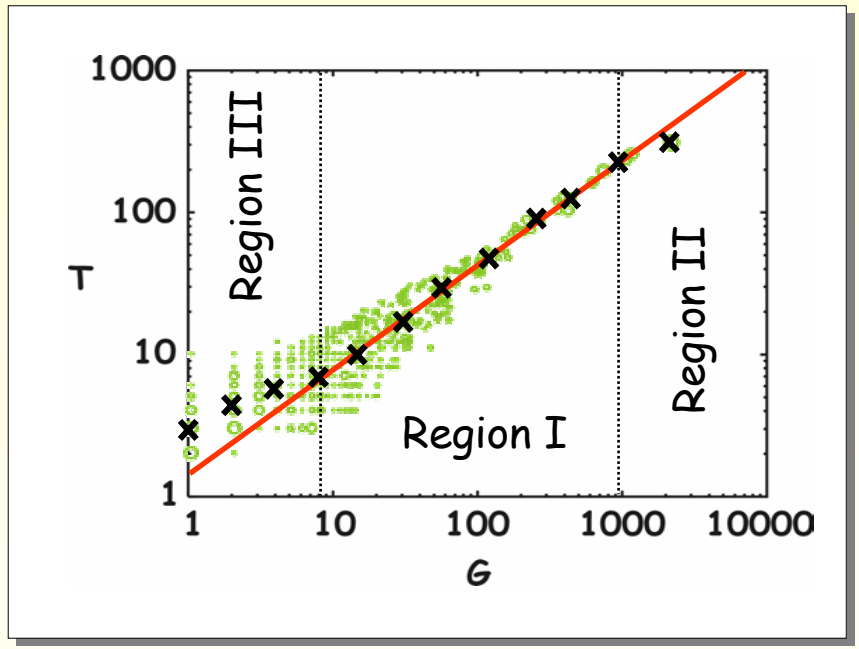
Derivation of Rent parameters for a given circuit :

- Perform hierarchical circuit partitioning
- Find average data points for T vs. G (=Rent characteristic)
- Fit power law to region I

$$T = tG^{p}$$

p: Rent exponent

t: Rent coefficient



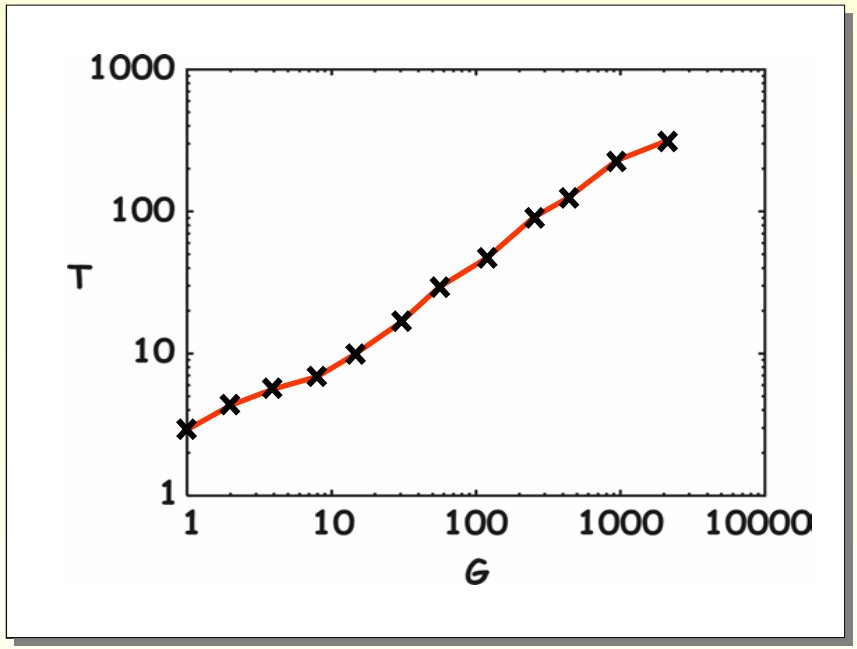
From Rent's rule to the Rent characteristic

Deviations from Rent's rule cause errors in model !

-> Use Rent characteristic instead

Not analytical

-> numerical model evaluation required

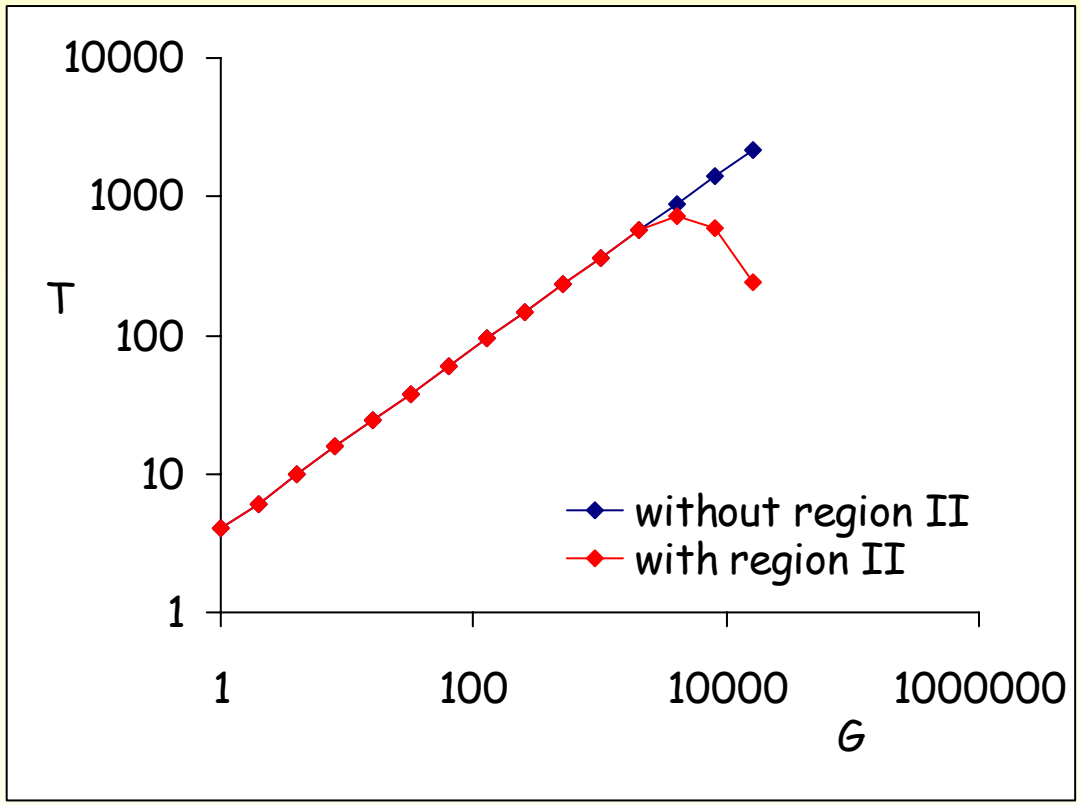


Impact of region II

New synthetic benchmark circuits with same t and p, but with region II

Example for:

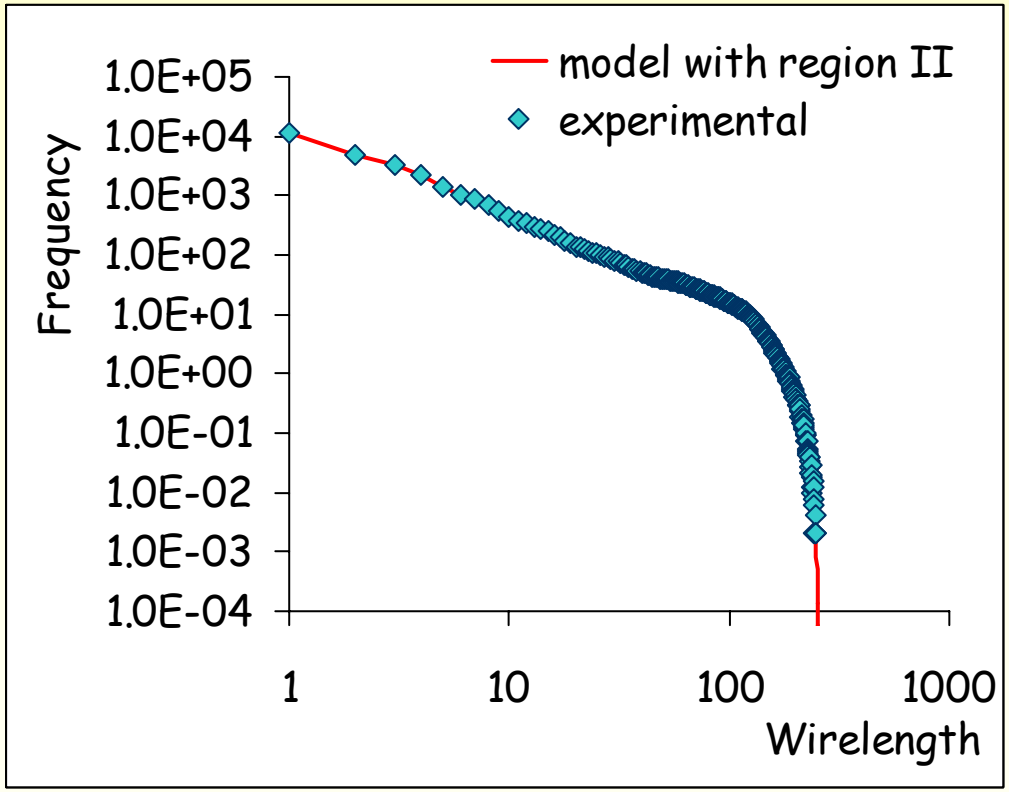
- p = 0.65
- t = 4



Impact of region II

Wirelength distribution for:

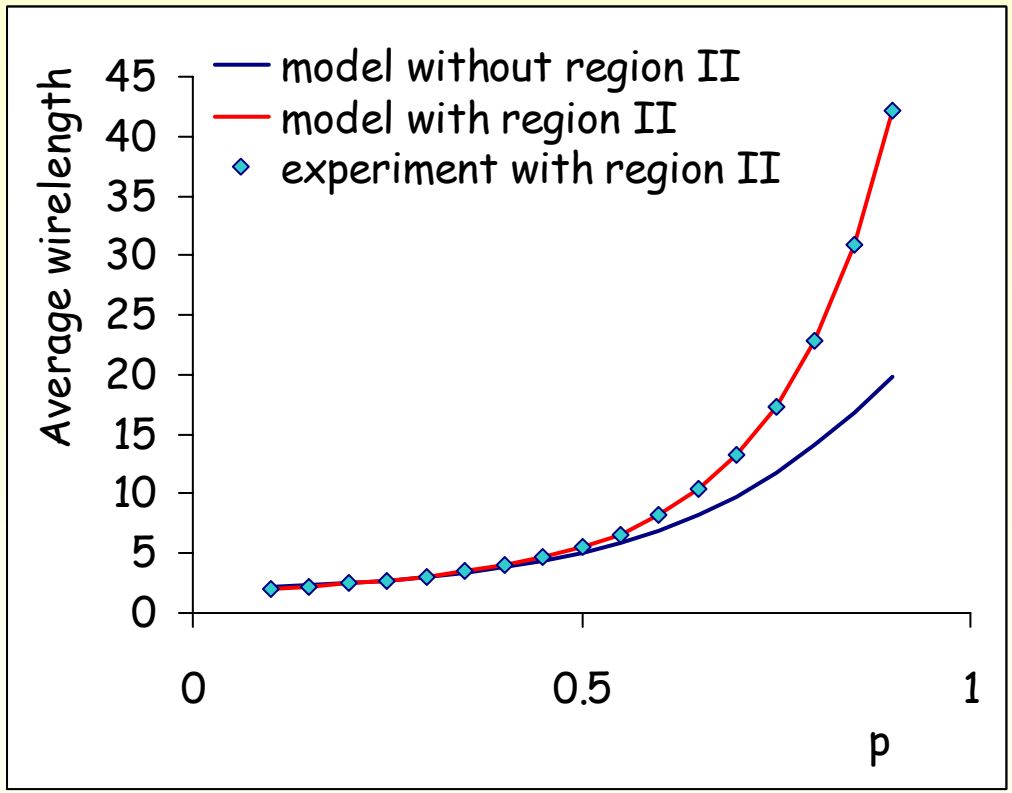
- circuit of 16384 gates
- p = 0.65
- t = 4
- bipartitioning based placement
- 500 placement runs



Impact of region II

Average wirelength for:

- circuit of 16384 gates
- p = 0.65
- t = 4
- bipartitioning based placement
- 500 placement runs



Presentation outline

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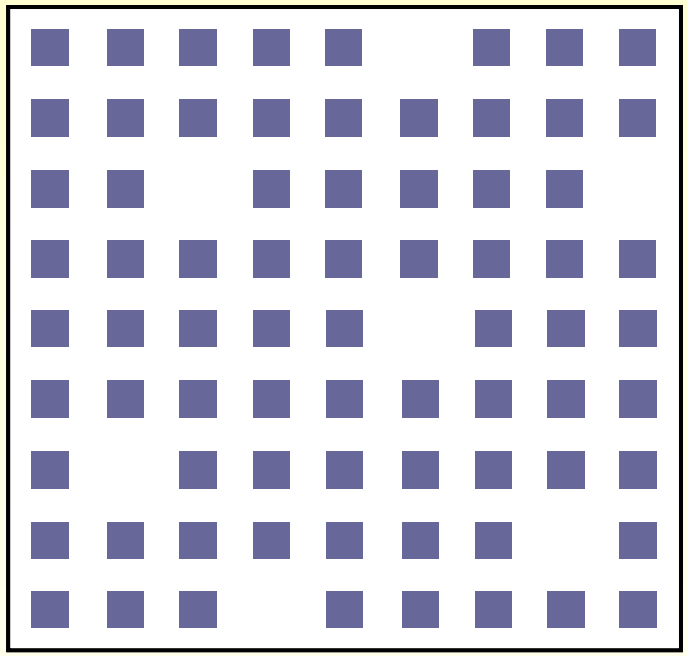
Circuit size and layout grid size

Number of gates usually different from number of layout grid positions :

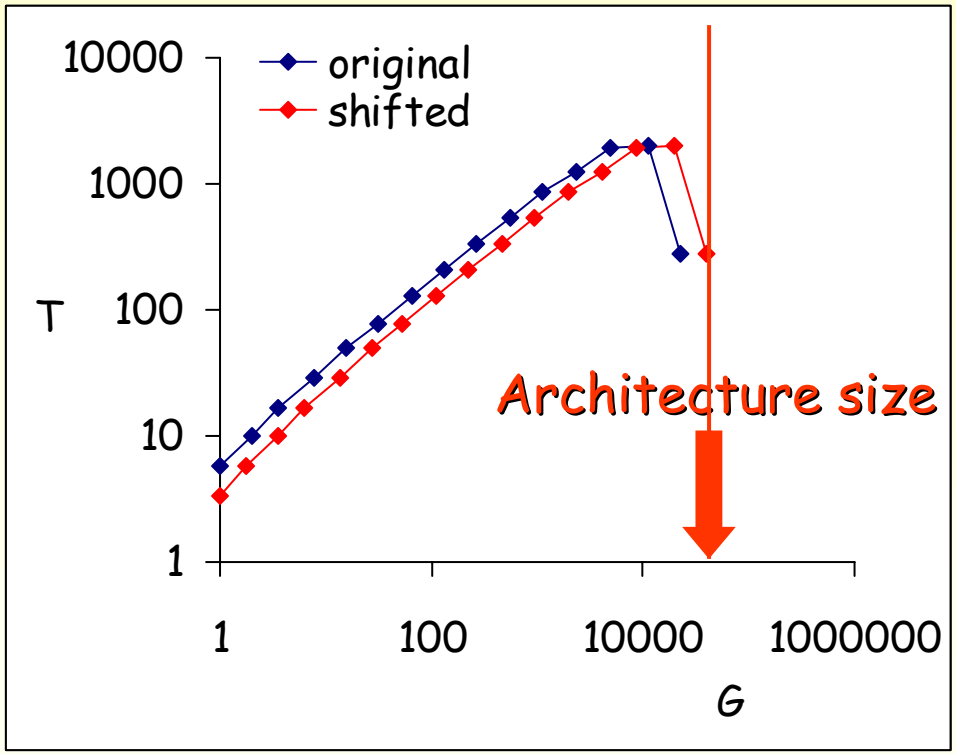
- Some empty positions in placement grid
- Suppose homogeneously spread

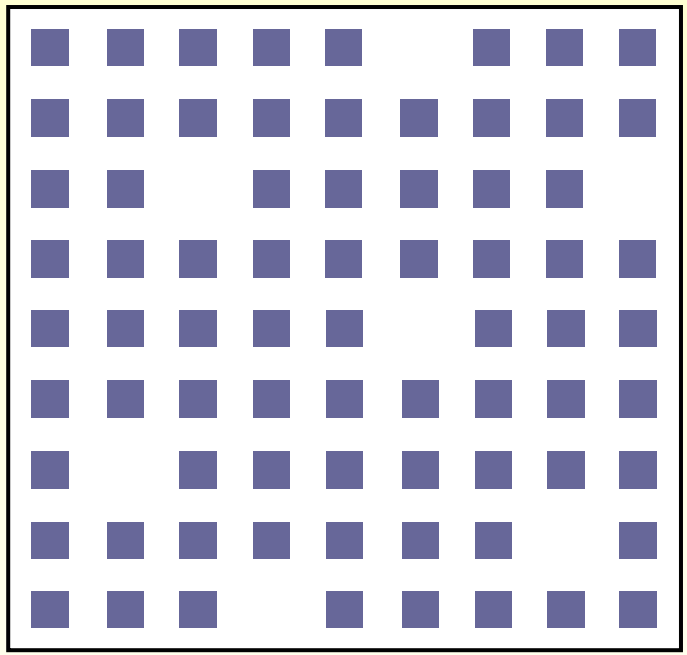


Circuit size and layout grid size

Need to 'shift' Rent characteristic

Example : ibm03, 57% filling ratio

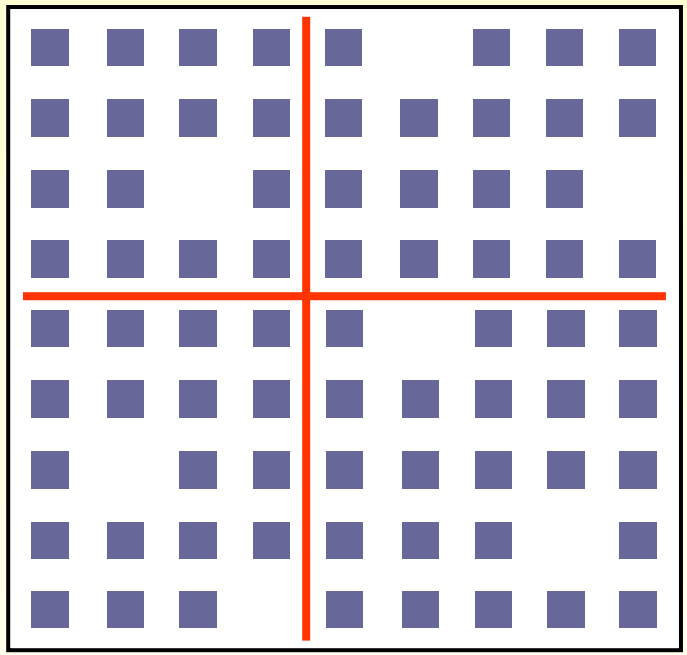




Circuit size and layout grid size

Grid side rarely an exact power of 2 :

- Unequal module sizes during architecture partitioning



Impact on model :

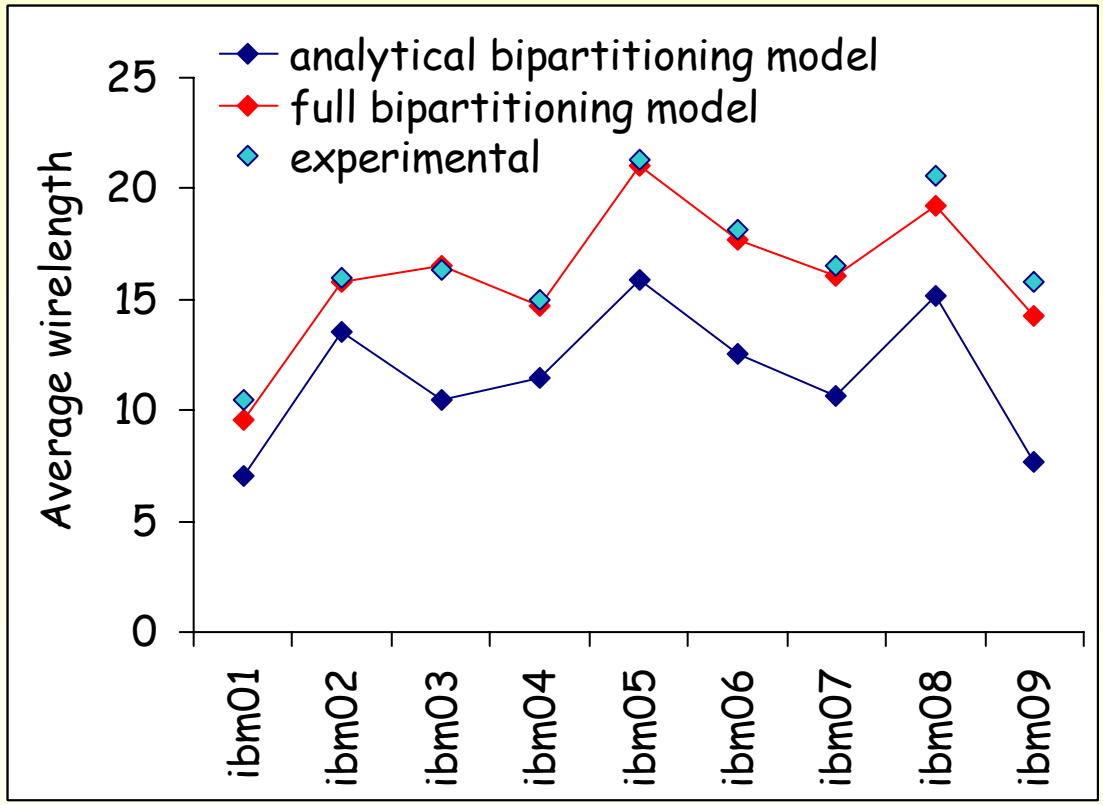
- Site functions for rectangles (easy)
- Bipartitioning: no other changes
- 4-way partitioning: suppose number of nets connecting two modules proportional to size of each module

And now for some 'real' circuits
model compared to unoptimized placement

- benchmarks: ibm01 – ibm09
- placed in square grid
- ~ 95 % filled
- using unoptimized bipartitioning based placement (100 runs)

Remaining deviations probably caused by inhomogeneity in circuit complexity

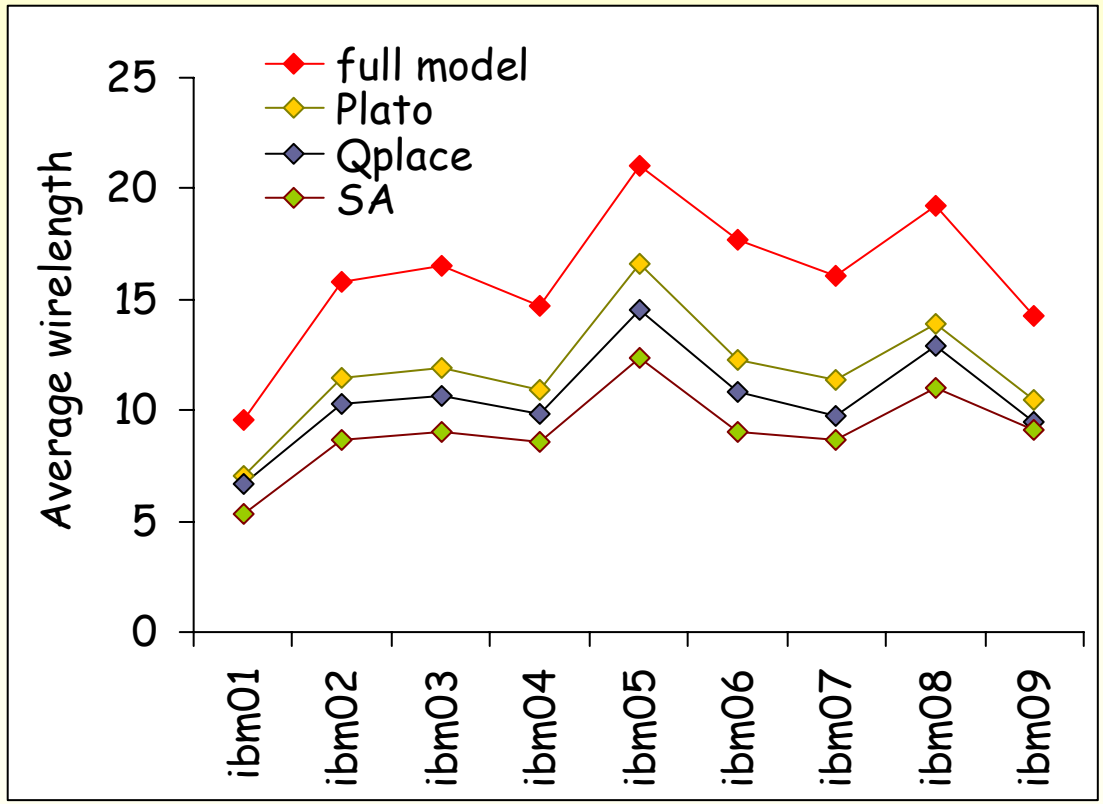
Improved by including Rent's rule variance in model (Verplaetse) ?



... and compared to optimized placement

- benchmarks: ibm01 – ibm09
- placed in square grid
- ~ 95 % filled
- using optimized placement :
  - Plato (10 runs)
  - Qplace (1 run)
  - homogeneous SA – cooling factor 0.999 (1 run)

Overestimation, but very good correlation !



Correlation results

Model	Unoptimized	optimized		
		Plato	Qplace	SA (0.999)
Analytical bipartitioning	0.856	0.879	0.892	0.810
Full bipartitioning	0.990	0.977	0.971	0.949

Significantly higher correlations with all placement results for full bipartitioning model !

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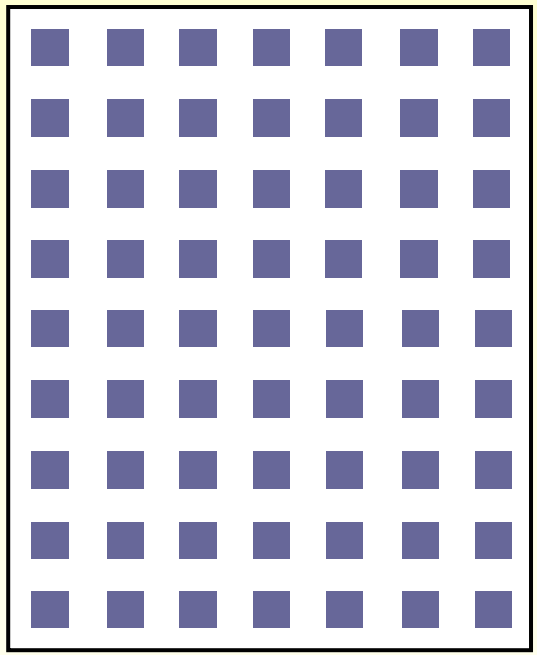
Rectangular grids ...

Floorplanning: sometimes smaller layout area if rectangular subcircuit layouts allowed

-> change grid aspect ratio



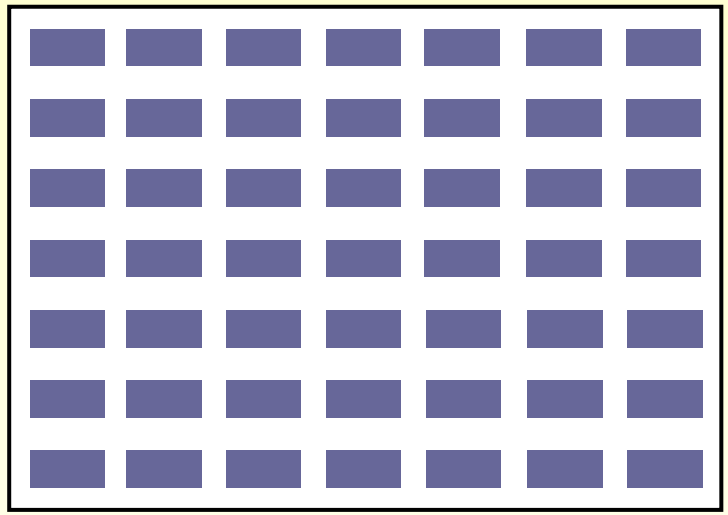
Impact on model :

- Site functions for rectangles (easy)
- Partitioning order : choose cut direction to minimize module aspect ratio

... and rectangular cells

Cells are often rectangular instead of square : cost in X- and Y-directions different

-> change cell aspect ratio

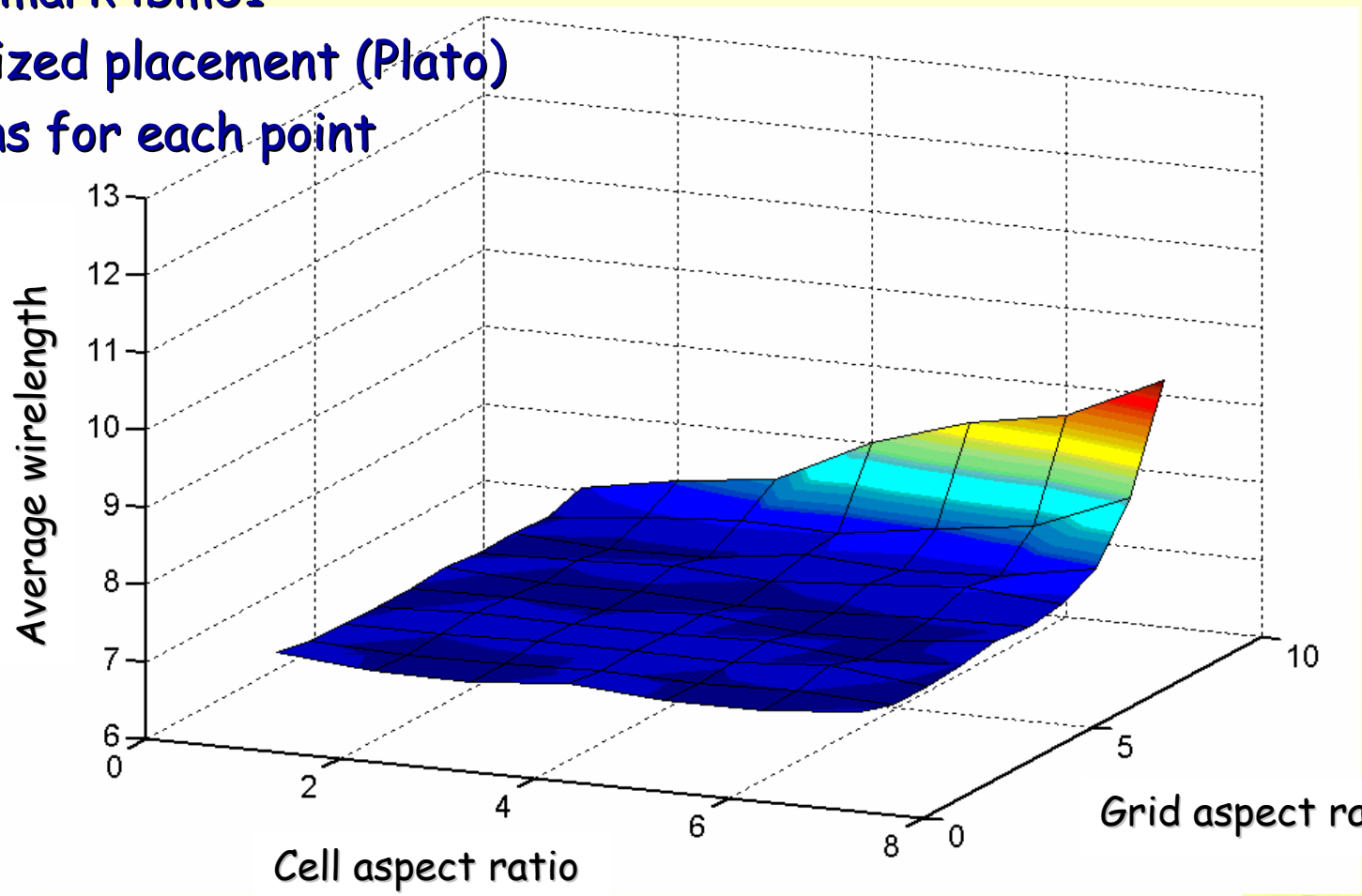


Impact on model :

- Convert site functions for weighted unit distances (easy)
- Currently only for rational cell aspect ratios !
- Partitioning order : choose cut direction to minimize module aspect ratio

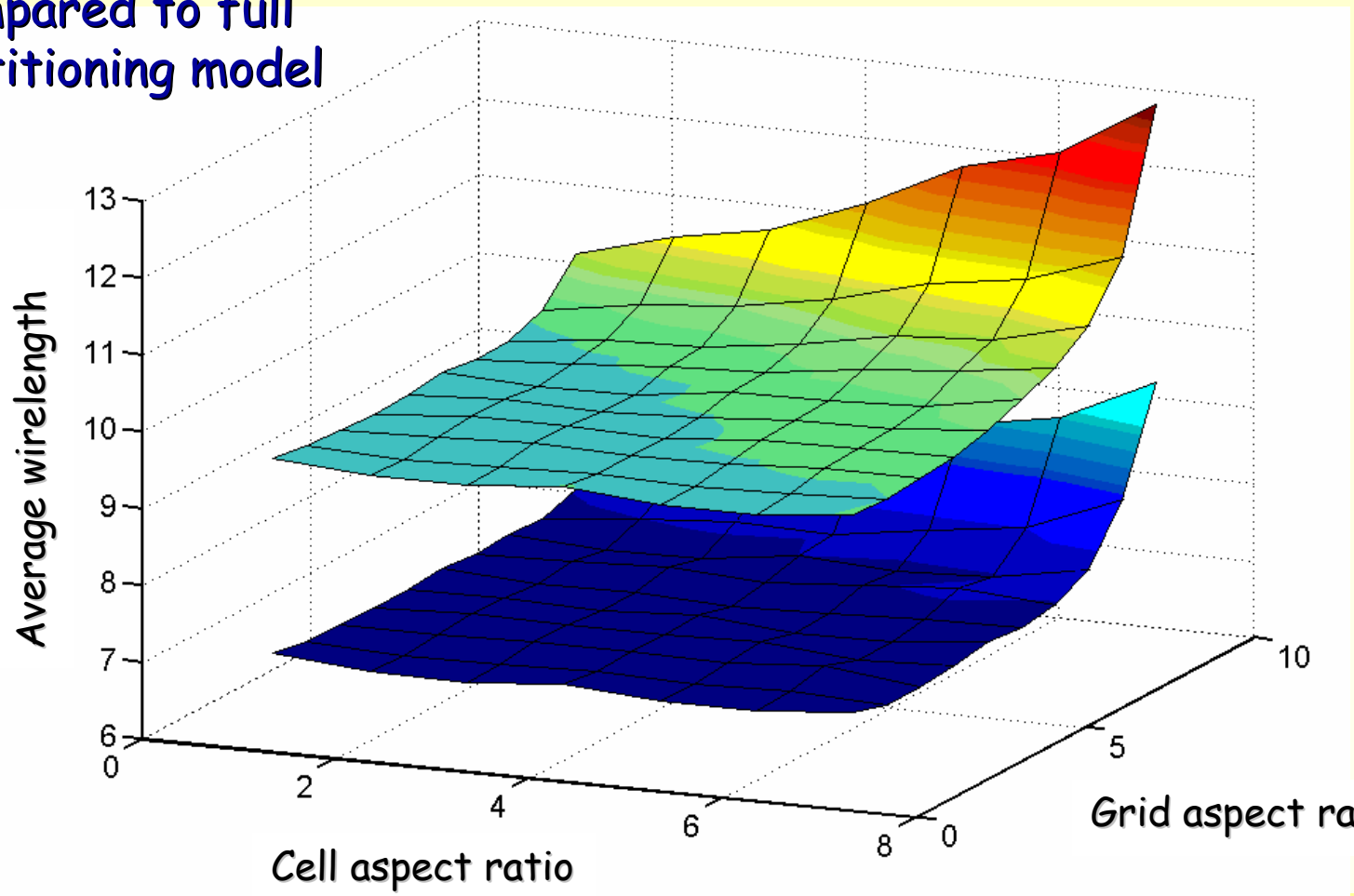
Impact of grid and cell aspect ratio

- benchmark ibm01
- optimized placement (Plato)
- 10 runs for each point



Impact of grid and cell aspect ratio

- ... compared to full bipartitioning model



Impact of grid and cell aspect ratio

Correlations between model and experiment for each benchmark (across 70 architectural variants)

Benchmark	Correlation
ibm01	0.964
ibm02	0.990
ibm03	0.999
ibm04	0.987
ibm05	0.998
ibm06	0.979
ibm07	0.992
ibm08	0.994
ibm09	0.998

Correlations are very high

Model is very suitable for comparing different options

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Conclusions

Extension of Donath's model to make it accord better with real placement experiments:

- Bipartitioning vs. 4-way partitioning (analytical)
- Use of Partitioning Rent characteristic (region II !)
- Relaxation of circuit and architecture size
- Relaxation of architecture grid and cell aspect ratio

Conclusions

Systematic experimental validation, matching assumptions as closely as possible. Results:

- For synthetic (homogeneous) benchmark experiments, models are almost exact (within statistical variation)
- For real benchmarks (unoptimized), some deviations occur, probably due to inhomogeneity of circuit complexity
- Average wirelengths from our models show very high correlation with experimental optimized placement results with different tools

Conclusions

And ...

the whole thing was implemented in Matlab and is available on request

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Future work

- Include external connections
- Include multi-terminal connections (Stroobandt's models ?)
- Include optimization (tricky !!)