Terminal optimization analysis for functional block re-use

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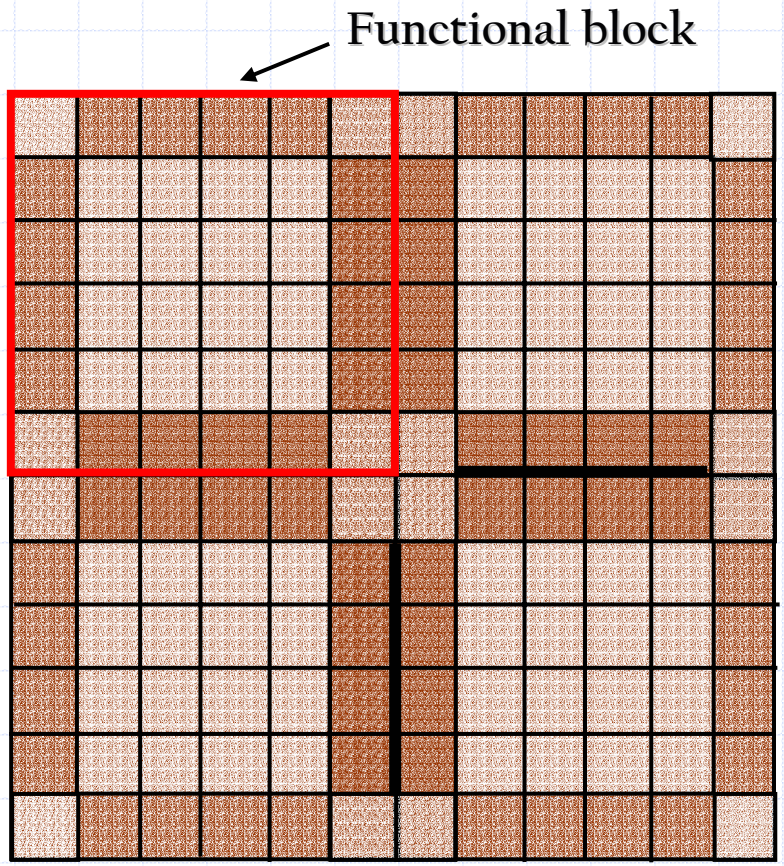
Introduction

- Aid the designer in designing a SoC chip to optimize wire length on the chip.
- Improve clock rate and/or decrease power loss of the chip.
- Provide a mathematical model which can be used to chose between two methods of design.

Description of SoC Chips

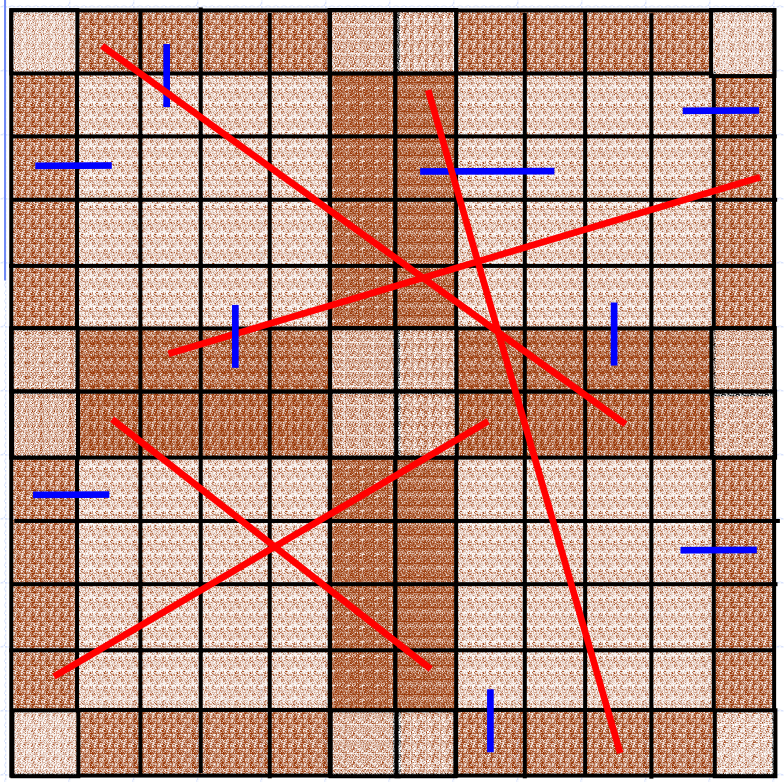
- Increasing trend towards re-use of large functional blocks
- Like a printed circuit board, pre-built functional blocks are mounted on the chip
- Analysis on functional block placement has not yet been done.



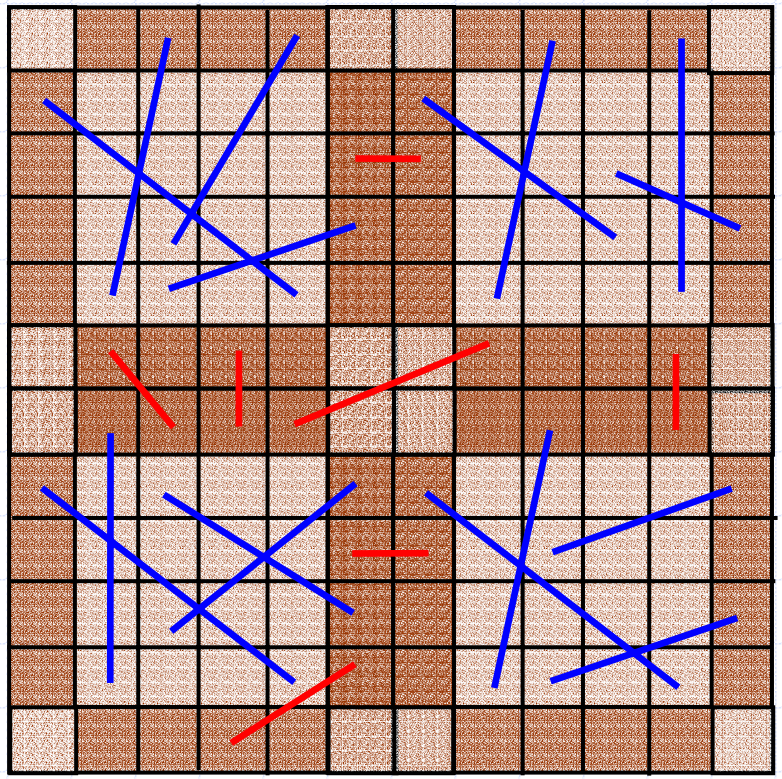
Local and Global optimization

Pins may be placed to optimize either global or local wire lengths.

Local Optimization



Global Optimization



Mathematical Model

- Analysis is based on wire length distribution
- Function to find the number of wires of length l

$$N(l) = q(l)\, D(l)$$

$$D(l) = Number\ of\ placement\ sites$$

$$q(l) = Pr\{placement\ site\ is\ filled\}$$

Probability function *q(l)*

- Two forms of probability used in model
  - For random placement of pins
  - For optimized placement of pins

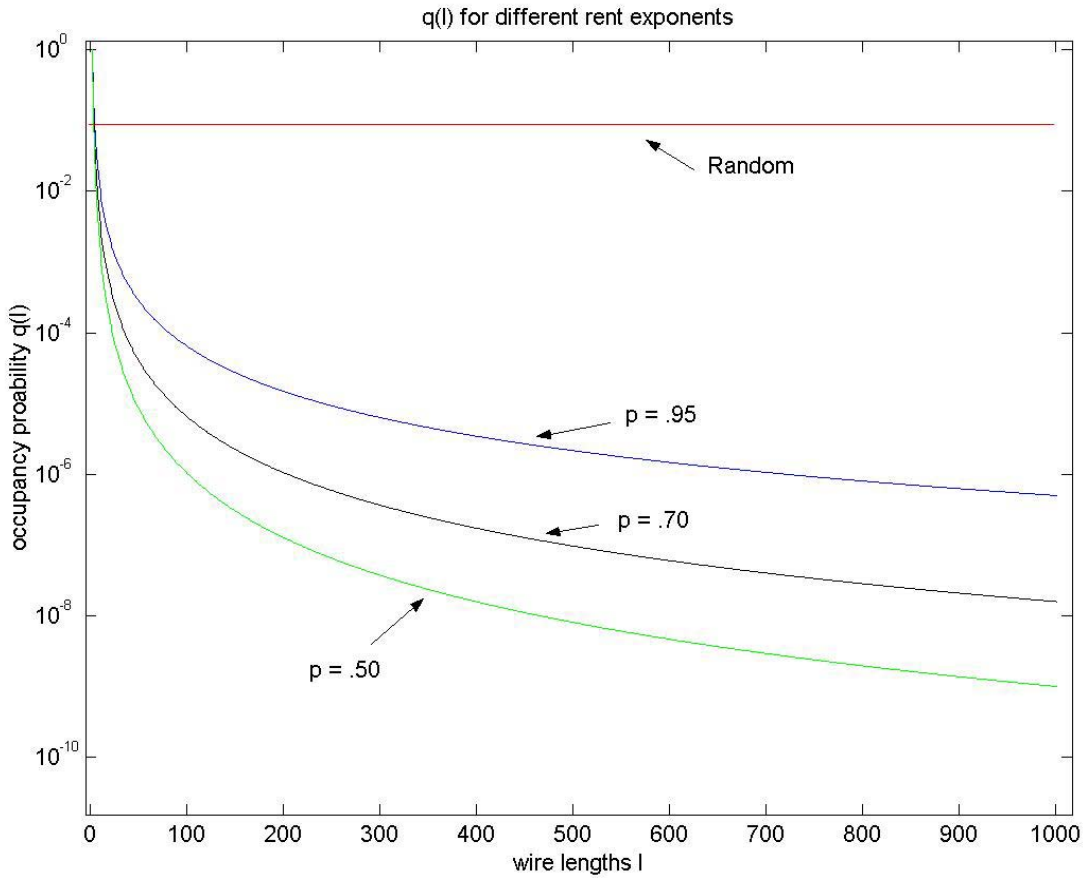
$$q_{random}(l) = K_{random}$$

$$q_{optimized}(l) = K_{opt}\, l^{-(4-2p)}$$

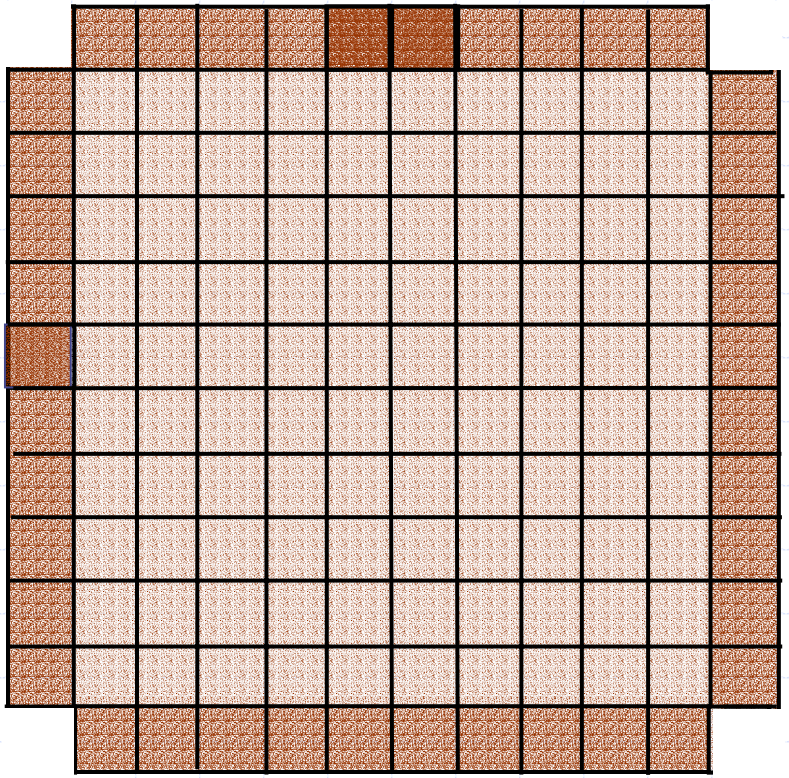
  - In both cases, K_{opt} and K_{random} can be found by ensuring

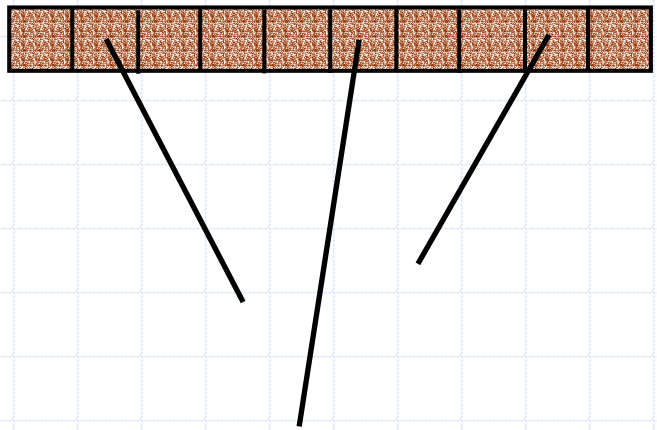
$$Total\ number\ of\ terminal\ connected\ wires = \sum_{l=1}^{L_{max}} N(l)$$

q(l) and the Rent Exponent



Sites function *D(l)* for local wires

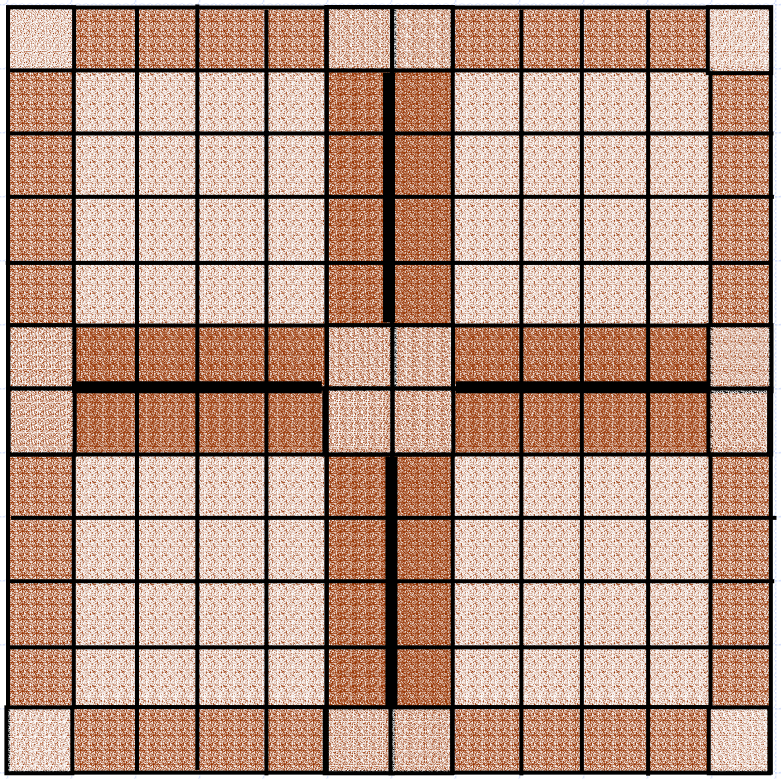


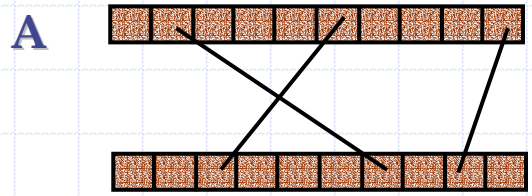


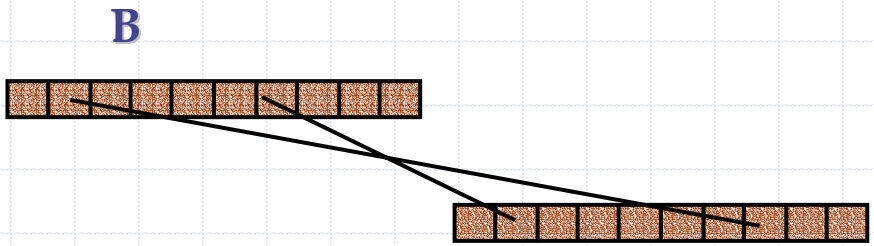
Derived by the method of generating polynomials

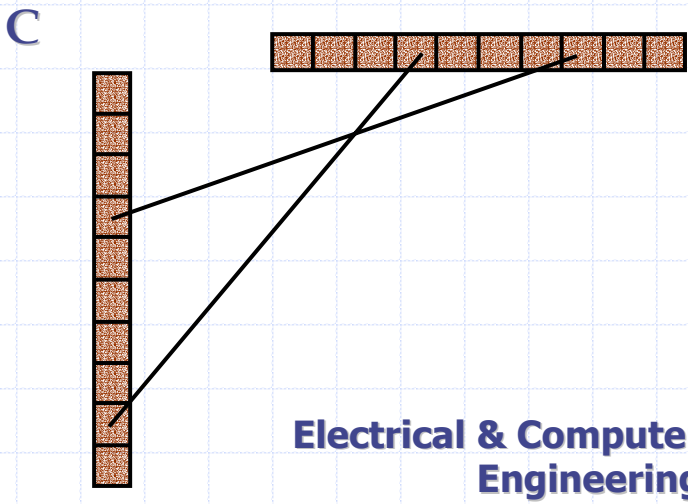
Sites function for global wires

- Can use these three site functions to construct other, higher-level site functions.

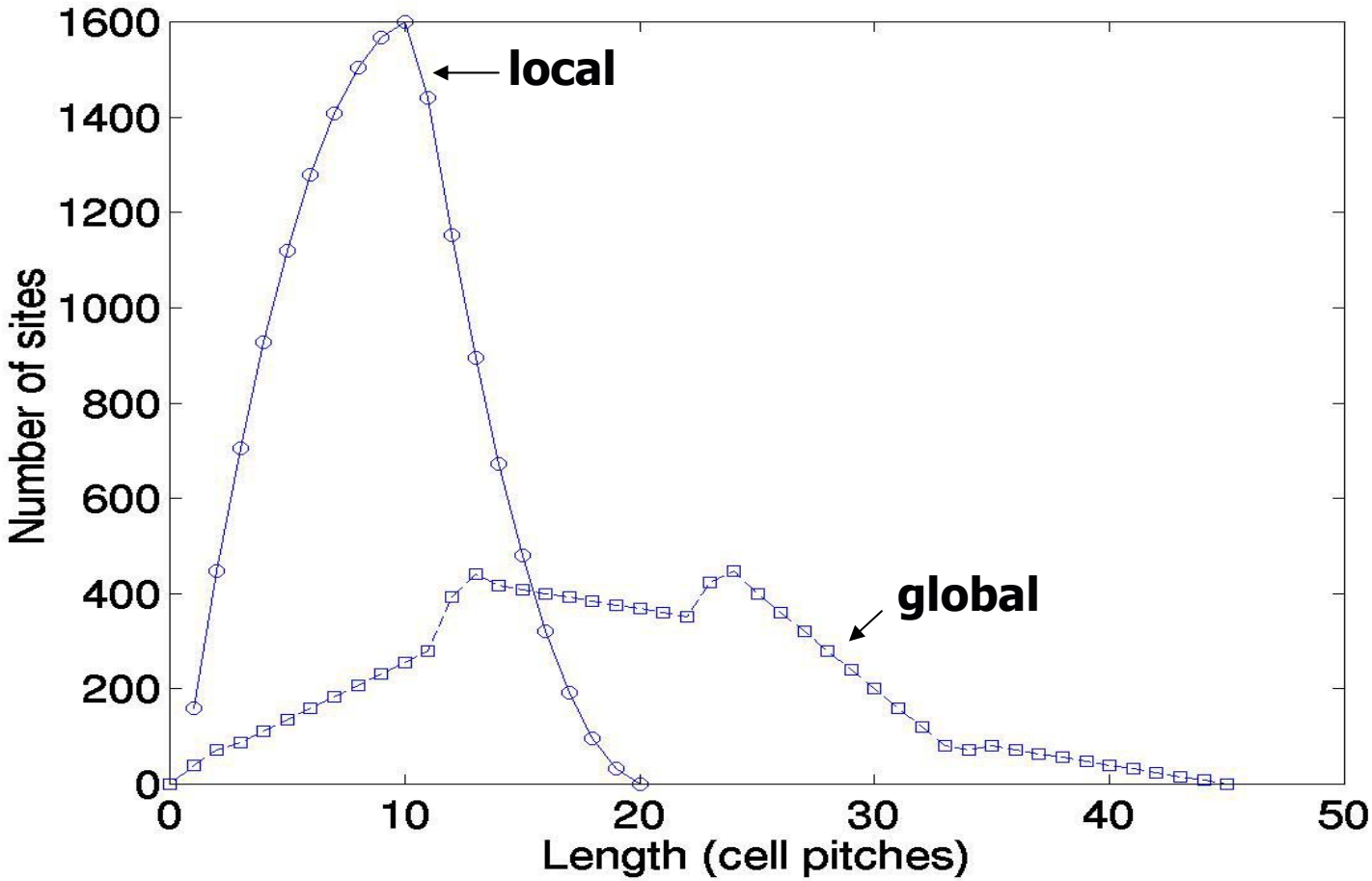








Plot of local and global site functions



Floor Plan Analysis

- Model both case
  - Local Optimization

$$N_{local}^{opt}(l) = q_{opt}(l)\, D_{local}(l)$$

$$N_{global}^{random}(l) = q_{random}(l)\, D_{global}(l)$$

  - Global Optimization

$$N_{local}^{random}(l) = q_{random}(l)\, D_{local}(l)$$

$$N_{global}^{opt}(l) = q_{opt}(l)\, D_{global}(l)$$

Finding total Wire length

- The length distribution is used to calculate the total wire length due to pins connected nets
- Same equation is used for local or global optimization

$$Total\ Wire\ Length = \sum_{l=1}^{L_{max}} l\, N_{local}(l) + \sum_{l=1}^{L_{max}} l\, N_{global}(l)$$

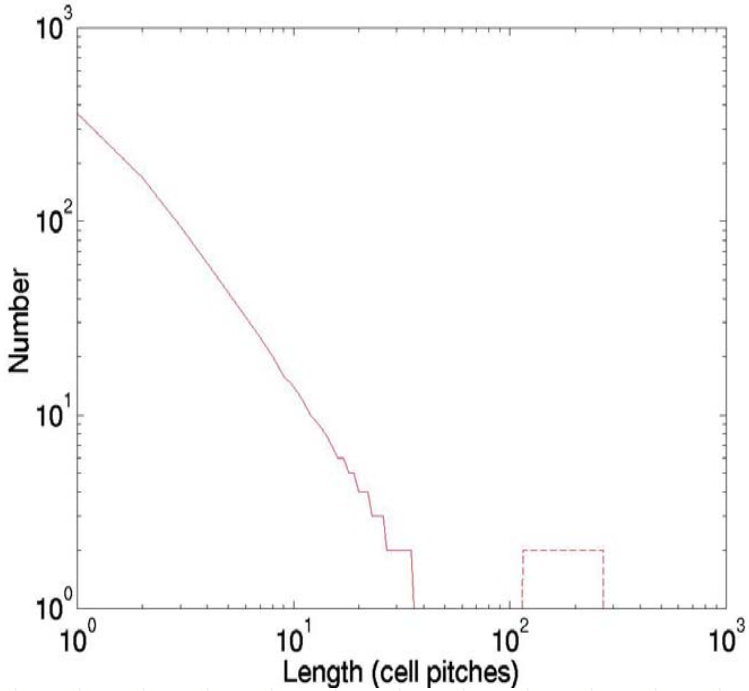
- Compare results for local and global optimization to find which method of optimization is better.

Analysis:

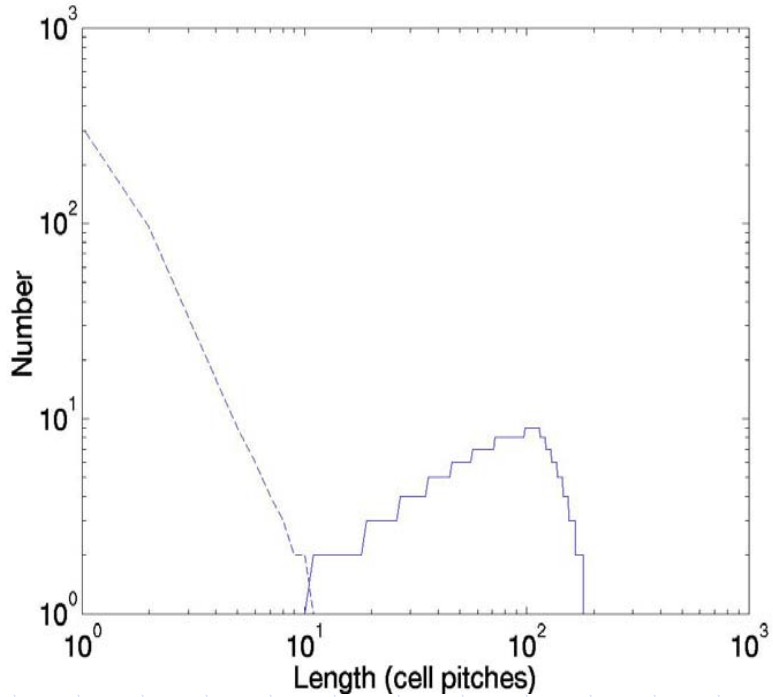
Square chip with 4 identical functional blocks

12,769 cells and 245 terminals per functional block

Local Optimization

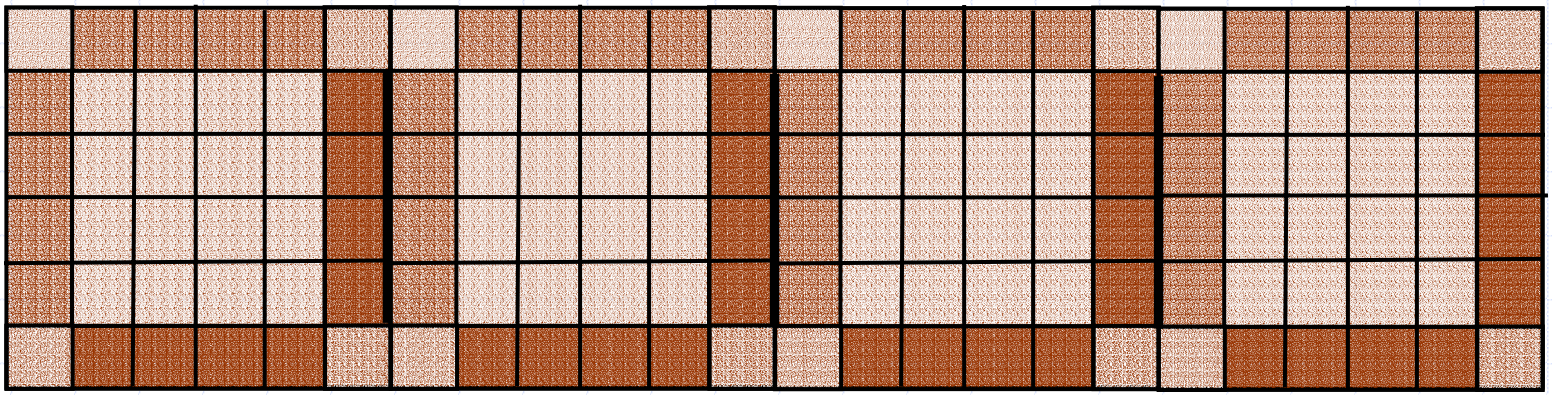


Global Optimization



- Local → smaller total wire length due to pins
- Global → smaller max length due to pins

Analysis: performed on linear array



- Linear array using the same 4 functional blocks as the square arrangement

Comparison of results

Square Floor plan				
Optimization Strategy	Local Length	Global Length	Total Length	Maximum Length
Local Global	5,645 92,580	85,488 901	91,113 93,481	333 199
Linear Floor plan				
Optimization Strategy	Local Length	Global Length	Total Length	Maximum Length
Local Global	5,645 92,580	104,598 1,080	110,243 93,660	428 199

- Global optimization yields smaller total wire length and a smaller maximum wire length
- Square floor plan produced less wire then linear

Conclusions

- The choice between optimizing local and global wires depends on the geometry of the chip.
- By deriving three basic site functions for global wires, the global site function for higher level designs can be realized as a linear combination of these basic site functions.
- A model has been shown to aid in the decision between optimizing global or local wire length to decrease the total wire length.

Acknowledgements

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