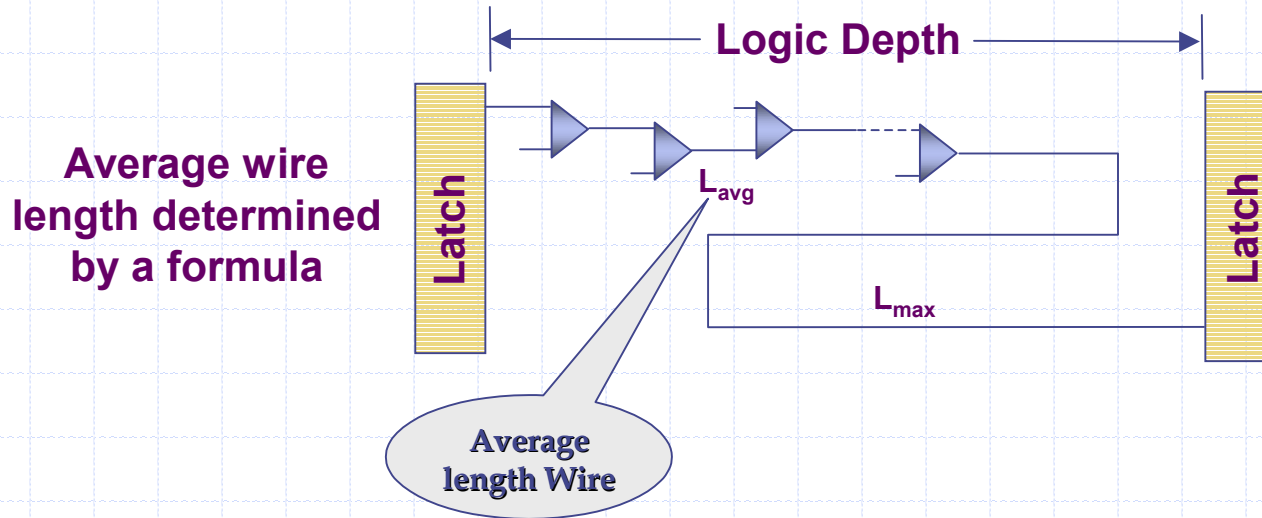


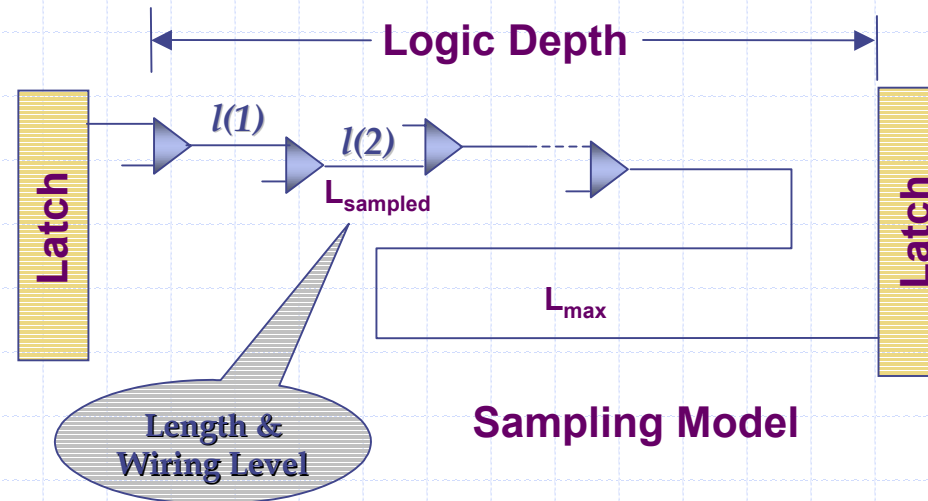
Stochastic Wire Length Sampling For Cycle Time Estimation

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- Cycle time models are used for a-priori estimation of chip Clock Rate.
- Standard model incorporates delays incurred due to
 1. Standard Cell.
 2. Interconnection Wire.
- Electrical Characterization of Interconnecting Wire is based upon wire geometry of the layer where the wire of average length resides.

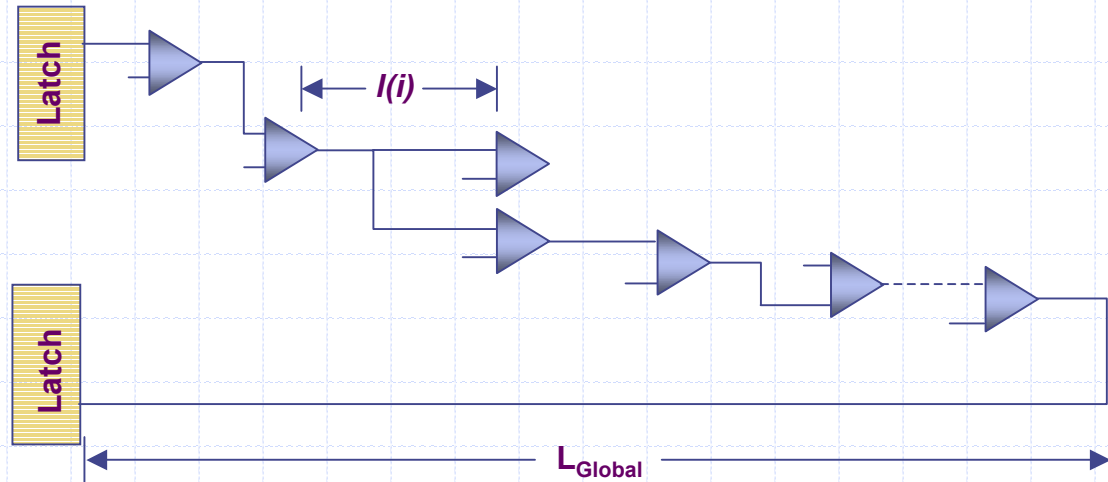


- Sample wires from the Global Wire length Distribution.
- Before sampling we need
 1. Pseudo-Placement (Obtain Global Wire Length Distribution).
 2. Pseudo-Routing (Allocation of Wires to Wiring Levels).
- Sampling model incorporates the effects of varying wire geometries in different layers.
- Provides an estimate of variation due to the inherent stochastic nature of the layout process.

Stochastic Cycle Time Model

Electrical Characterization:

- R_{int} : Interconnect Resistance
- C_{int} : Interconnect Capacitance
- R_{cell} : Gate Resistance
- C_{cell} : Gate Capacitance
- $l(i)$: Wire length



Sakurai model for 50% Rise time:

$$t(i) = 0.377R_{int}C_{int}l(i)^2 + 0.693(R_{cell}C_{int}l(i) + C_{cell}R_{int}l(i) + R_{cell}C_{cell})$$

Collecting terms:

$$t(i) = \underbrace{0.377R_{int}C_{int}l(i)^2}_{\text{Purely interconnect term}} + \underbrace{0.693(R_{cell}C_{int} + C_{cell}R_{int})l(i)}_{\text{Cross Coupling term}} + \underbrace{0.693(R_{cell}C_{cell})}_{\text{Pure device term}}$$

- Quadratic nature of *Sakurai delay model* may induce non-linearity in delay estimates, if the *pure interconnect term* dominates.

Local Delay:

$$t_{local} = \sum_{i=1}^{\text{Logic depth}} t(i)$$

Cycle time:

$$t_{cycle} = \frac{t_{local} + t_{global} + t_{setup} + t_{flip-flop}}{1-skew}$$

Where

$T_{flip-flop}$: Time take from the clock edge data is captured at the input latch to when its available at output (200 *ps*)

T_{setup} : stabilizing time for inputs of latches of prior to next rising clock edge (200 *ps*).

skew : worst case skew between clocks (10 % of cycle time).

Global Wire length estimate – Pseudo – placement

- Global Wire length distribution extracted from a standard netlist, ibm03p (ISPD) of approximately 27000 cells.
- The length distribution (N) is determined by using

$$N(L) = KqD$$

Where

$N(L)$ is number of wires of length L .

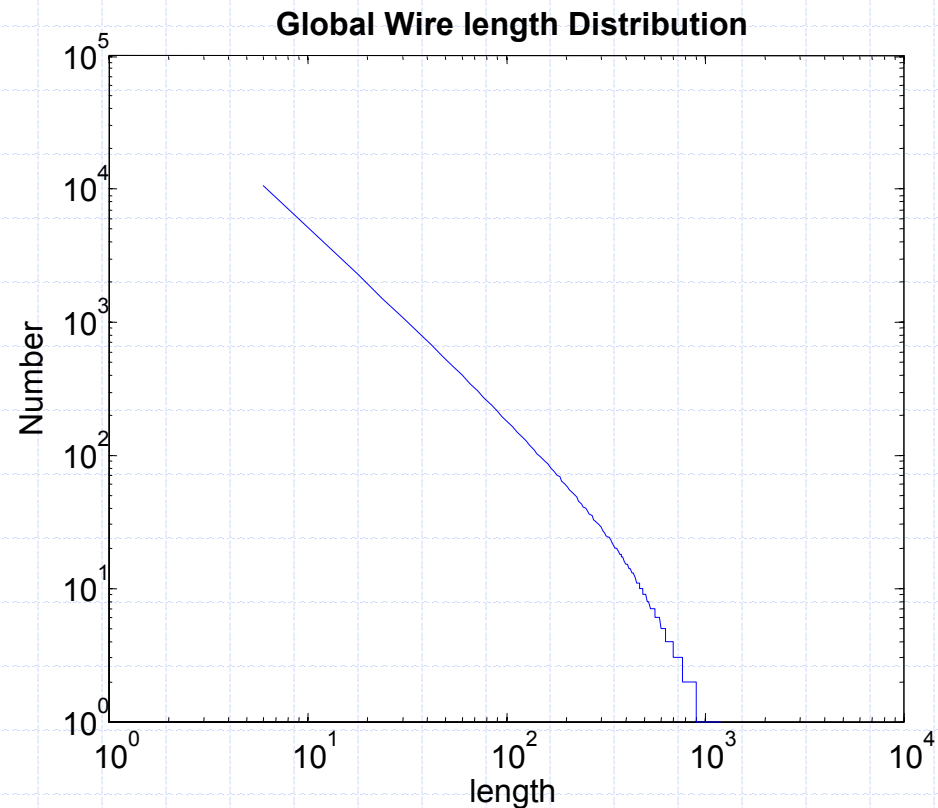
q is occupancy probability given by

$$q = l^{2\rho-4}$$

ρ = rent exponent.

K is a normalization coefficient.

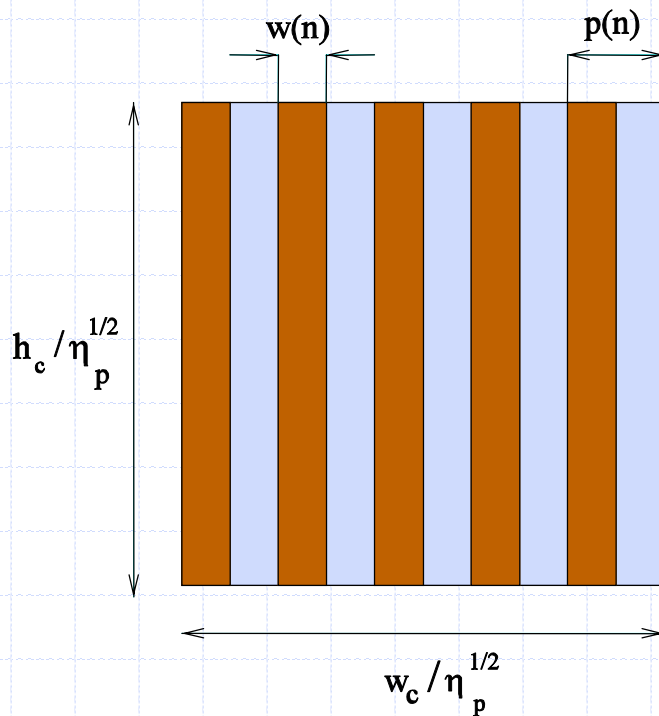
D is all probable sites for cell placement for a given floor plan.



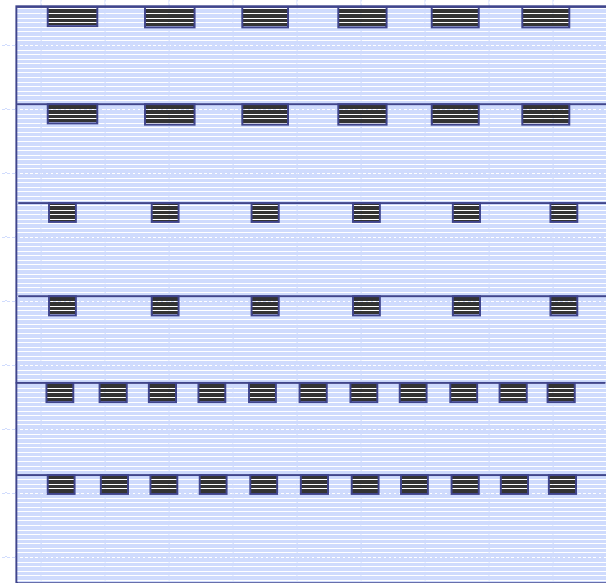
Wire Allocation (pseudo routing)

Parameters for determining wiring capacity

- Geometrical parameters for the layer
- Placement efficiency
- Floor plan



Layer 6

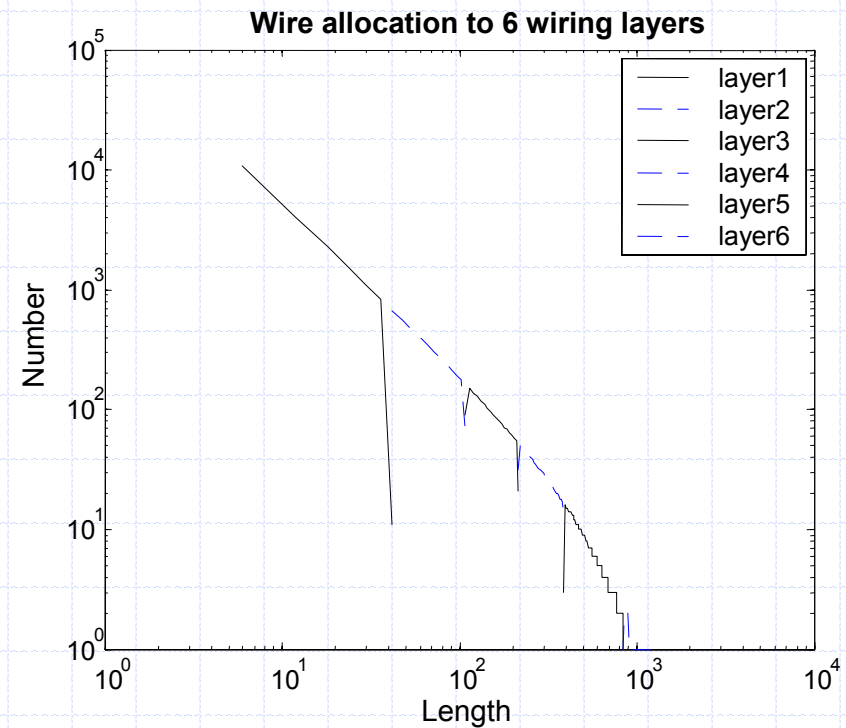
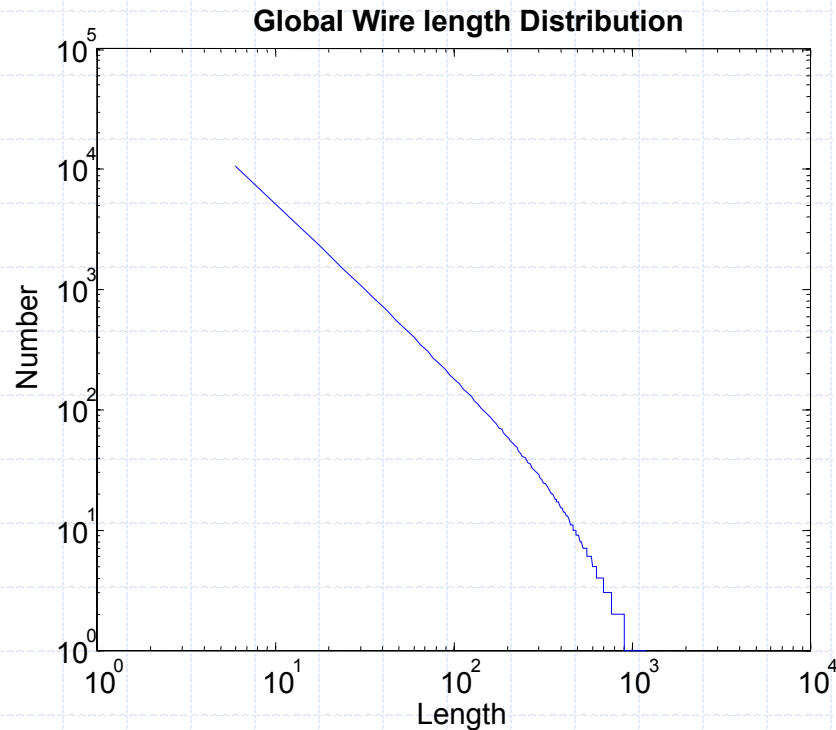


Layer 1

Wire Allocation to Wiring levels

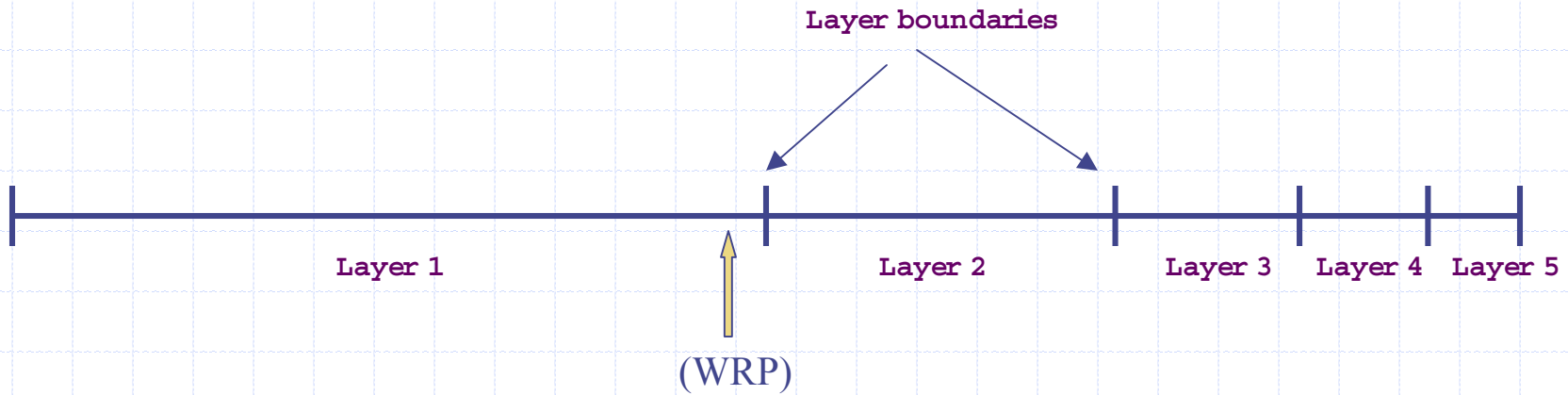
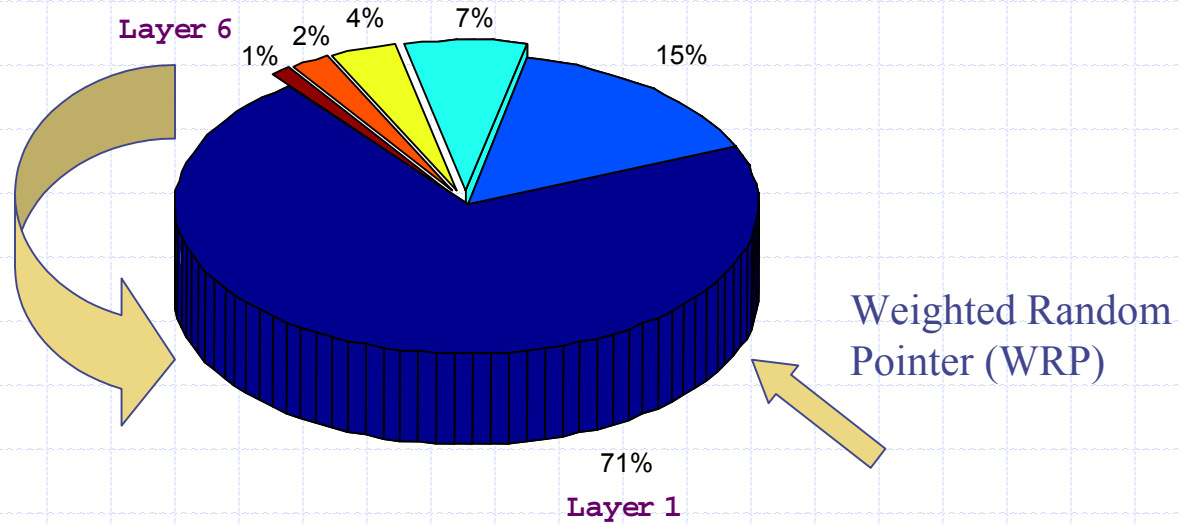
Layer Capacity:

$$C = \eta(n)_r C_{tot} \{w_c h_c / \eta_p p(n)\}$$

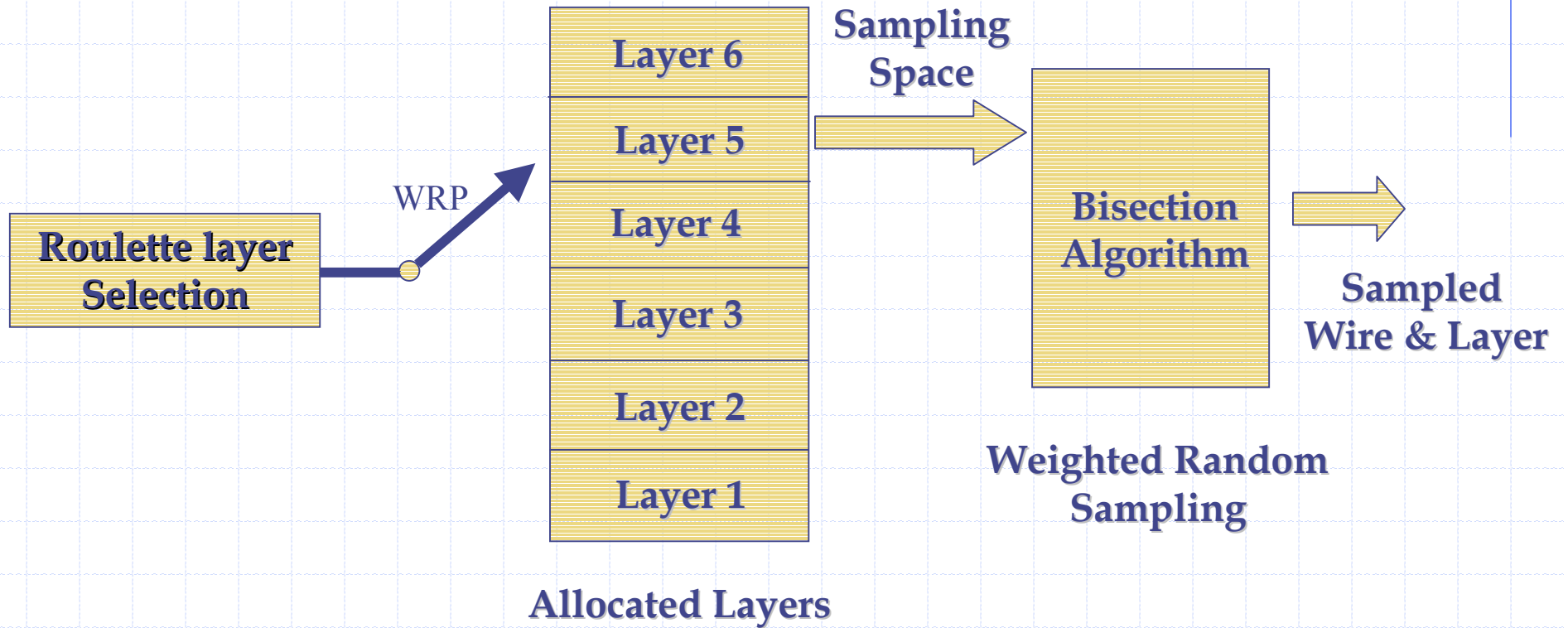


- The global wire length distribution is allocated to a six layer process.
- Pseudo - Routing renders an *allocated distribution* which is used in wire sampling

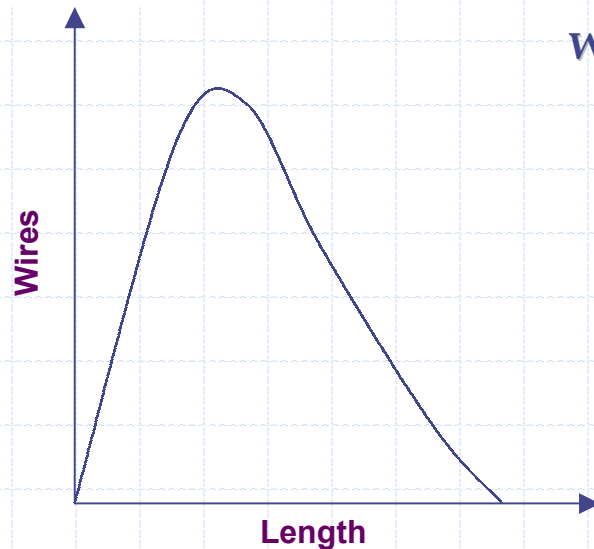
The Roulette - Layer Selection



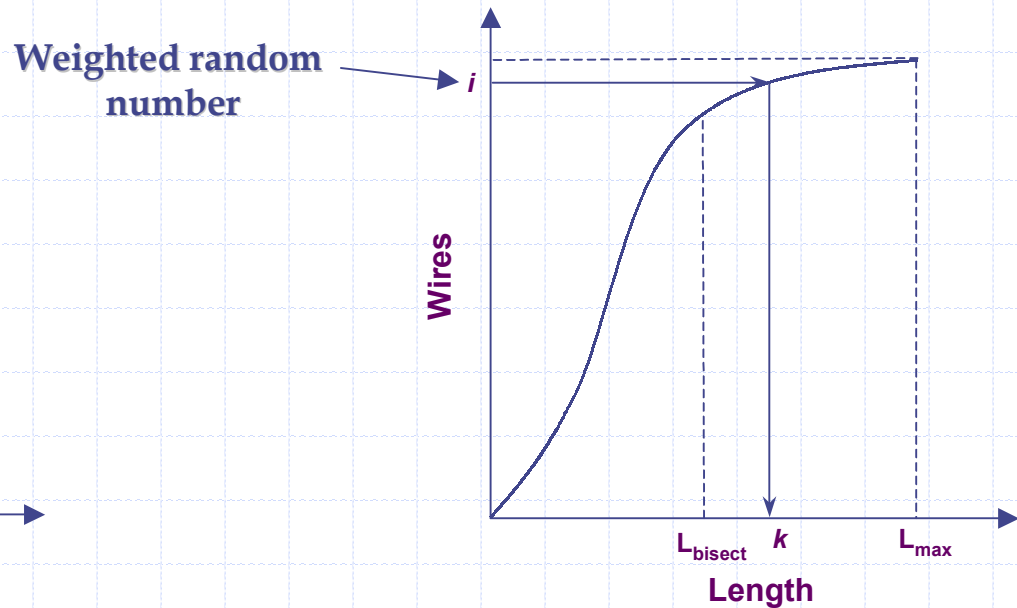
Weighted Random Sampling



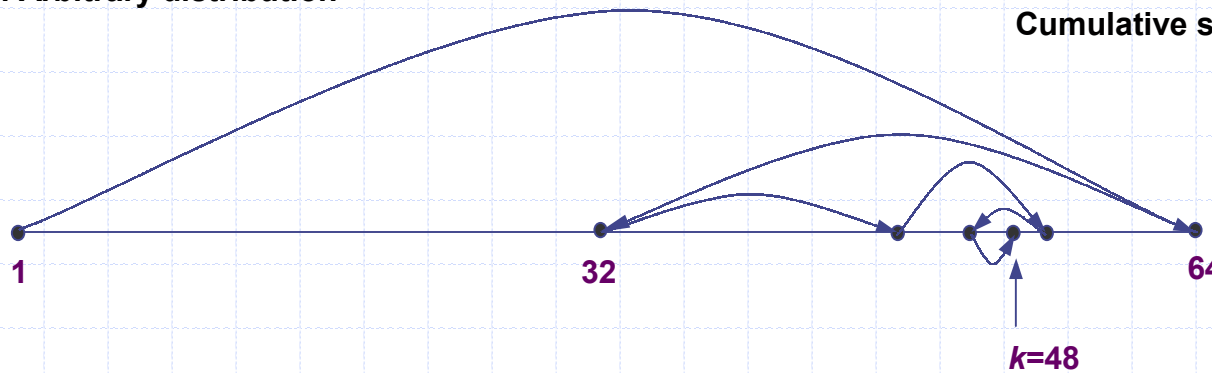
The Bisection Algorithm



An Arbitrary distribution

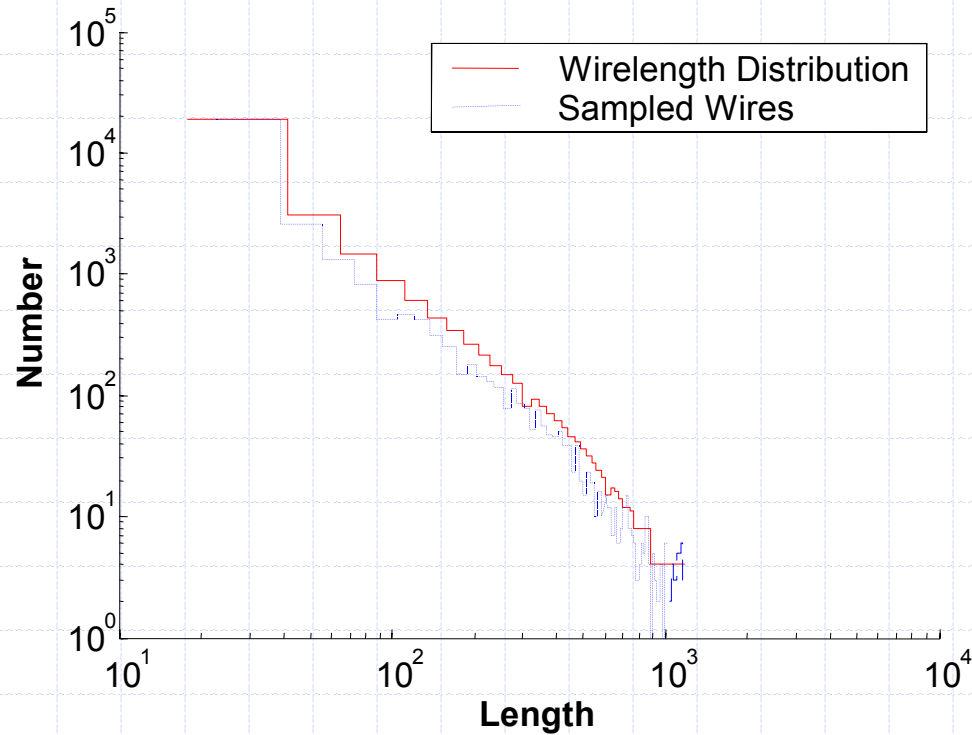


Cumulative sum



- Efficient Search Algorithm for heavily skewed distributions.
- Search process requires $O(\log N)$ steps
- The Algorithm is searching for the value 48.

Distribution Recovery Test



- Wire allocation, layer selection and Wire sampling algorithms work together to recover approximately the Actual Wire length.
- The weighted random sampling of wires reflects the behavior of actual wire length distribution with reasonable accuracy.

The Setup

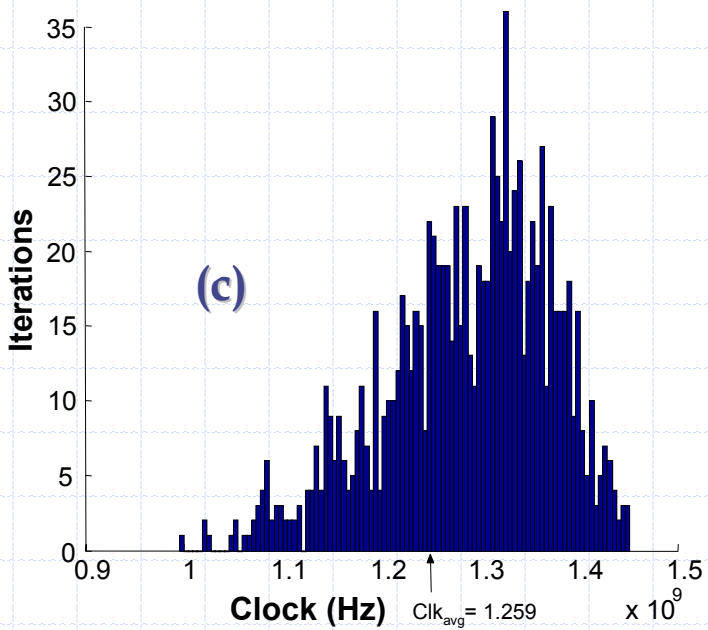
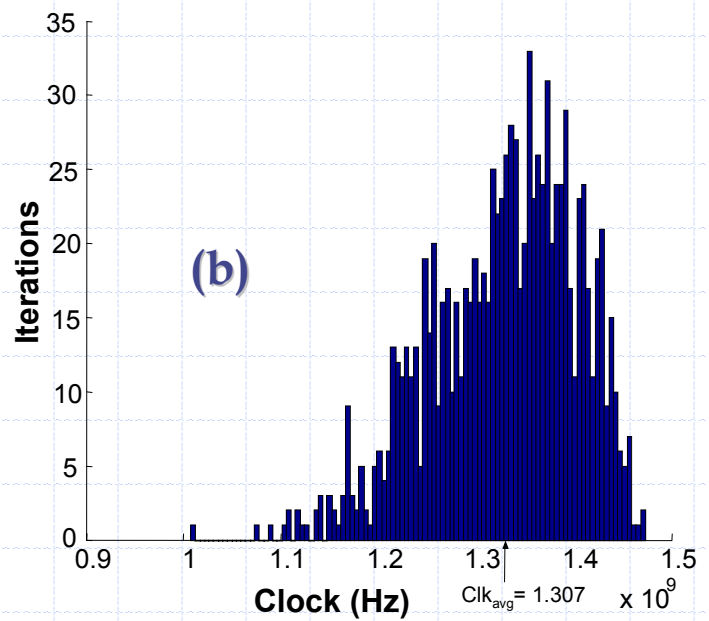
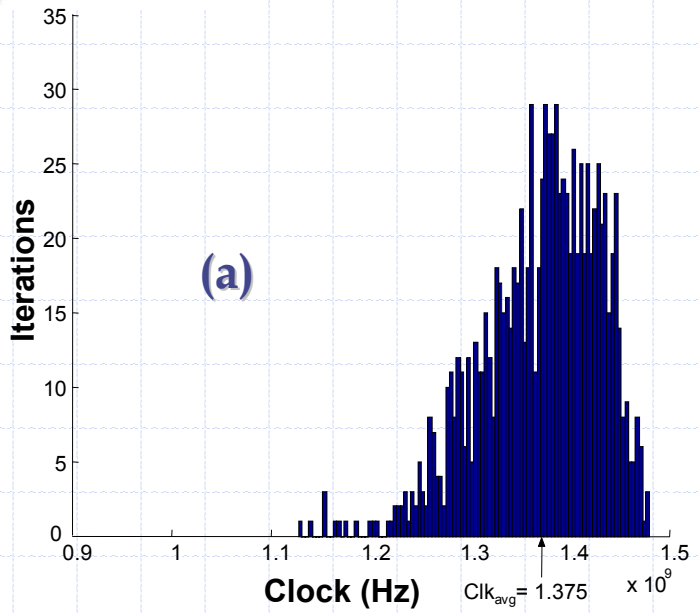
- Cycle Time Estimates with
 1. Local Delays (Excluding t_{global} term in Sakurai Equation)
 2. Local and Global Delay (Including t_{global})

Cycle time:

$$t_{\text{cycle}} = \frac{t_{\text{local}} + t_{\text{global}} + t_{\text{setup}} + t_{\text{flip-flop}}}{1\text{-skew}}$$

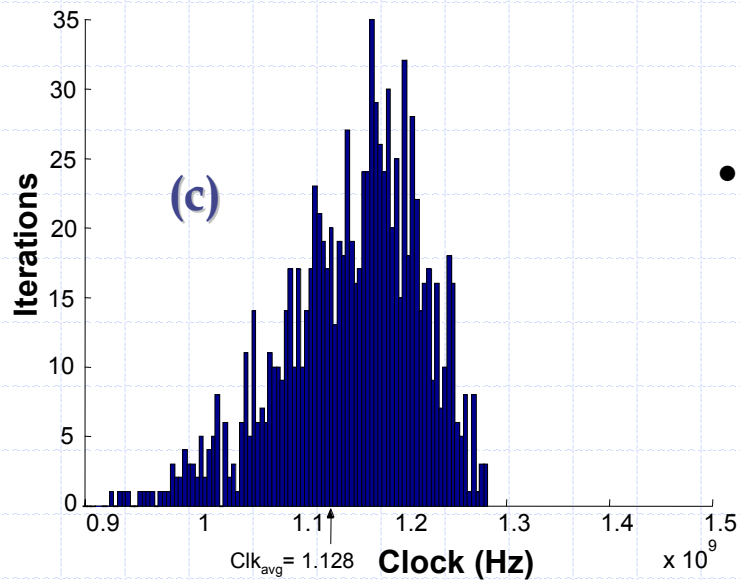
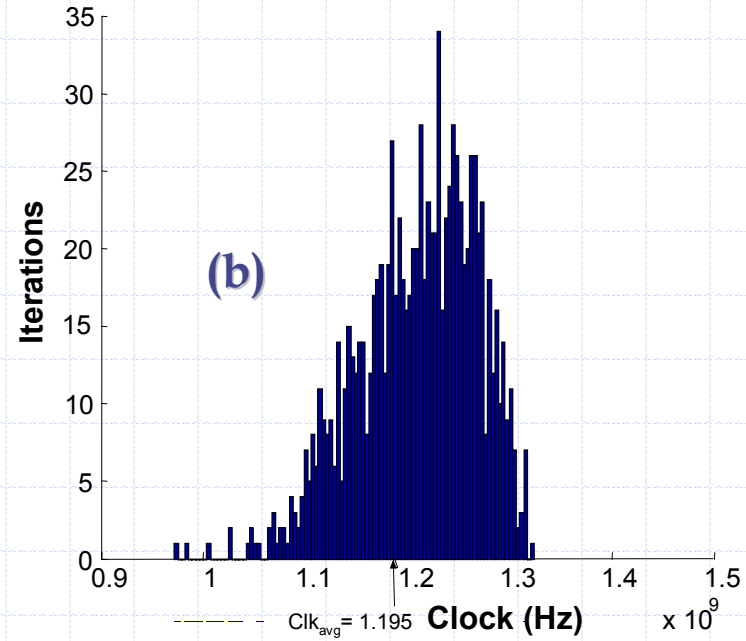
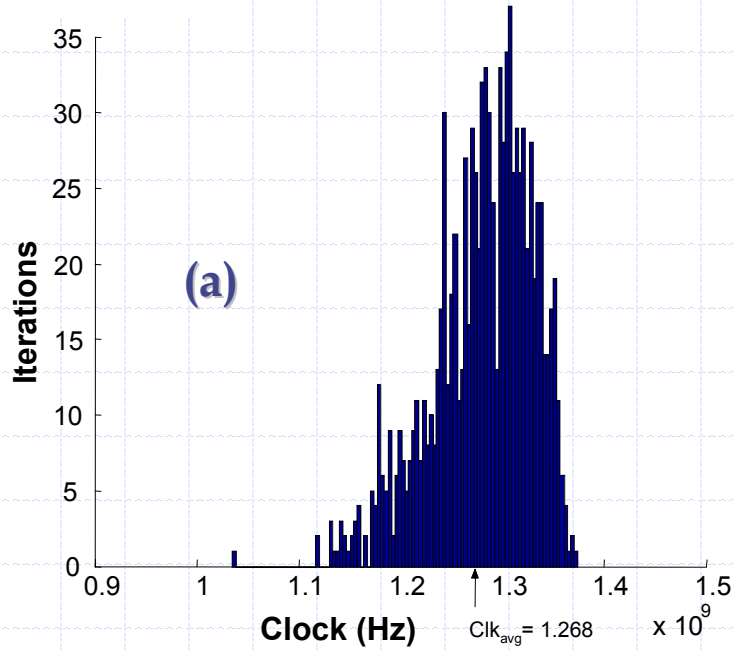
- Fixed Fan Out range from 1 to 3.
- Calculation of Clk_{avg} (based on Mean Value model).
- Each Experiment was run of 1000 trials for above conditions

Results - Local Estimates



- 1000 trials of clock rate estimates based on stochastic *local delay* with fixed FanOut of (a) 1 (b) 2 (c) 3. Clk_{avg} is cycle time estimated using average wire lengths.

Results - Global Estimates



- 1000 trials of clock rate estimates *local delay* and deterministic *global delay* with fixed FanOut of (a) 1 (b) 2 (c) 3. Clk_{avg} is cycle time estimated using average wire lengths.

Local Clock Estimate

Statistical Analysis	Fanout 1	Fanout 2	Fanout 3
Standard Deviation (Ghz)	0.0573	0.0731	0.8266
Mean (Ghz)	1.3740	1.3276	1.2860
Clk _{avg} (Ghz)	1.3751	1.3070	1.2598

Global Clock Estimate

Statistical Analysis	Fanout 1	Fanout 2	Fanout 3
Standard Deviation (Ghz)	0.0495	0.0574	0.0679
Mean (Ghz)	1.2805	1.2096	1.1499
Clk _{avg} (Ghz)	1.2683	1.1951	1.1298

- Fixed FanOut Vectors ranging from 1 to 3 shows a decreasing mean clock rate and increasing Standard Deviation with increasing FanOuts.
- Including a wire of maximum length (Global Estimates) reduces mean clock rate with relative reduction in standard deviation.
- The Clk_{avg} values based on mean value model lies in close vicinity of mean clock rate estimated for each set of experiments.

- The scheme is suitable for investigating variable geometries in multi-layer wiring schemes.
- The estimates have an expected mean value and a standard deviation of approximately 5 %.
- The median *global* clock rates do not differ significantly from *local* rates.
- There is a sharp fall in the clock rate distribution after the median values.
- The scheme gives a measure of distribution *skewness*, thereby modeling the inherent stochastic nature of layout process.
- The Clk_{avg} being in close vicinity of the median rates, validates the appropriateness of the mean value model for logic depth of 25.