Prediction of Interconnect Pattern Density Distribution: Derivation, Validation, and Applications

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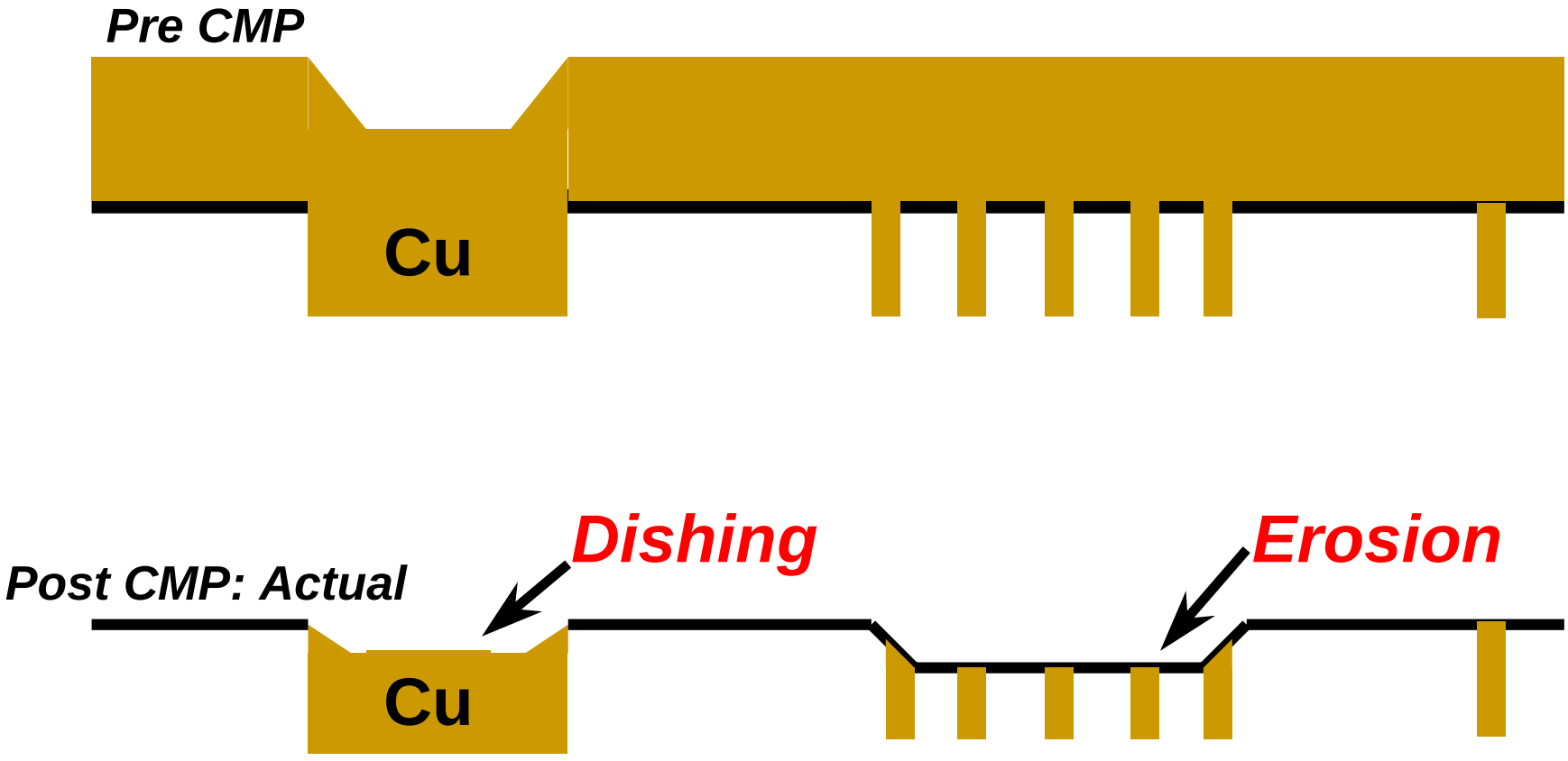
Outline

- **Motivation**
- **Interconnect Pattern Density Model**
  - **Derivation**
  - **Validation**
  - **Applications**
- **Conclusion**

Motivation

- **Large variation (+/- 30%) in metal thickness.**
- **Mostly due to effect of metal coverage (*Pattern Density)* on CMP process.**
- **Interconnect thickness variation becomes layout dependent, which makes it impossible to perform a system level analysis without a completed layout.**
- **Prediction of interconnect pattern density distribution is essential in understanding the limitations of a future technology *without* prior access to the layout details.**

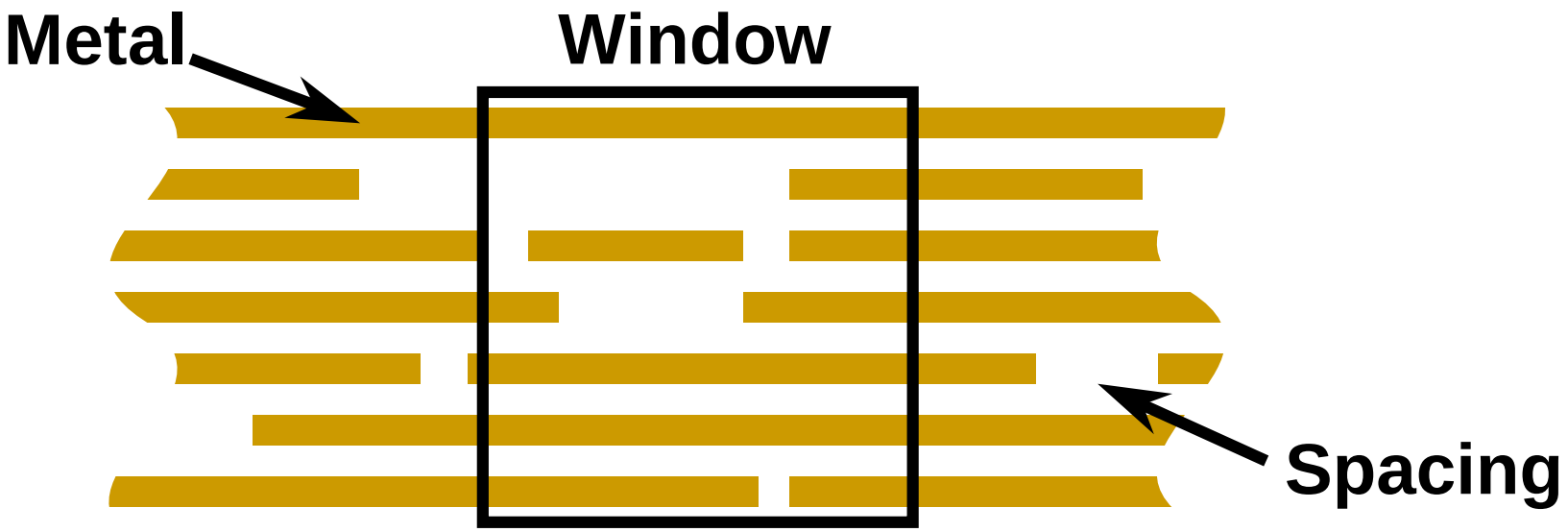
Topography After Copper CMP



Courtesy of S. Lakshminarayanan of LSI Logic

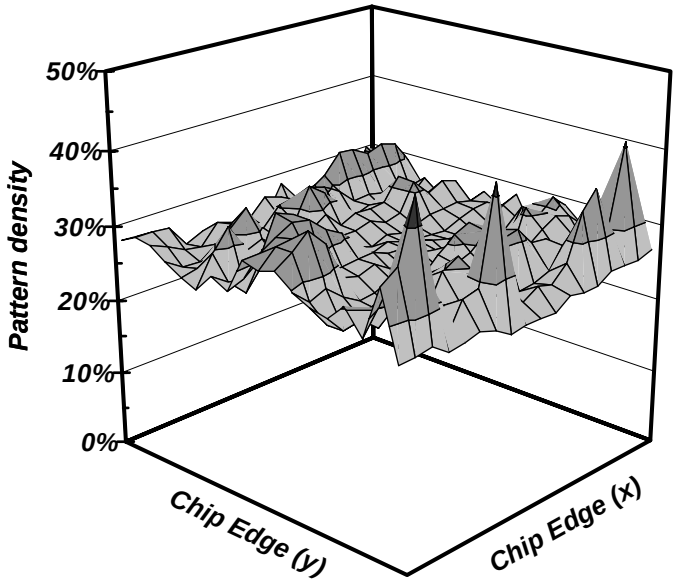
Pattern Density Definition

Interconnect pattern density (IPD) is the fractional area occupied by the metal interconnects within a window of given size.

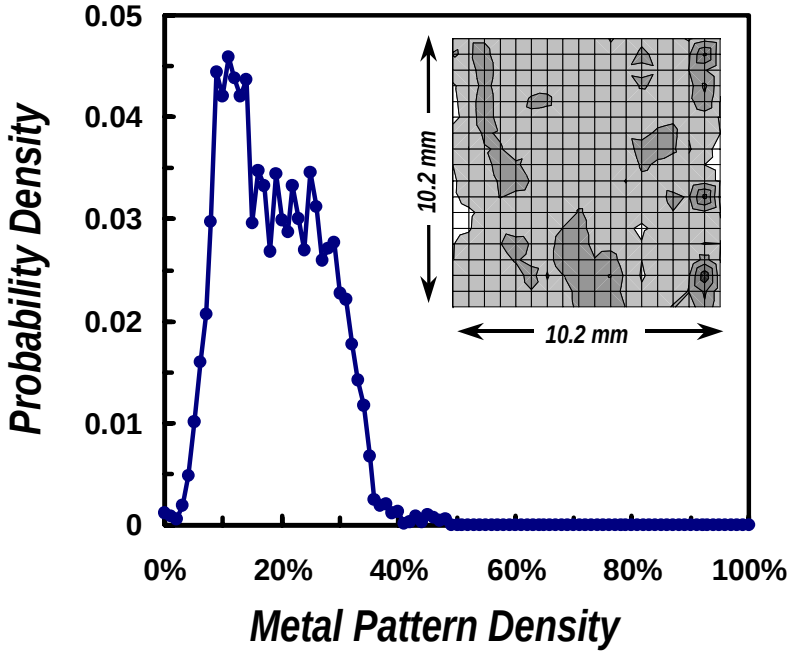


IPD = Metal Coverage = 38%

IPD Probability Density Function



A 3-D Pattern Density Distribution



Interconnect Pattern Density PDF

Design Specifications:

Metal Layer = M2	Window Size = 100×100 μm^2
Chip Size = 10×10 mm^2	Technology = 0.18 μm
No. of Gates = 2.5 M gates	Total Metal Layers = 5

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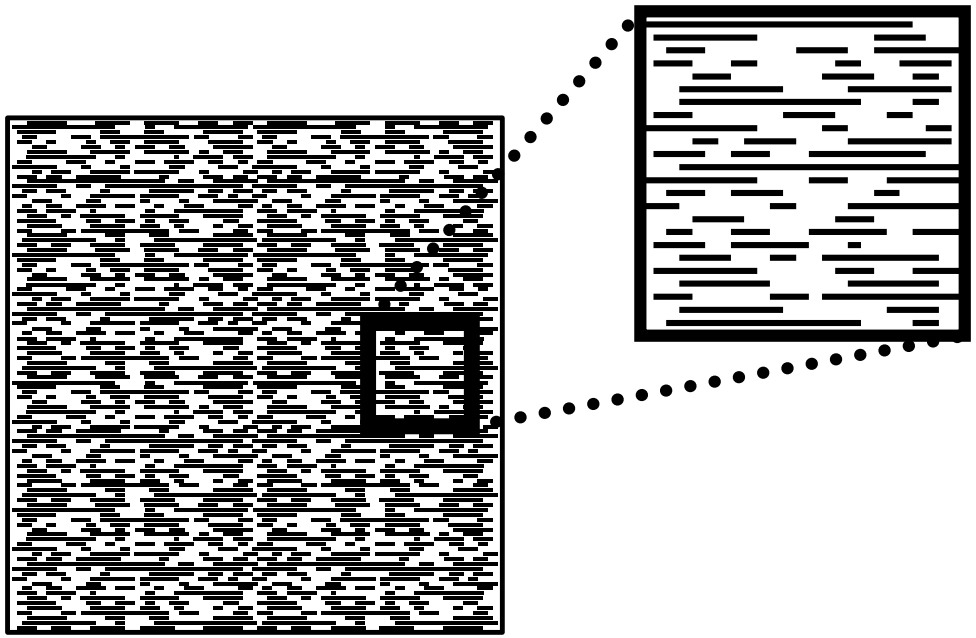
Assumption 1

- **Random logic network is complex and irregular enough to be well approximated by a random variable.**
- ***P* = Wire placement probability (channel utilization).**



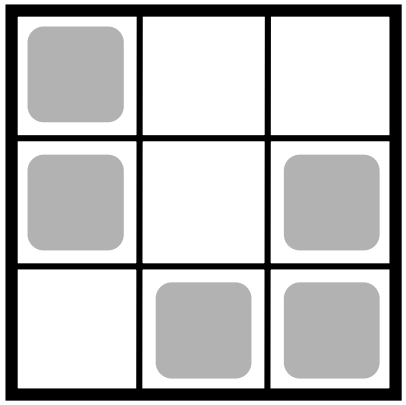
Simple Example

Simplified problem:

Array size, *n* = 3x3

Probability of placing a dot, *p* = 0.75

Probability of having 5 dots, *f(5)* = ?

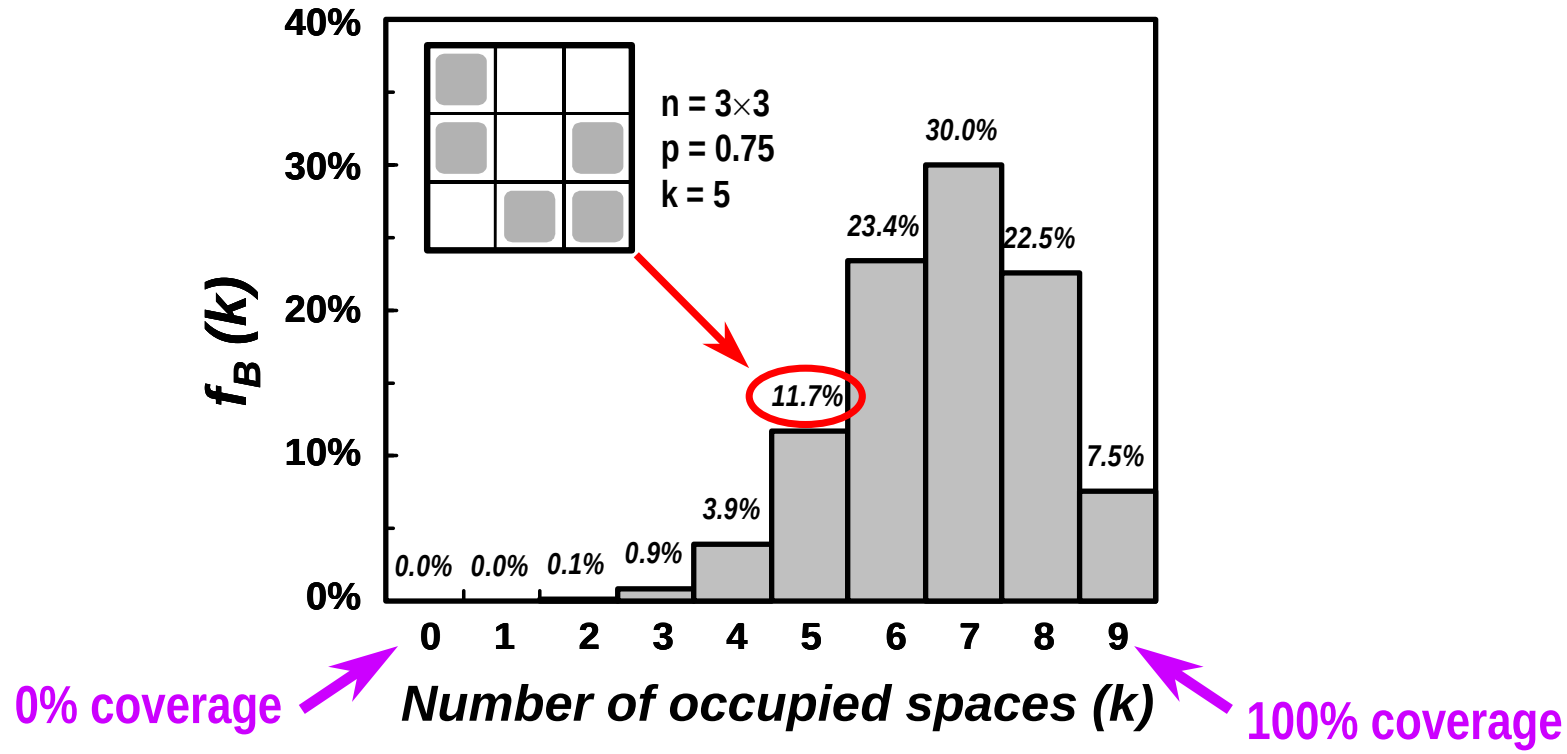


$$f(5) = \frac{9!}{5! \times 4!} (0.75)^5 (0.25)^4$$

$$f(5) = 11.7\%$$

Bernoulli Probability Function

Basic IPD Distribution

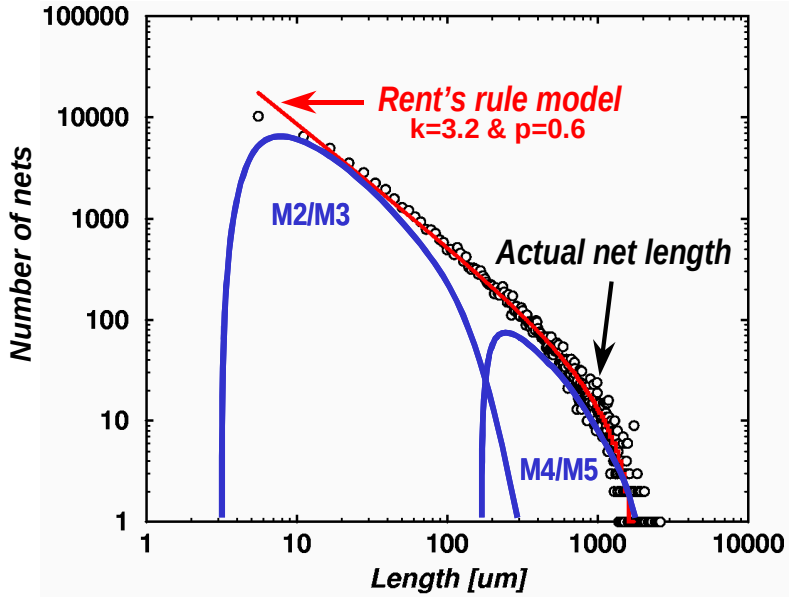


Bernoulli probability function:

$$f_B(k) = \frac{n!}{k! \times (n-k)!} p^k (1-p)^{n-k}$$

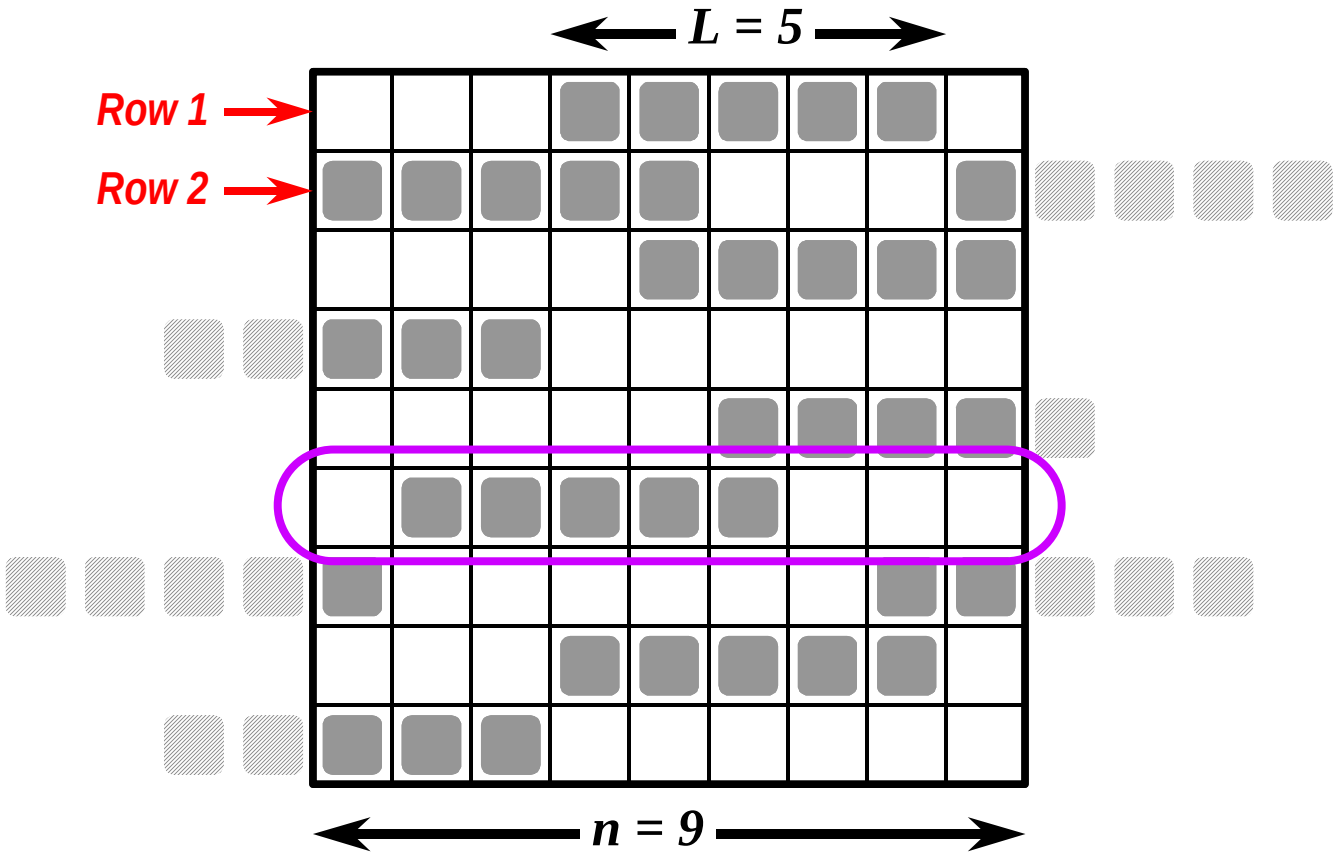
Assumption 2

- We use average wire length in each metal layer.
- It is computed by wire allocation to that metal layer
  [P. Christie and J. Gyvez, SLIP 2001].

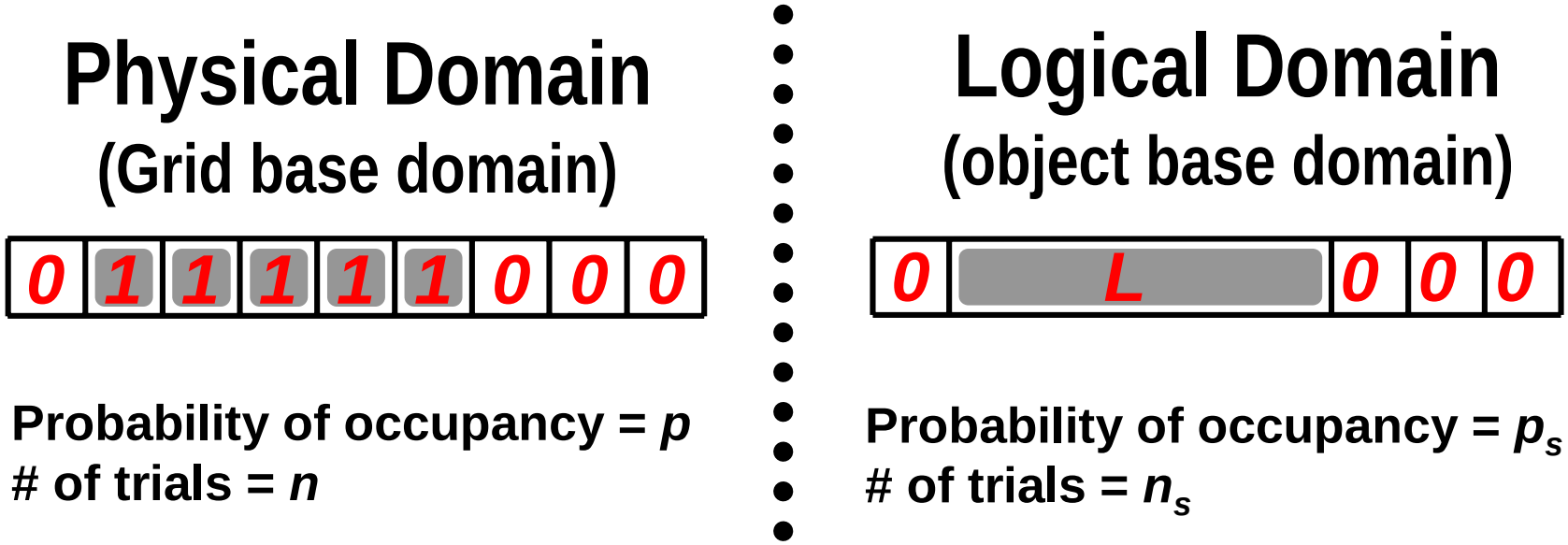


Courtesy of Weidan Li of LSI Logic

Realistic Case



Physical versus Logical Domains



- We map the problem in physical domain to logical domain to be able to use Bernoulli distribution.
- Then, we map the results back to the physical domain.

Physical versus Logical Domains

Physical Domain
(Grid base domain)

Probability of occupancy = p
# of trials = n

Logical Domain
(object base domain)

Probability of occupancy = p_s
# of trials = n_s

# of filled spaces: $np = L(n_s p_s)$

# of empty spaces: $n(1-p) = n_s(1-p_s)$

Physical versus Logical Domains

Physical Domain
(Grid base domain)

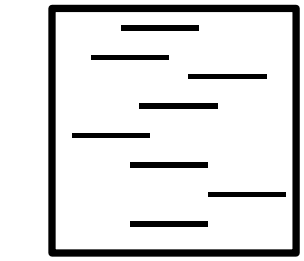
Probability of occupancy = p
# of trials = n

Logical Domain
(object base domain)

Probability of occupancy = p_s
# of trials = n_s

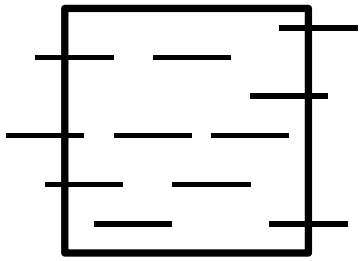
$$\frac{1}{1+(1/p-1)L} = p_s$$

Interconnect Pattern Density of Row



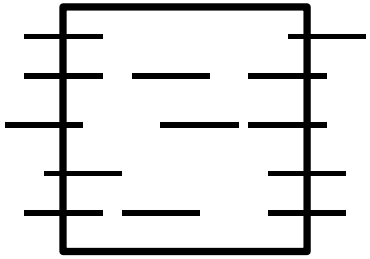
Fully inside (no crossing)

a) $P_0(k)$



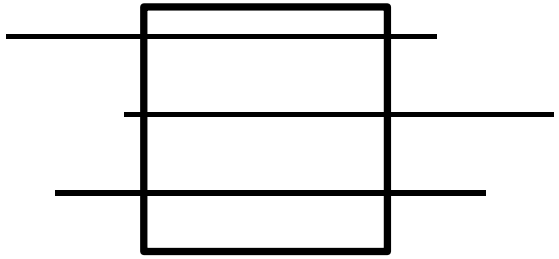
Single side crossing

b) $P_1(k)$



Double side crossing

c) $P_2(k)$



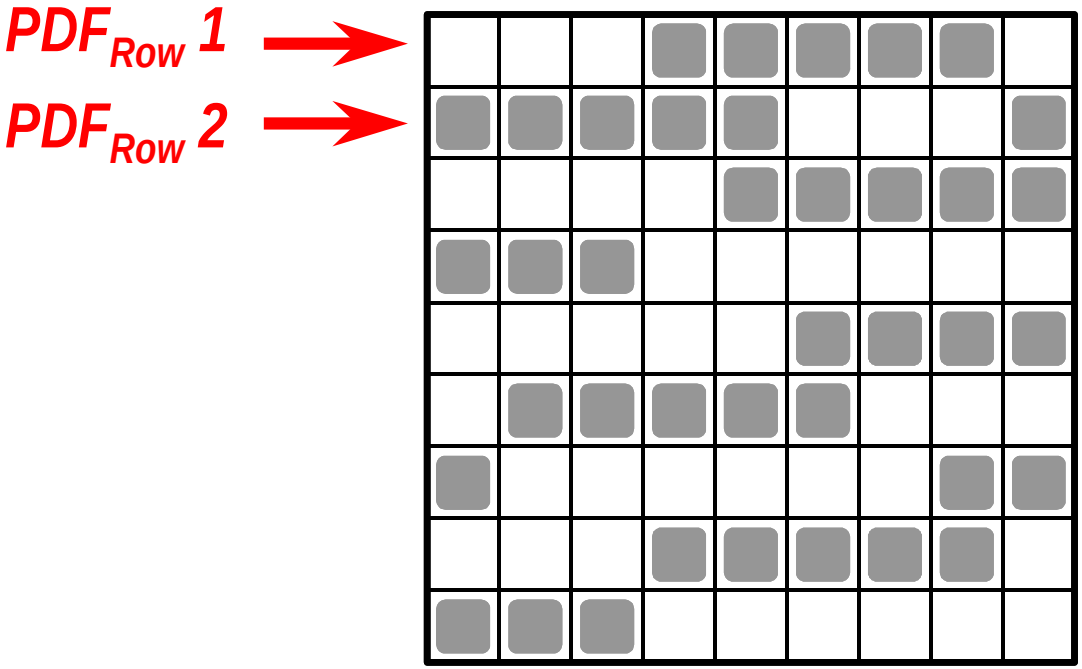
All the way going through

d) $P_3(k)$

$$P_{Row}(k) = P_0(k) + P_1(k) + P_2(k) + P_3(k)$$

$$PDF_{Row}(k) = norm(P_{Row}(k))$$

Overall IPD distribution



$$IPD(k) = PDF_{Row} * PDF_{Row} * .... * PDF_{Row}$$

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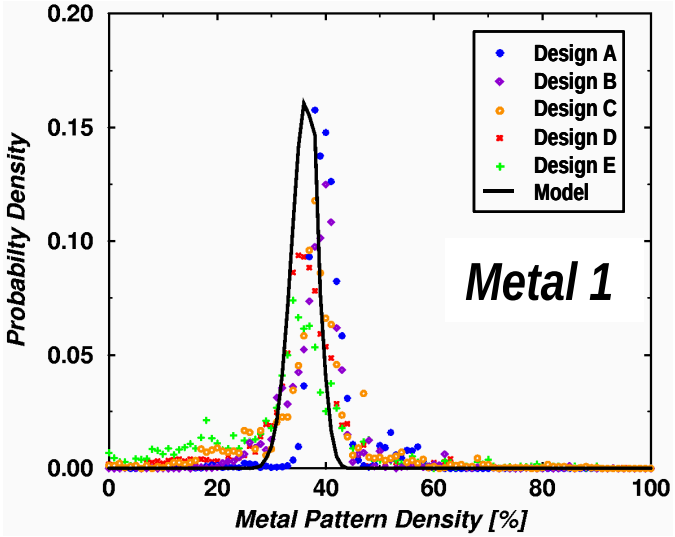
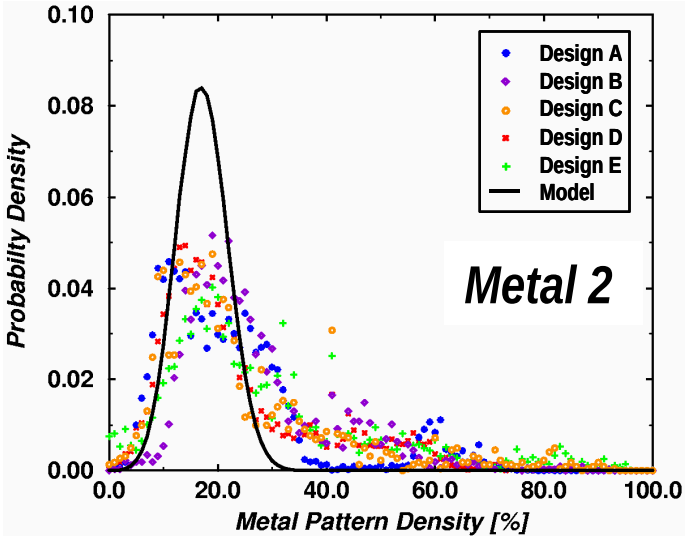
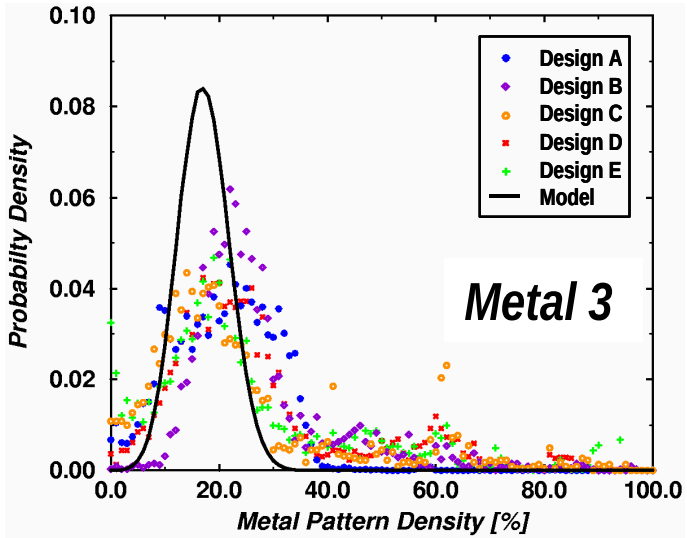
Experimental Data





Input Parameters

1) Window size
2) Average wire-length
3) Wire width and spacing
4) Gate pitch
5) Wiring utilization



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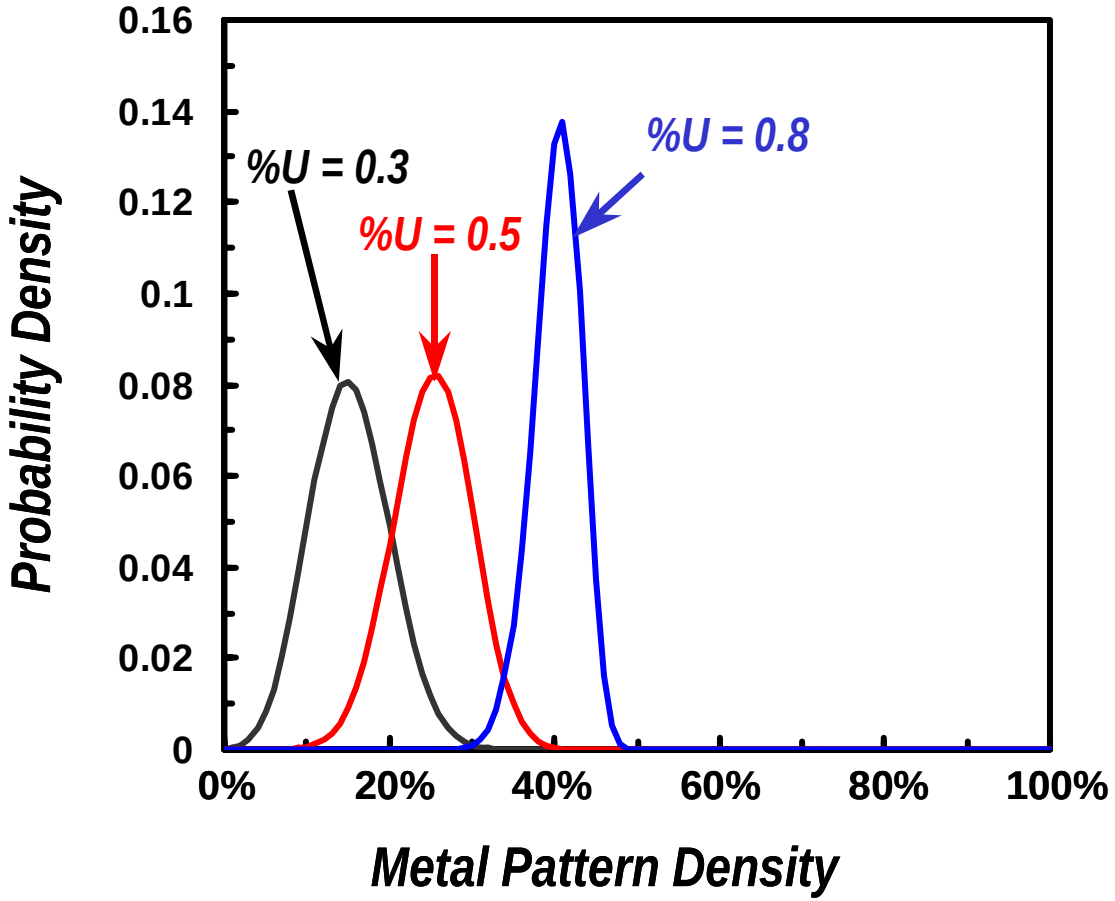
Application 1

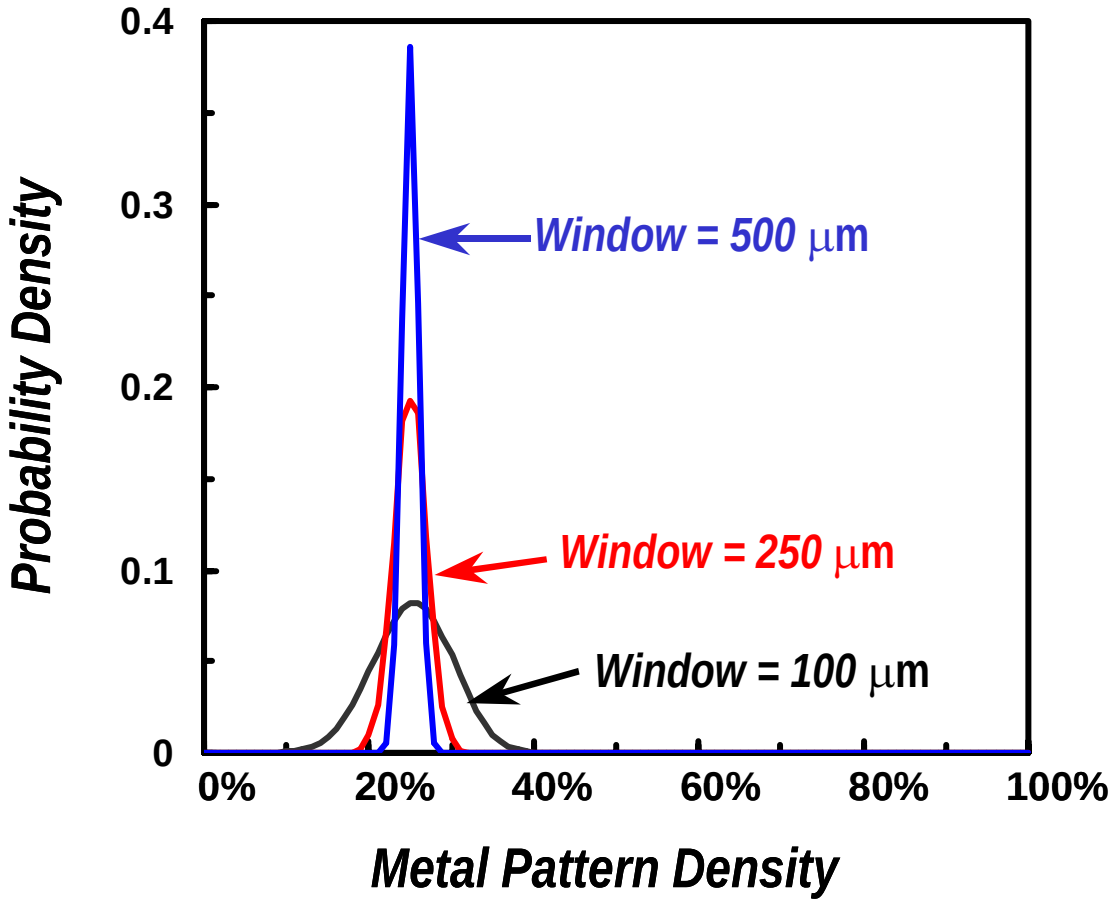
Inference of IPD Distribution

Impact of Channel Utilization



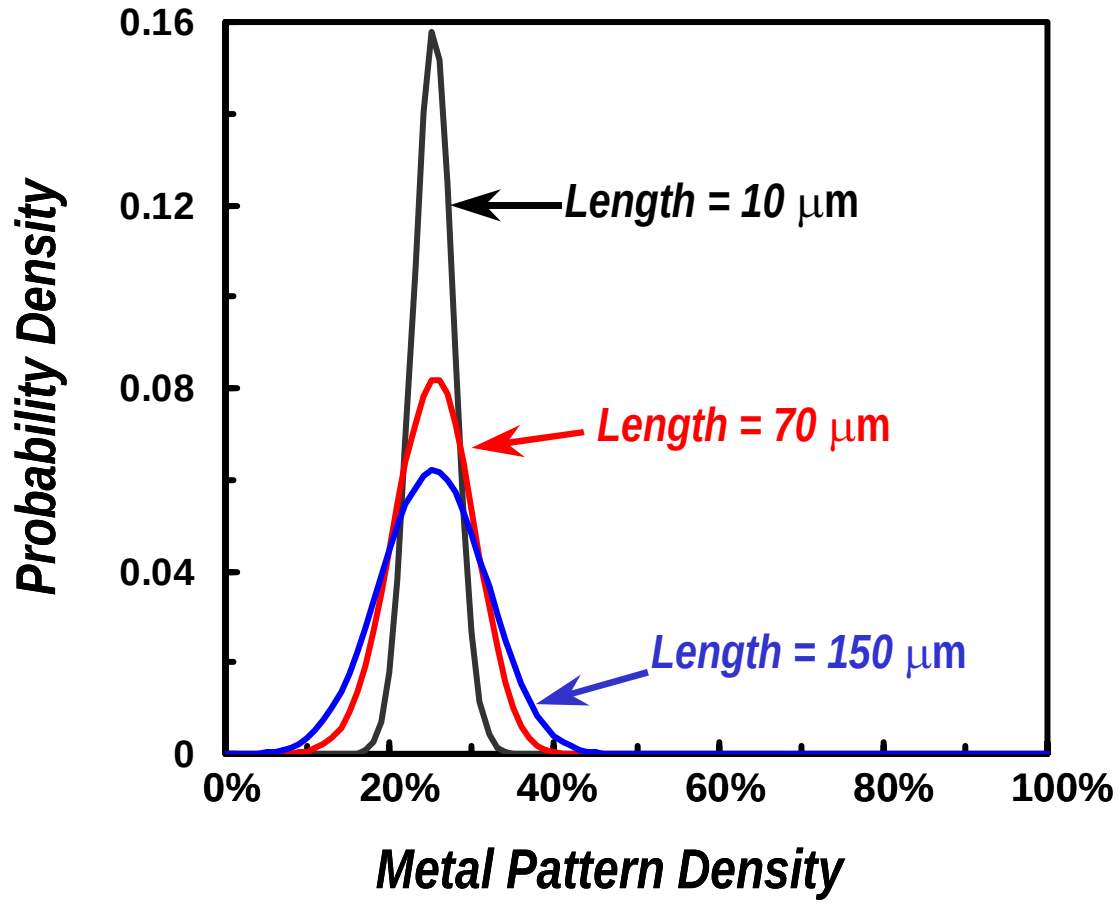
Window = 100 μm
length = 70 μm
width = 0.5 μm
spacing = 0.5 μm
gate pitch = 10 μm

Impact of Window Size



length = 70 μm
width = 0.5 μm
spacing = 0.5 μm
gate pitch = 10 μm
utilization = 0.5

Impact of Wire Length

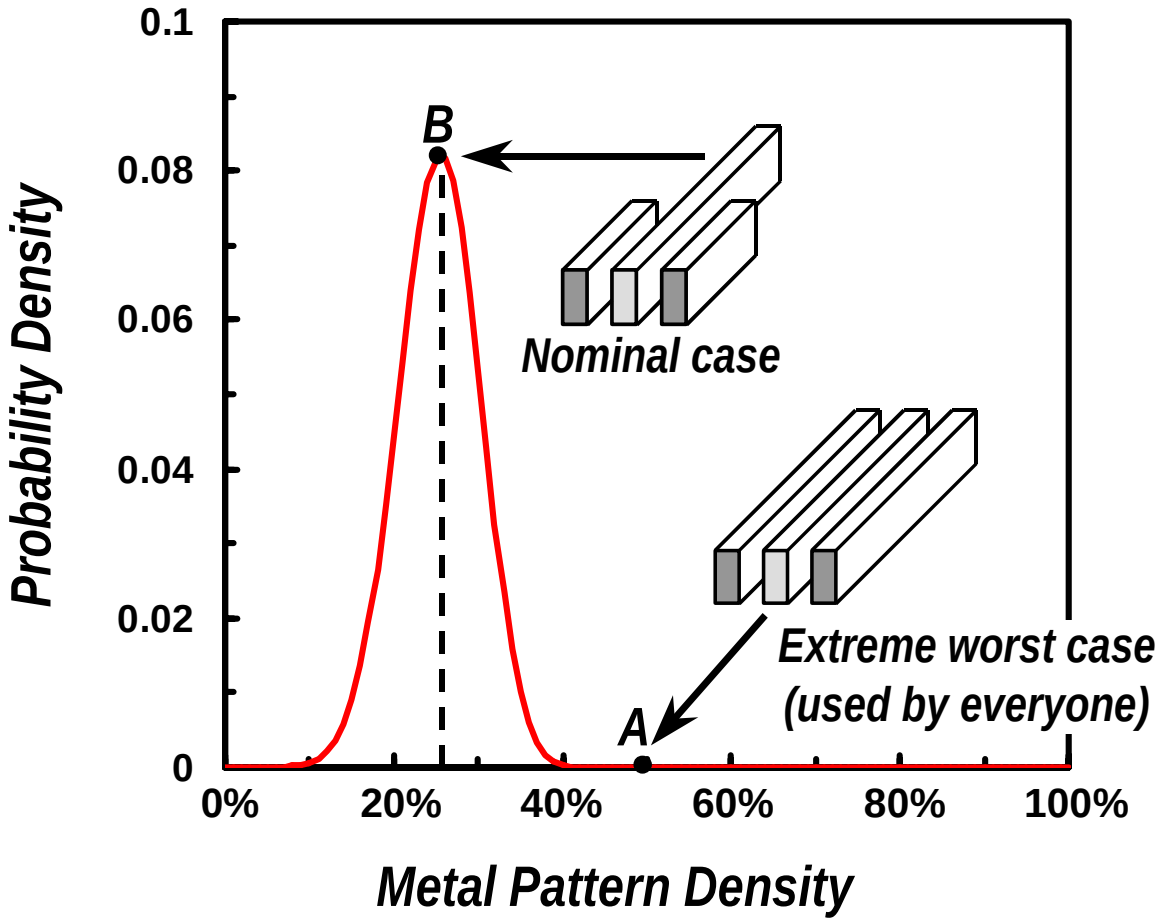


Window = 100 μm
width = 0.5 μm
spacing = 0.5 μm
gate pitch = 10 μm
Utilization = 0.5

Application 2

Statistical Interconnect Reference Circuit

Statistical Interconnect Reference Circuit

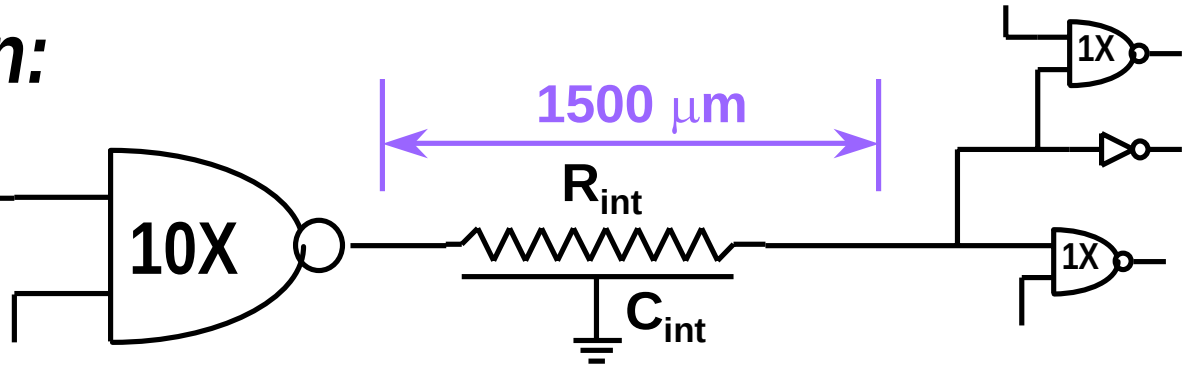


Application 3

Assessing the Impact of IPD on System Performance

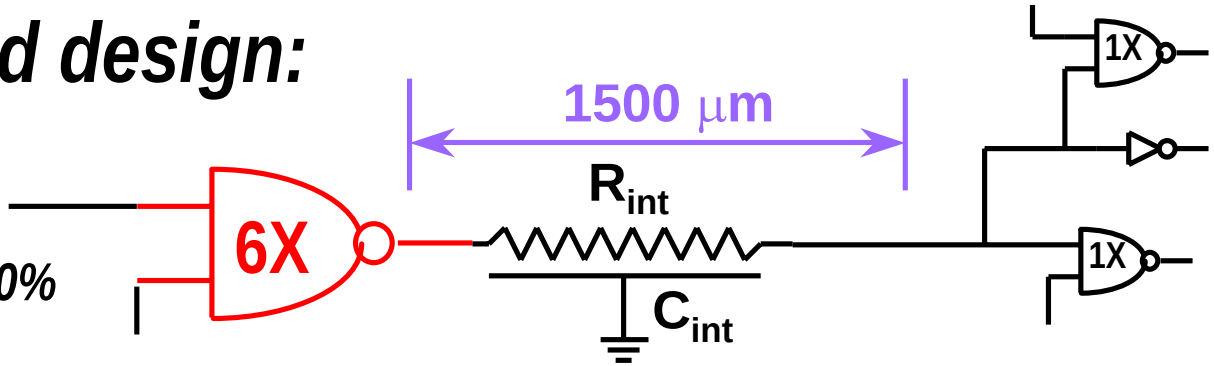
Circuit of a Synthetic Global Net

Over-design:



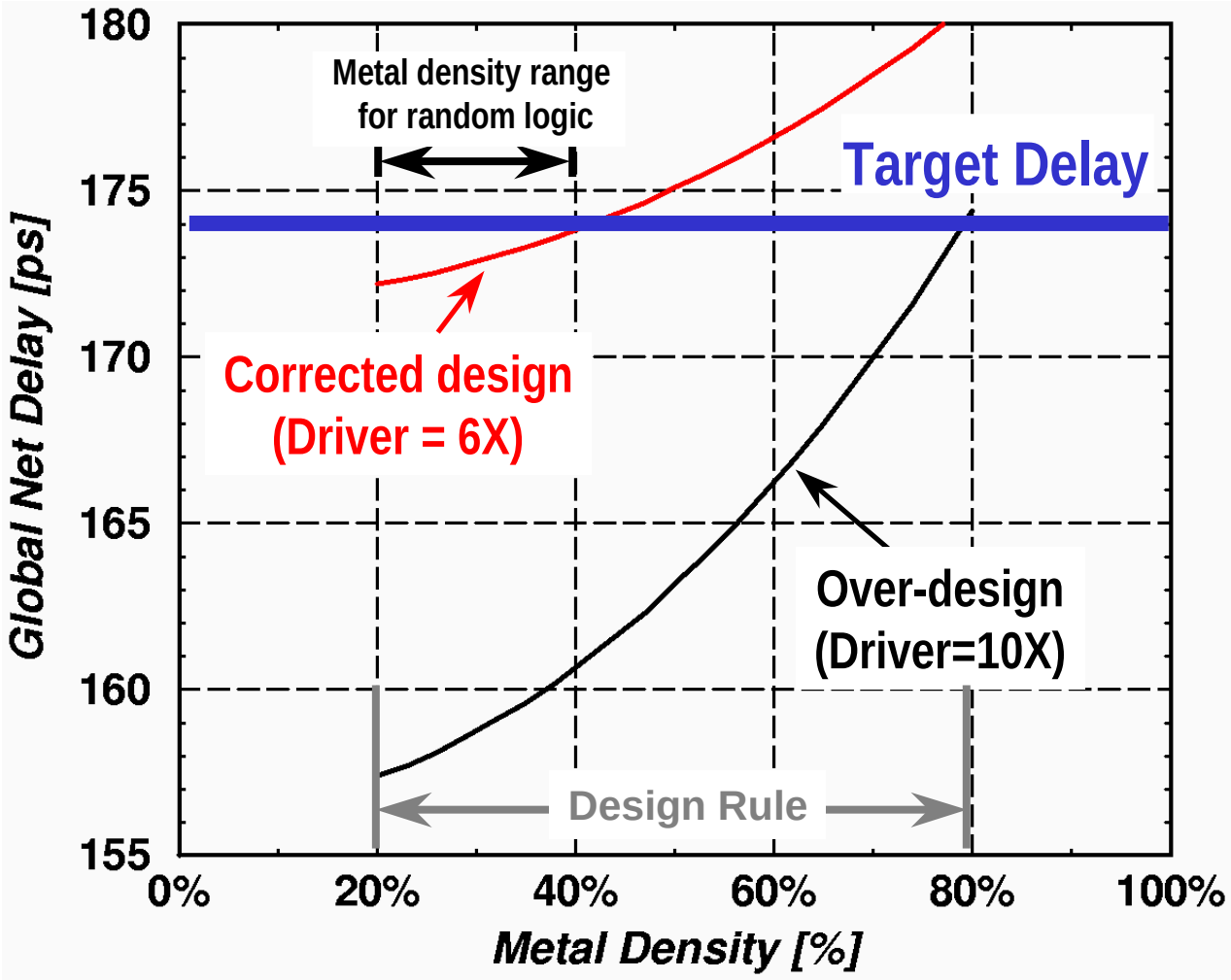
20% < IPD < 80%
Delay < 174ps
Driver size = 10X

Corrected design:



20% < IPD < 40%
Delay < 174ps
Driver size = 6X

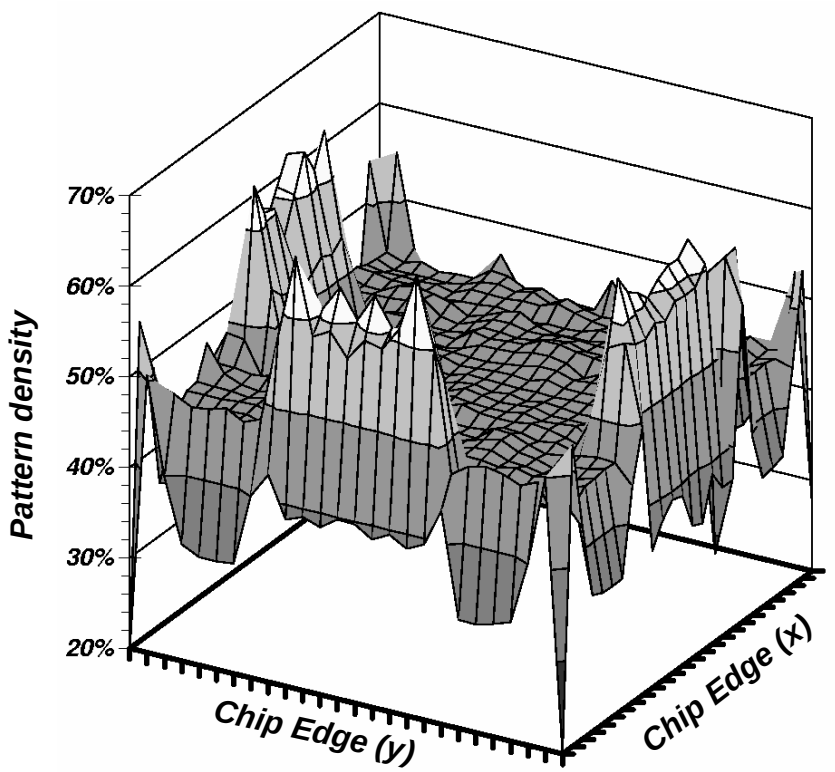
Wire Delay versus Metal Density



Conclusions

- Analytical model for interconnect pattern density (IPD) distribution for random logic networks is derived.
- The model uses only system level generic parameters such as window size, average wire-length, wire width and spacing, gate pitch, and wiring utilization.
- Comparison to product data confirms the accuracy of the model.
- Some possible applications of the IPD are proposed.

Impact of Memory on IPD



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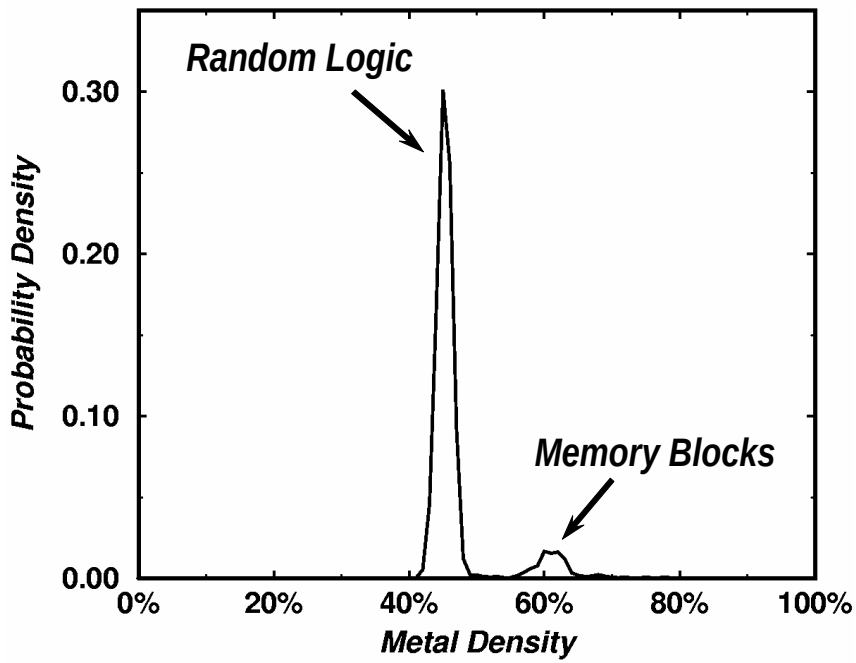

Interconnect Pattern Density PDF