Investigating the Frequency Dependence Elements of CMOS RFIC Interconnects for Physical Modeling

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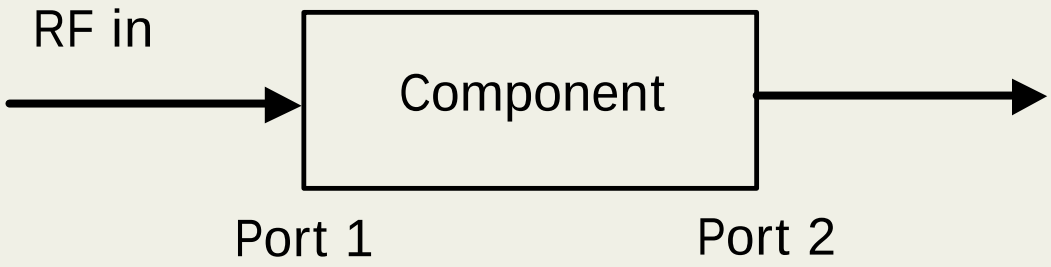
DISCLAIMER!

- Dr. Ong could not come due to compulsory service with the Singapore army
- I (Lou Scheffer) have prepared this summary of the paper, using the paper itself and my correspondence about with him about this paper earlier
- This is my interpretation of the work, not Dr. Ong's.
  - I have been unable to contact him by email for correction, clarifications, etc.
  - He has not even seen, much less blessed, this talk.
- So any mistakes here are my responsibility, and should not be blamed on Dr. Ong

Basic idea

- Use an analog technique called “S parameters” to measure interconnect
- Deduce a SPICE model from these measurements

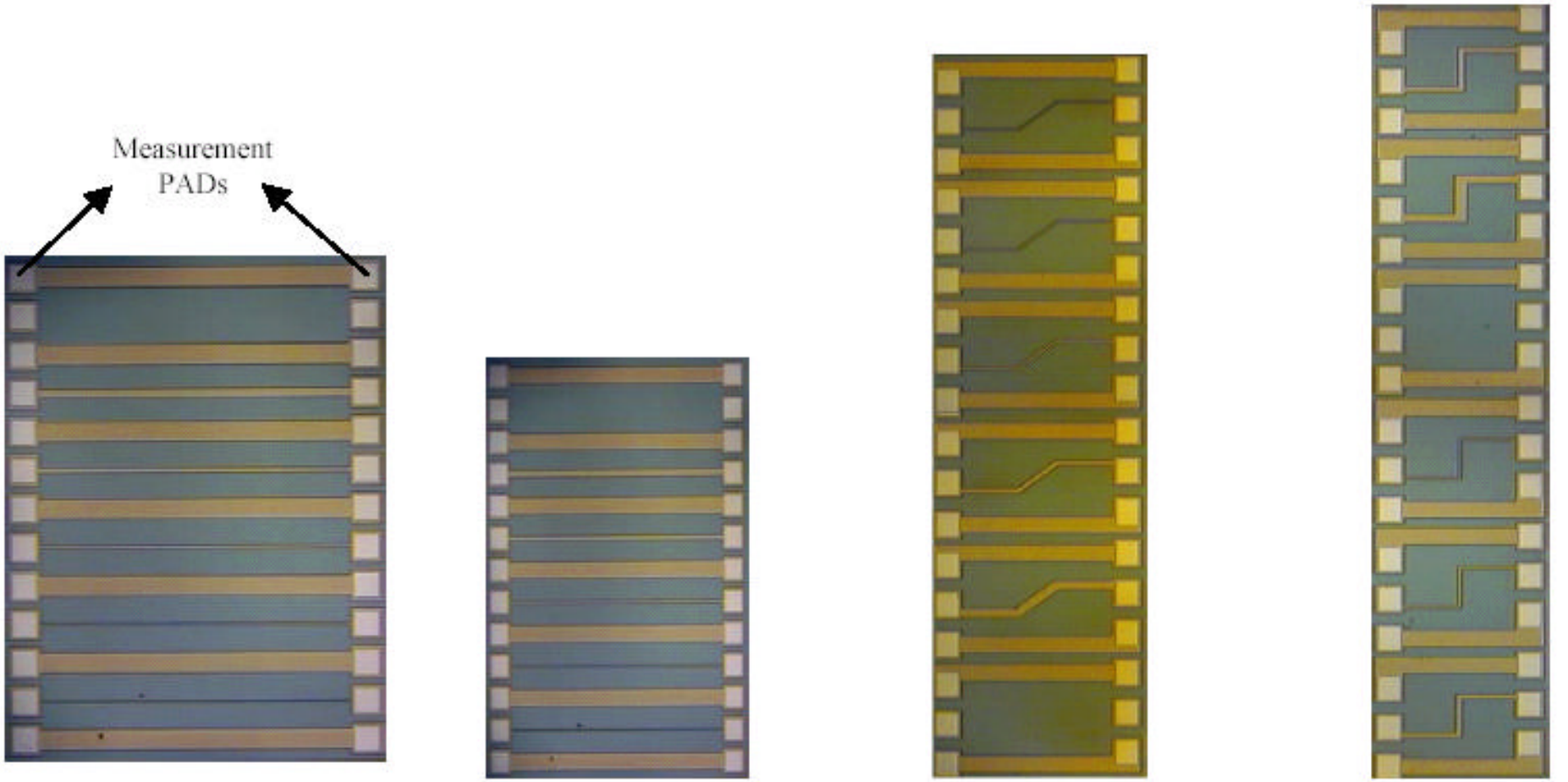


- Some energy is reflected, some absorbed, some transmitted.
  - Reflected is S11 and S22
  - Transmitted is S12 and S21

Why do this?

- Some interconnect values are very hard to measure directly
- Dominated entirely by test fixtures
  - C of wires
  - L of wires
  - Resistance if not at DC
- S parameters can be cascaded, so effect of pads, bonding, etc. can be removed
  - Called “de-embedding”

What they built and measured



(a) 800um straight line (b) 400um straight line (c) 45 degree line (d) 90 degree line

Figure 2: Interconnects test structures fabricated for the study in the work

Layer Thicknesses

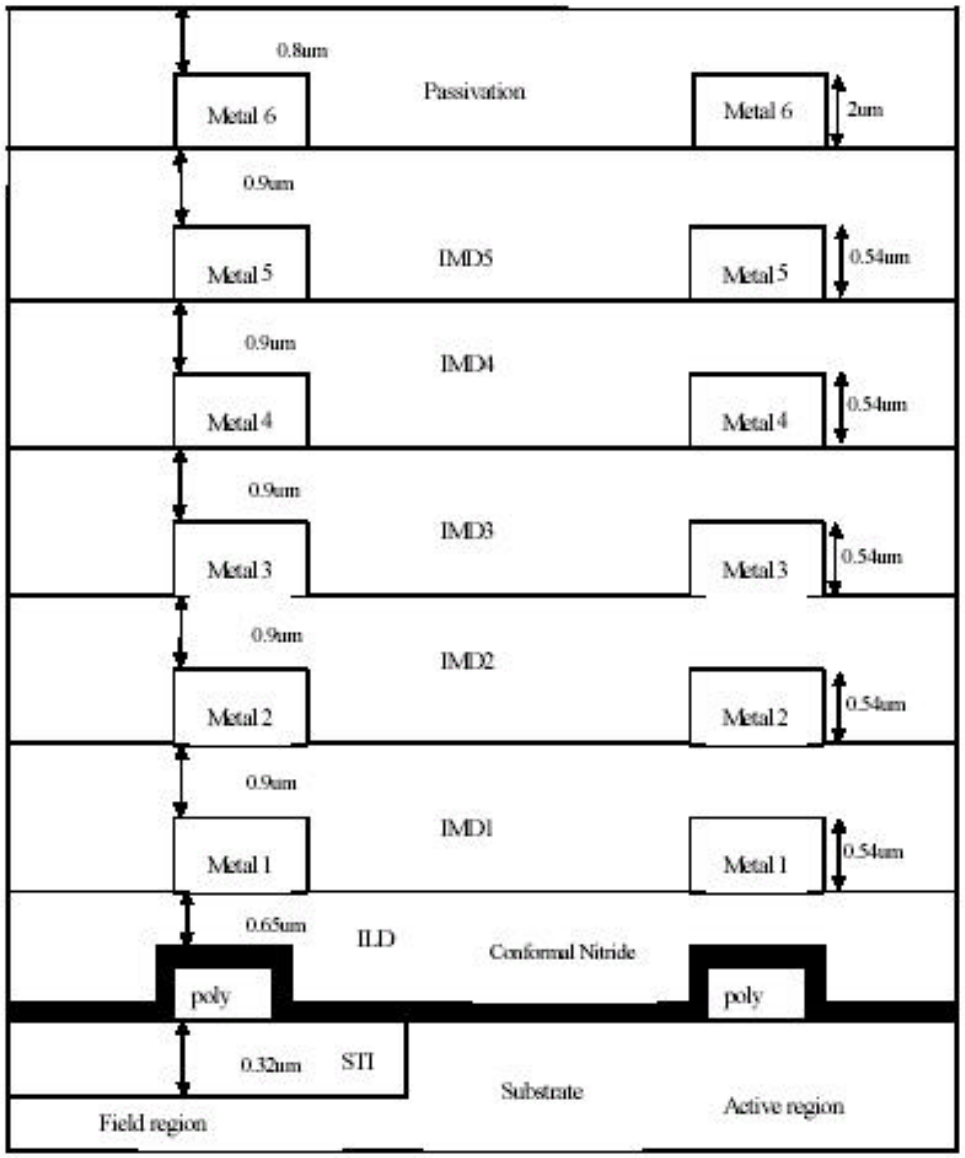
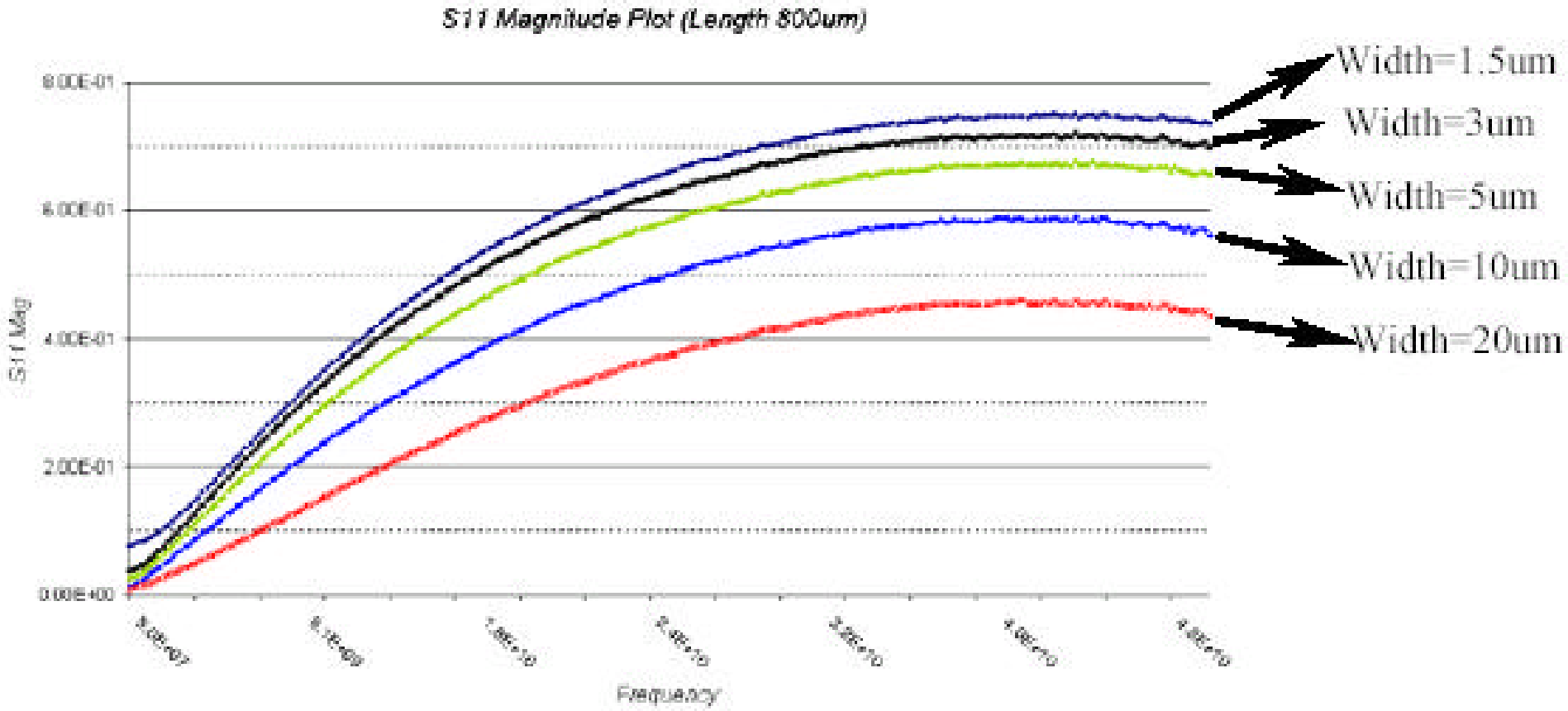
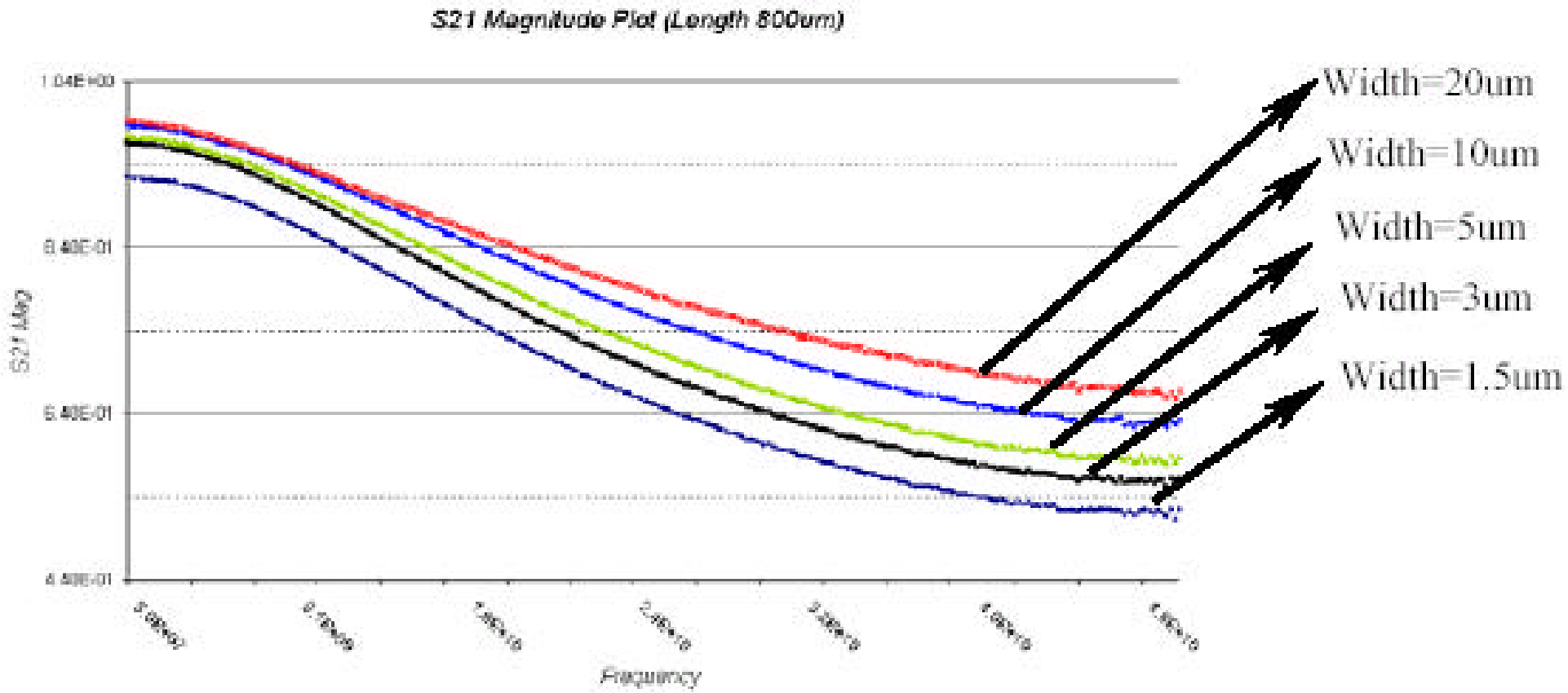


Figure 1: CMOS interconnect stack

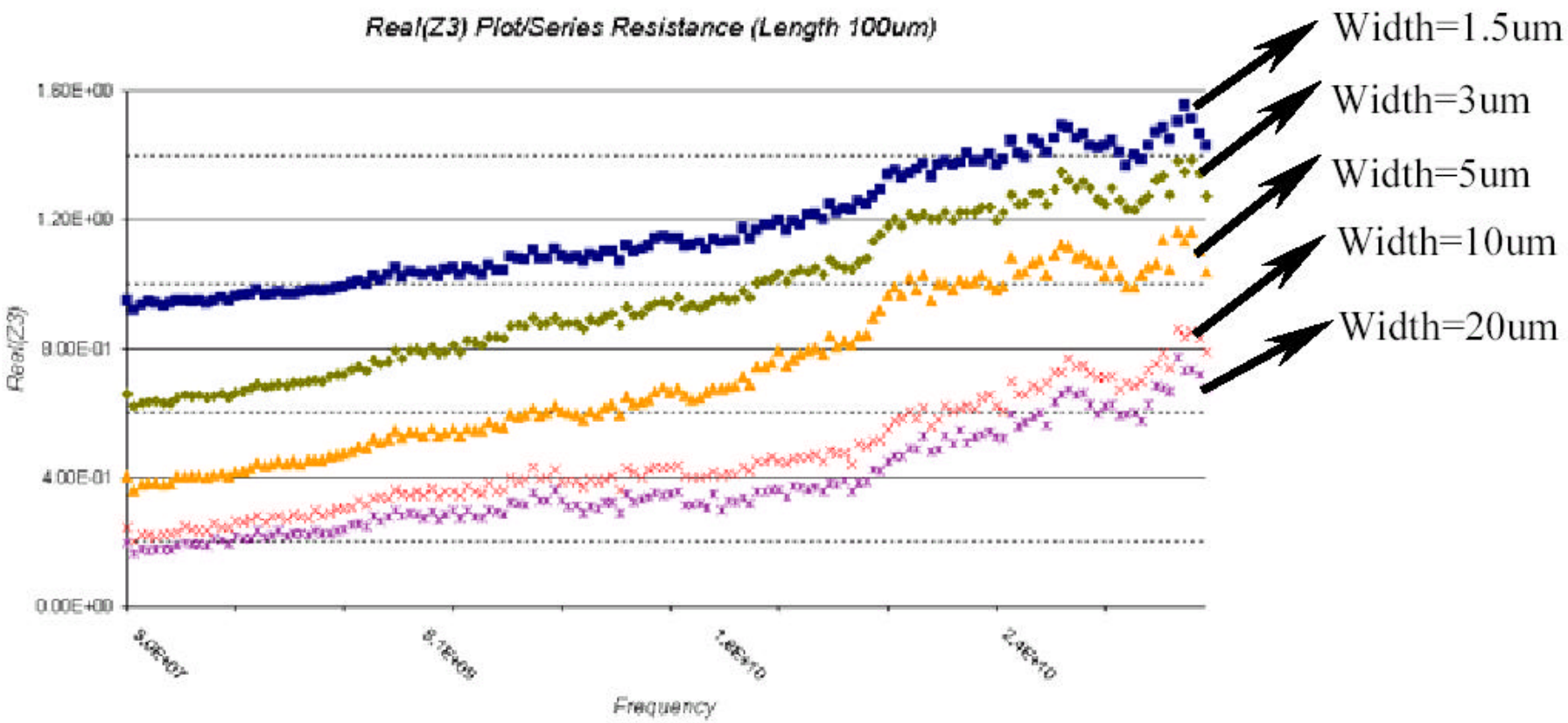
S11 = reflection from the input port



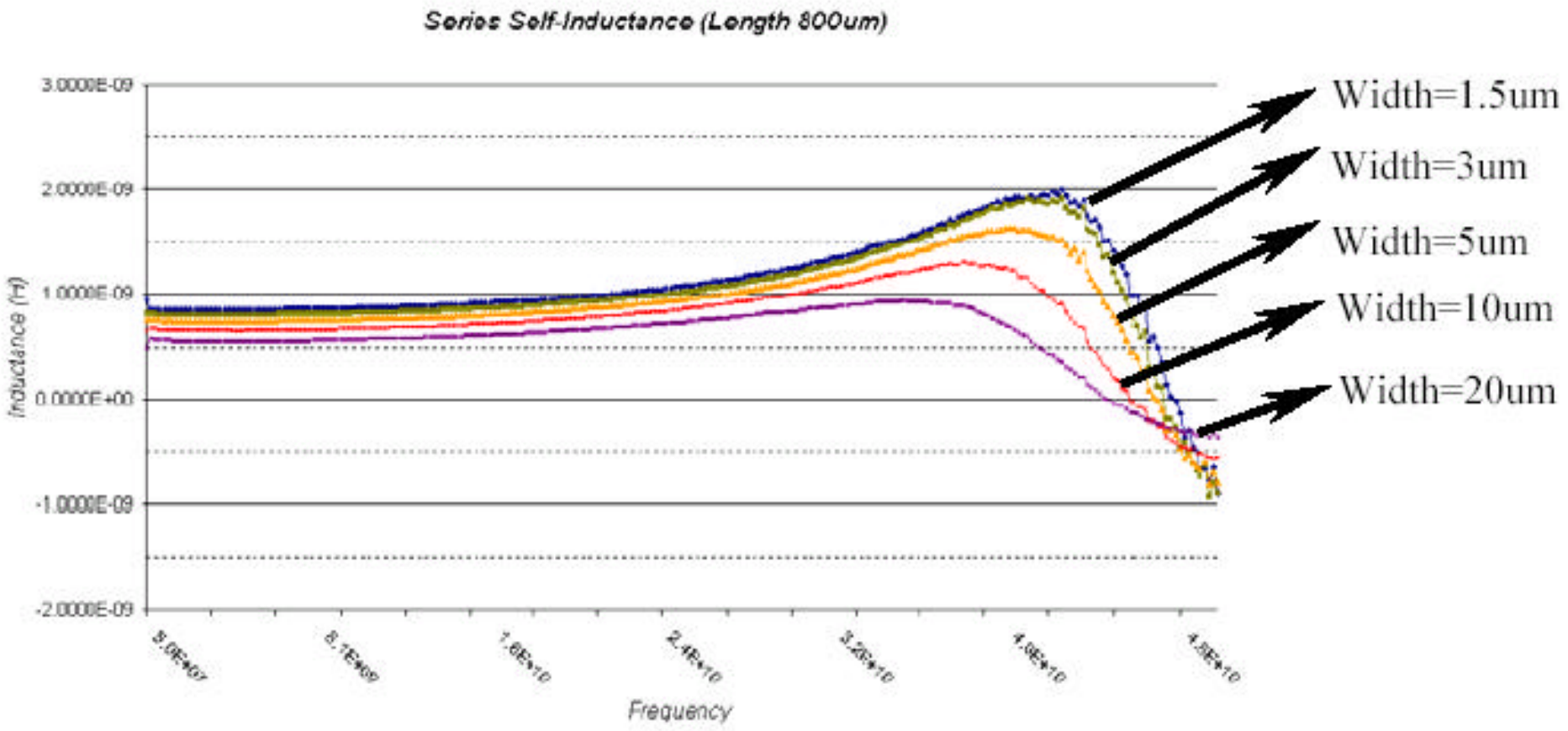
S21 = Transfer through the line



Series Resistance



Self-Inductance



Modeling the experimental data

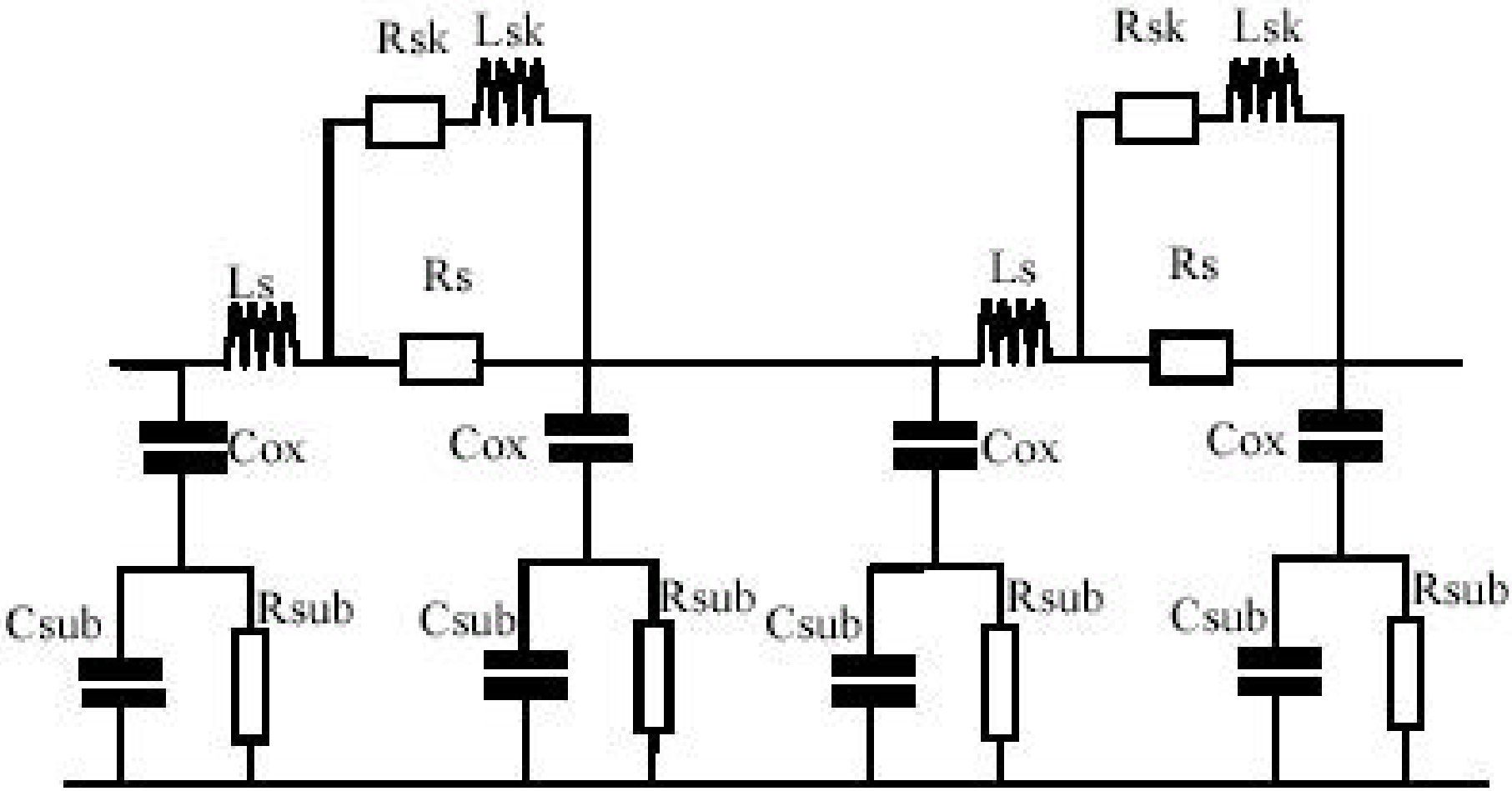
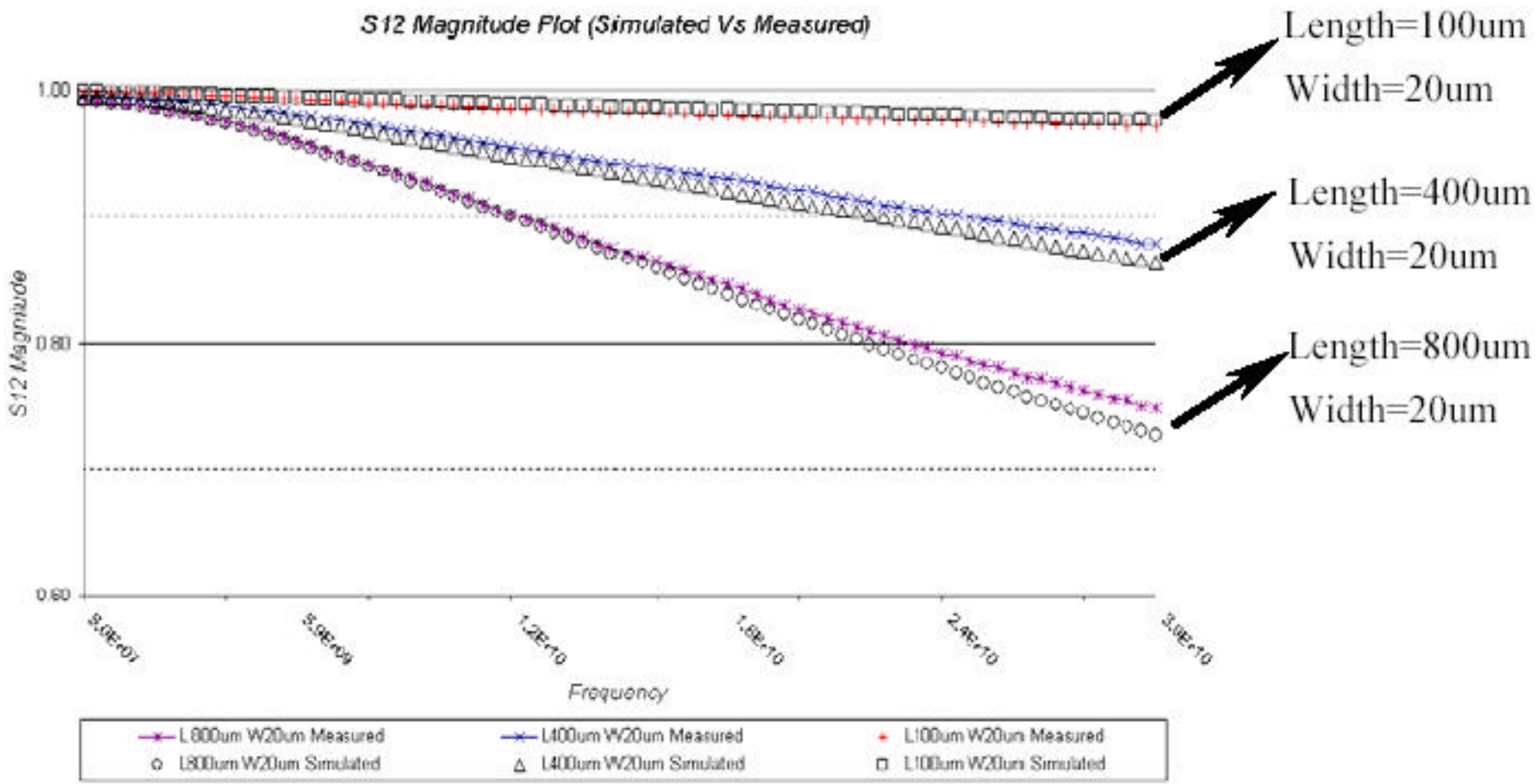
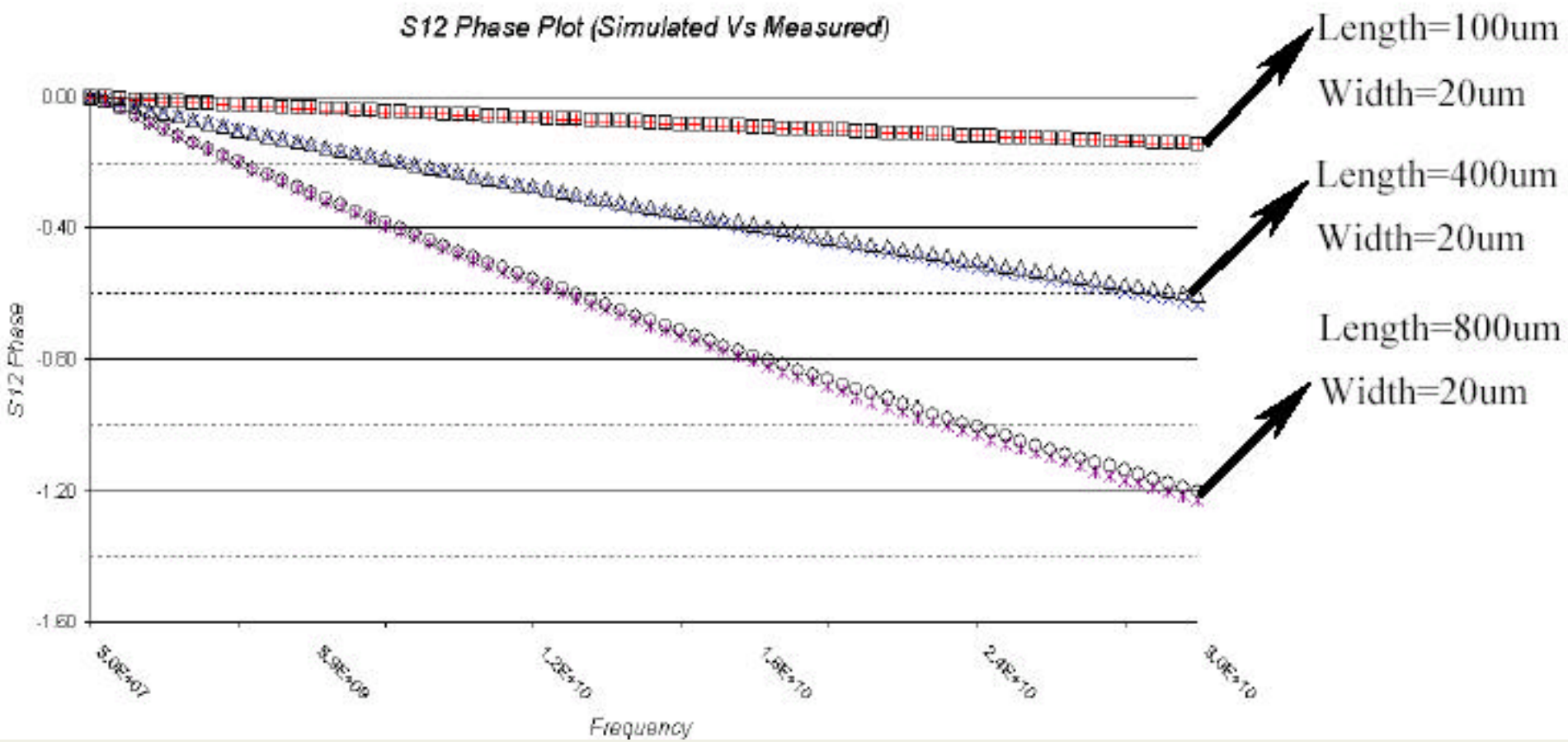


Figure 7: Physical model of interconnect

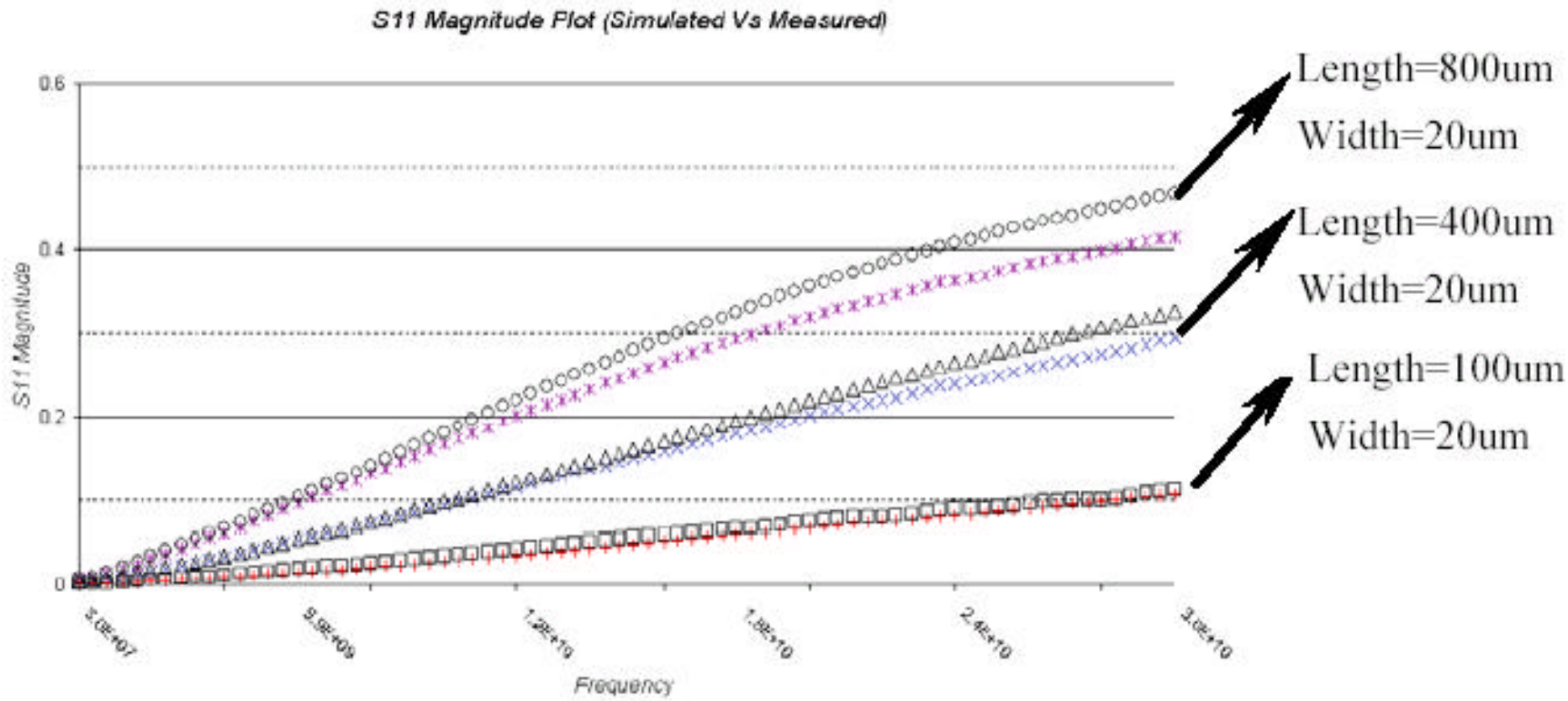
Modelled S12



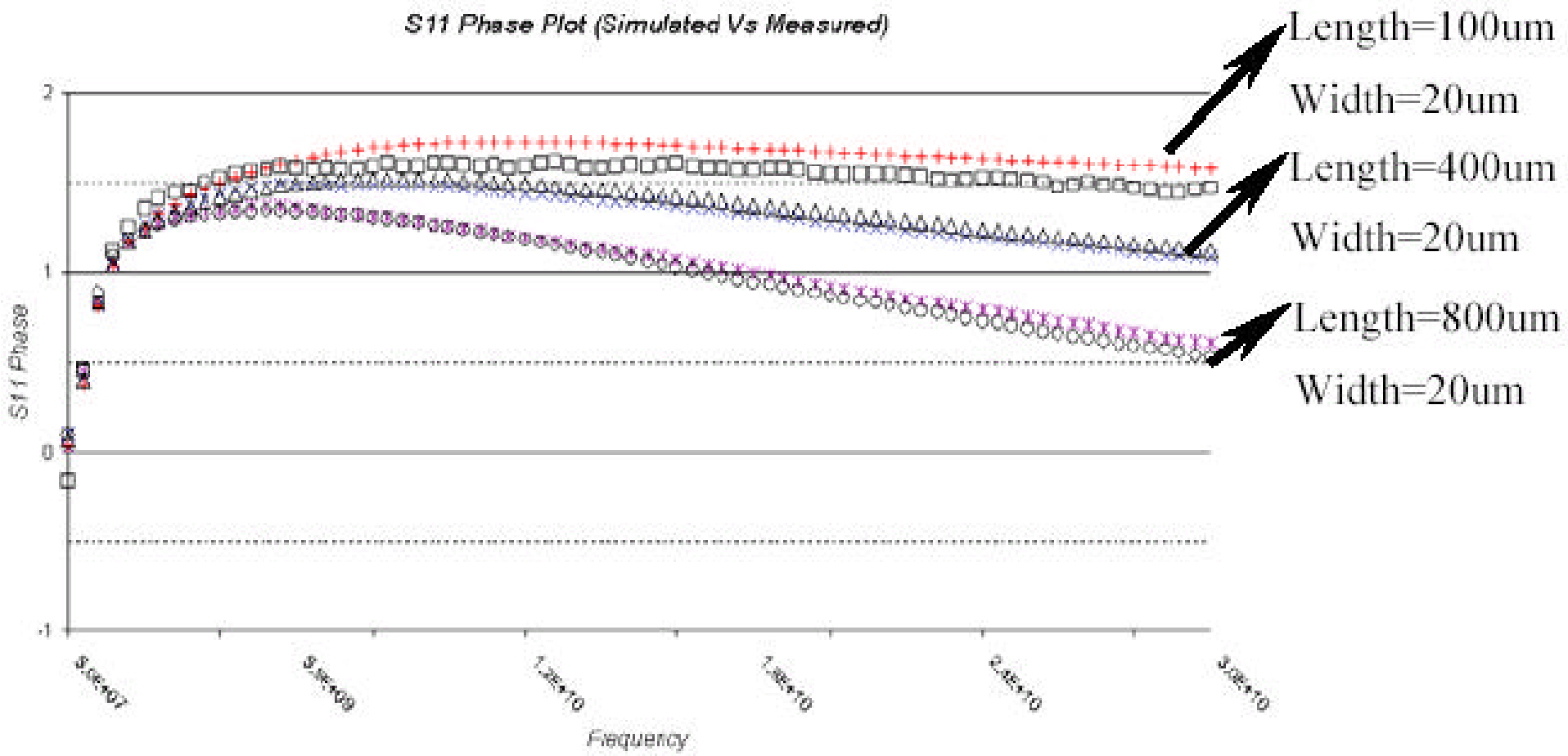
Modelled S12 Phase



Modelled reflection magnitude



Modelled reflection phase



What happens if you leave some elements out?

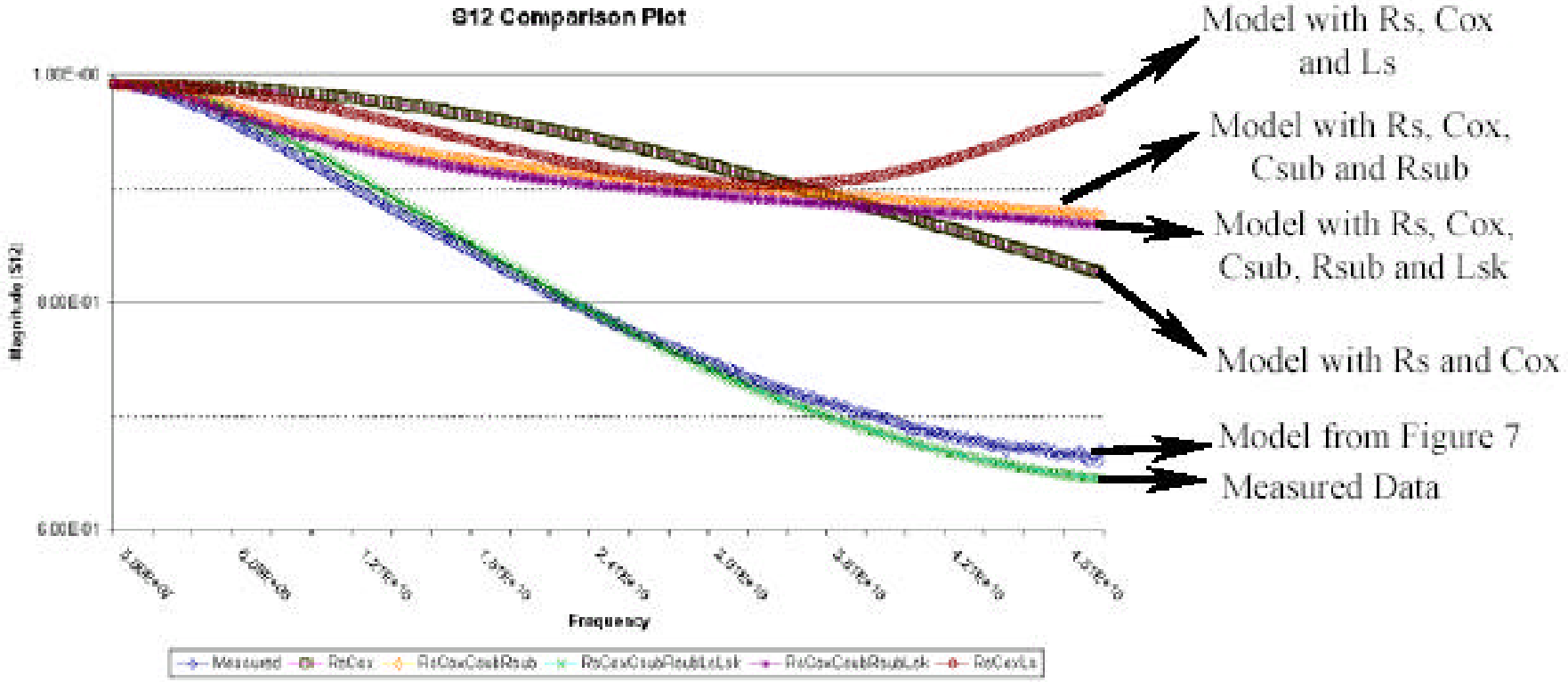


Figure 12: Model comparison

Conclusions (Ong's)

- Wire models can be well fit (S parameters or Spice) up to very high frequencies

Conclusions (mine)

- The models are well understood
- The hardware folks can measure all values we want
- So far they have measures of what the analog folks want
- If we cooperate, they could easily measure more ‘digital’ parameters
  - Over lower metal, not substrate
  - All layers and widths
- We need to cooperate with test structure folks