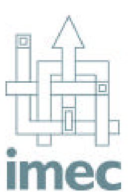

Interconnect Width Selection for Deep Submicron Designs using the Table Lookup Method

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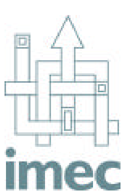


Backend Technology

→ More Functions per area
→ Less Cost per function

N

N + 1

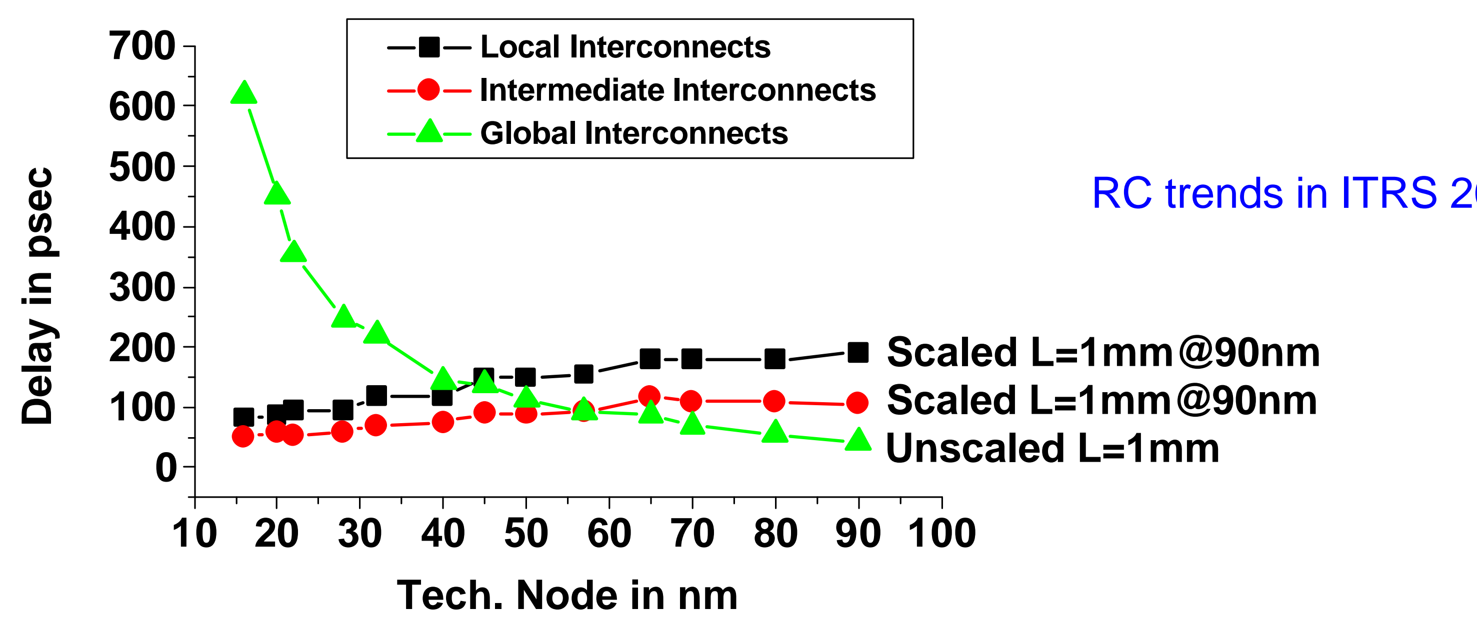
Metal

Dielectric

Silicon

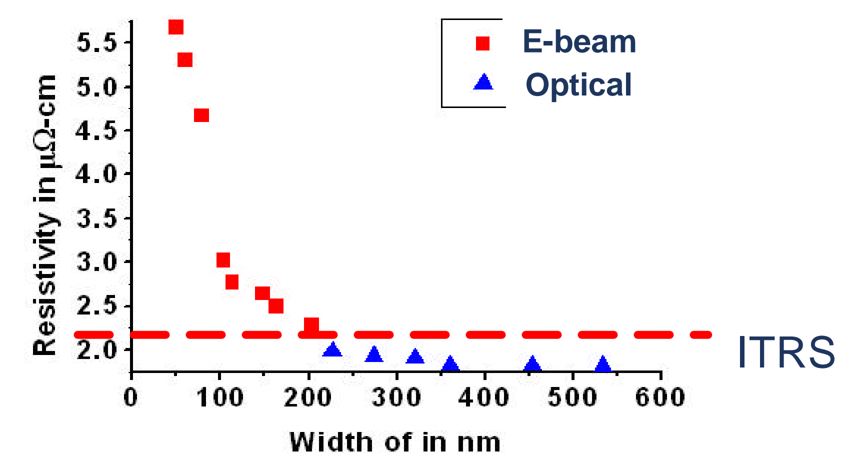
N : Tech. Node

Interconnect Delay



RC trends in ITRS 2003

W. Wu, R. Jonckheere, M. Stucchi, H. Struyf, Z. Tokei, I. Vervoort, I. Vos, F. Iacopi, and K. Maex, Studies on Resistivity of Narrow Cu Interconnects, Proceedings of Advanced Metallization Conference, pp. 345-348, (San Diego, October 2002)



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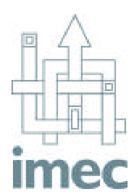


Technology Issues

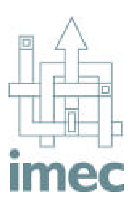
	Value	Error
a	-3.5e+20	4.3148e+20
b	3.75e+19	2.9387e+18
Chisq	5.4971e+41	NA
R^2	0.97735	NA

y = a + (b=limit(3e+19, 3.76...

F. Iacopi, M. Stucchi, O. Richard and K. Maex, "Electrical Equivalent Sidewall Damage in Patterned Low-k Dielectrics", to appear in Electrochemical and Solid-State Letters, 2004.

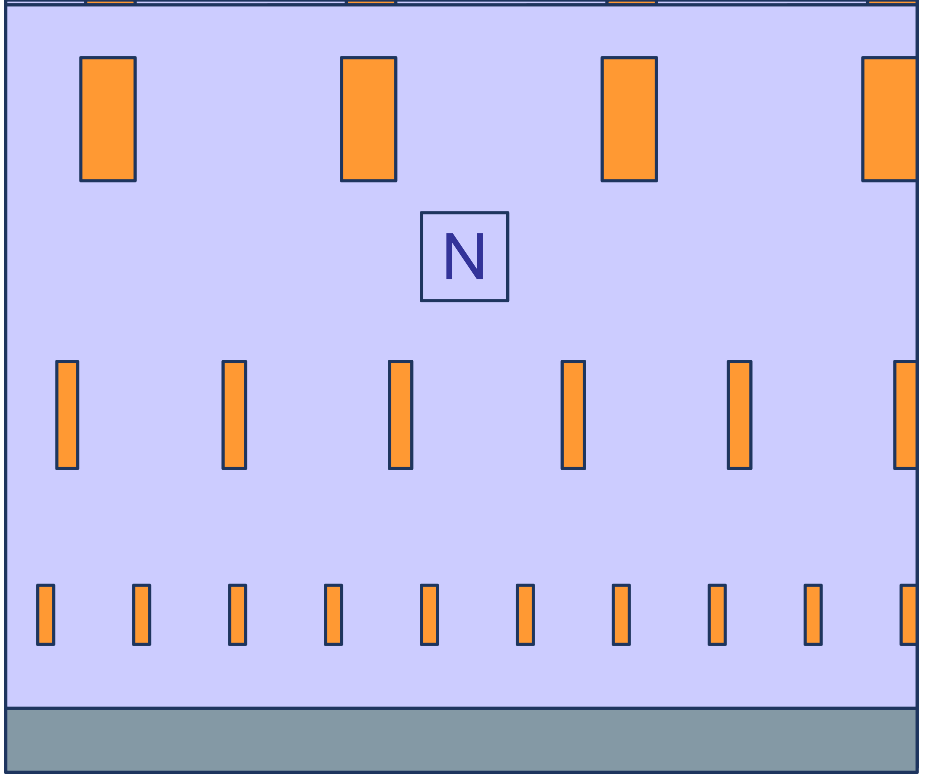
'Electrical equivalent sidewall damage'

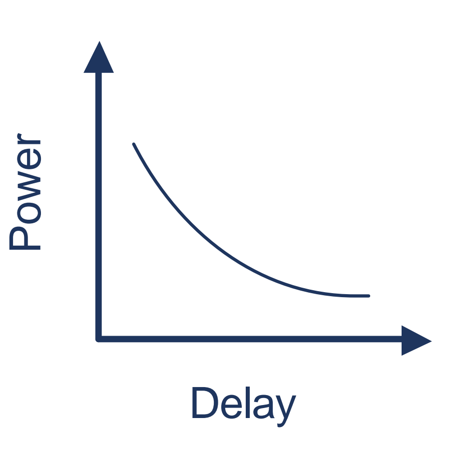
S'~10nm!



Let us assume that scaling continues in spite of DSM issues

Width and Height exploration for constant pitch





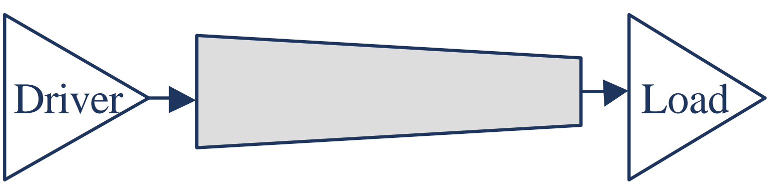
Metal

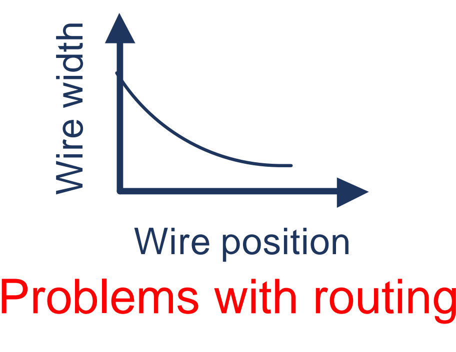
Dielectric

Silicon

Interconnect Width Sizing

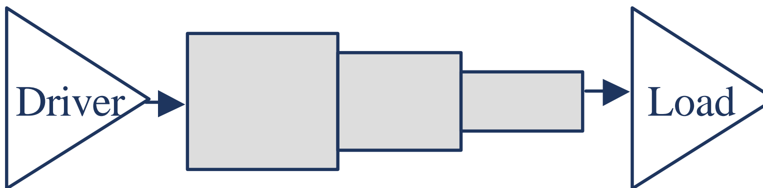
- Width Sizing [Lee2000,Alpert2001,Cong2002,Jiang2001]
  - Decreasing the wire width progressively from source to sink.(TWS)





  - Multiple Width Sizing (MWS or TWS)

Problems with routing



  - Uniform Width Sizing (UWS)

Interconnect Width Selection by Table Lookup Method

Driver

Interconnect

1

2

n

Slew

I

Mux.

Length

Type
of load

4-D Lookup Table

Variable R

R

Driver

C1

C2

Variable slew

Variable C1

Variable C2

$R = 0.48R_{int}$

$C1 = 1/6C_{int}$

$C2 = 5/6C_{int} + C_L$

O'Brien/Savarino pi Model

slew

R

C1

C2

Pre-Characterized Delay and Power Table

Delay

Power

Exploration Methodology (Case Study-1)

Obtain length information from the physical design process of a real Integrated Circuit

Extract *priori* length estimates using the rent's rule for a Integrated Circuit model

N = 1

Using the length estimates obtain the average interconnect length for a given metal layer = N

Select the interconnect width to minimize the targeted function

Check if the selected width is Within the accepted SI Spec.

no → Remove this option from the available width options

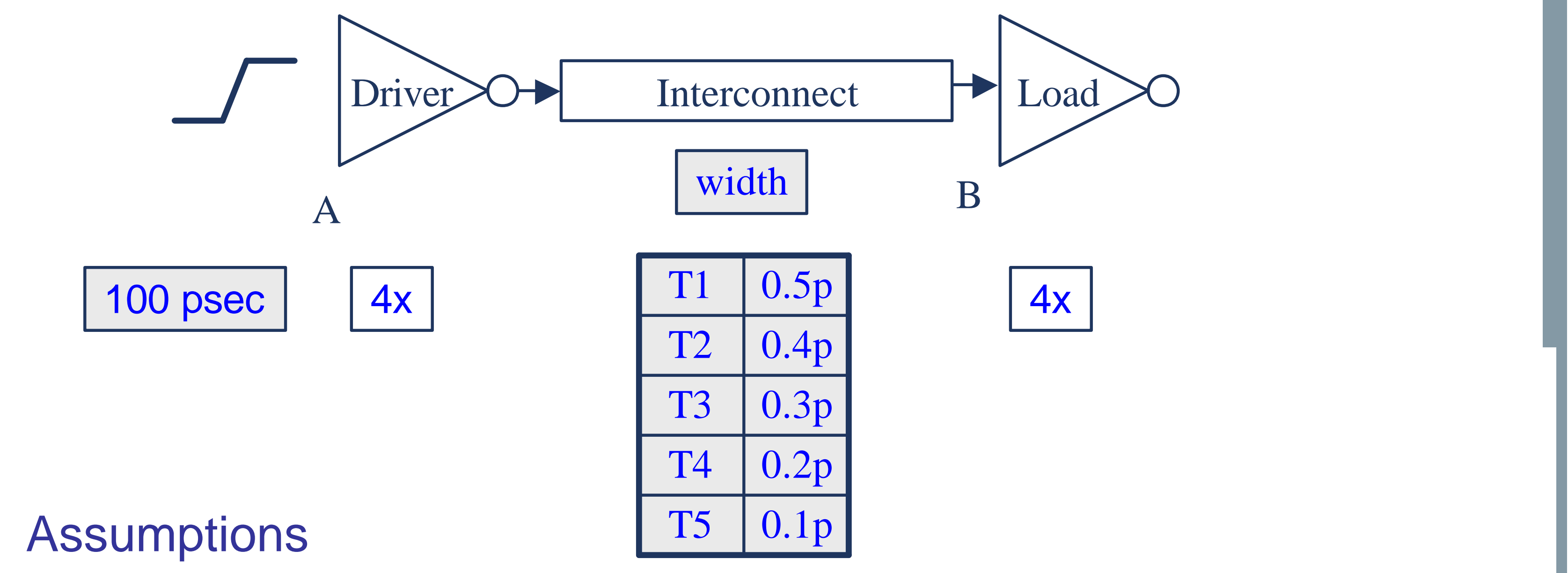
yes

N = last metal layer ?

yes → Do the routing with the Selected width for each layers

no → N = N +1

Circuit Example (2 pin net)



Assumptions

- Exploration for 45 nm node
- Length information obtained by using rent's rule for a simple isotropic model of an IC (a priori length information)
- Analysis done for average wire length in 2nd layer (440 um)
- Driver and load both are 4x inverters
  - 45nm BSIM4 model card used [1]
- One width per layer assumed
- $T_{A \rightarrow B}$ and Total power dissipation were calculated

[1] http://www-device.eecs.berkeley.edu/~ptm

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Exploration of width for optimizing delay

T1	0.5p
T2	0.4p
T3	0.3p
T4	0.2p
T5	0.1p

T1	0.5p
T2	0.4p
T3	0.3p
T4	0.2p
T5	0.1p

Volts

0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

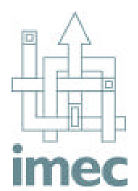
Vt

T1
T2
T3

AD
R
v1
AL
C12
C
VD
R
v2
VL
C

0
0.5
1
1.5
2
2.5

Time in nsec



Power vs. Delay

T1	0.5p
T2	0.4p
T3	0.3p
T4	0.2p
T5	0.1p

Including Buffer Sizing

Driver → Interconnect → Load

A

B

100 psec

Driver size
1x
2x
4x
8x

T1	0.5p
T2	0.4p
T3	0.3p
T4	0.2p
T5	0.1p

4x

Normalized Power Dissipation

1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4

0.5 1.0 1.5 2.0 2.5 3.0 3.5

Normalized Delay

1X
2X
4X
8X

Normalized w.r.t. T1 and 4x

T1

T5

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T1	0.5p
T2	0.4p
T3	0.3p
T4	0.2p
T5	0.1p

Normalized Power Dissipation

1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4

8X
4X
2X
1X

T1
T2
T3
T4
T5

0.5 1.0 1.5 2.0 2.5 3.0 3.5

Normalized Delay

Normalized w.r.t. T1 and 4x

Local Interconnects (length = 40 um)

T1	0.5p
T2	0.4p
T3	0.3p
T4	0.2p
T5	0.1p

Normalized w.r.t. T1 and 4x

Global Interconnects (length = 800 um)

T1	0.5p
T2	0.4p
T3	0.3p
T4	0.2p
T5	0.1p

Normalized Power Dissipation

Normalized Delay

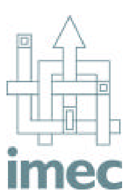
8X 4X 2X 1X

T1 T2 T3 T4 T5

Normalized w.r.t. T1 and 4x

Conclusions

- Exploration can be done for interconnect dimensions
  - Informed choice for interconnect dimensions
- Local Interconnects (very short wires…)
  - Not much Trade off is possible by width-only exploration
  - Smallest width is the best solution for constant pitch in context of power and delay optimization
- Intermediate Interconnects
  - Significant Trade off can be made between delay and power
- Global Wires
  - Dissipation can be traded for reducing the delay
  - Simultaneous buffer sizing and wire sizing is the best option
- Future work
  - Variable pitch and height exploration
  - Better Signal Integrity evaluation models
  - Effect on area



Thank you!

questions