# A 2-Slot Time-Division Multiplexing (TDM) Interconnect Network for Gigascale Integration (GSI)

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# Outline

- Motivation
- TDM technique for wire sharing
- System level impact
- Conclusion

# Motivation

- ITRS2003 Projections

| Year of production | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 |
|---|---|---|---|---|---|---|---|
| Technology generation (nm) | 100 | 90 | 80 | 70 | 65 | 57 | 50 |
| Number of metal levels | 9 | 10 | 11 | 11 | 11 | 12 | 12 |

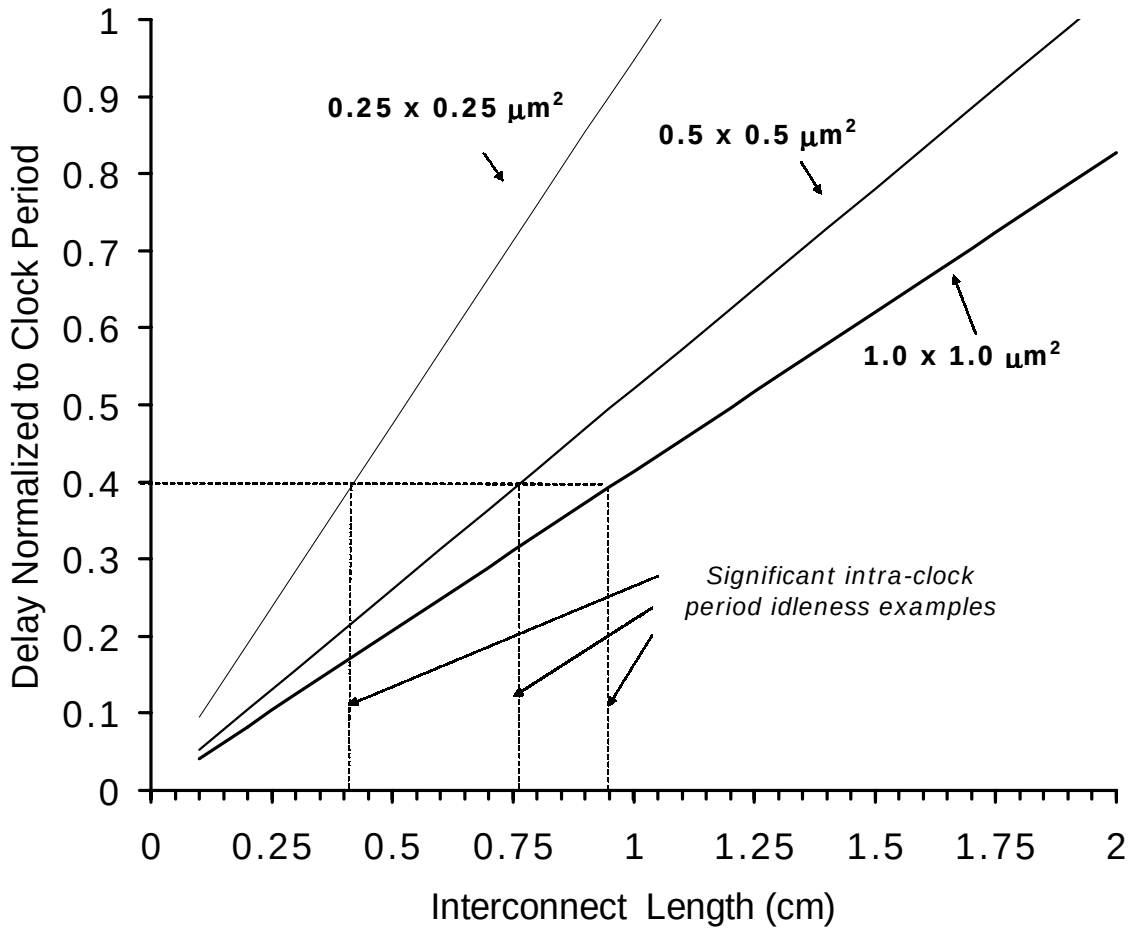
- Number of metal layers increases with each new technology generation
- Manufacturing cost $\propto$ number of metal levels

# Motivation (contd..)

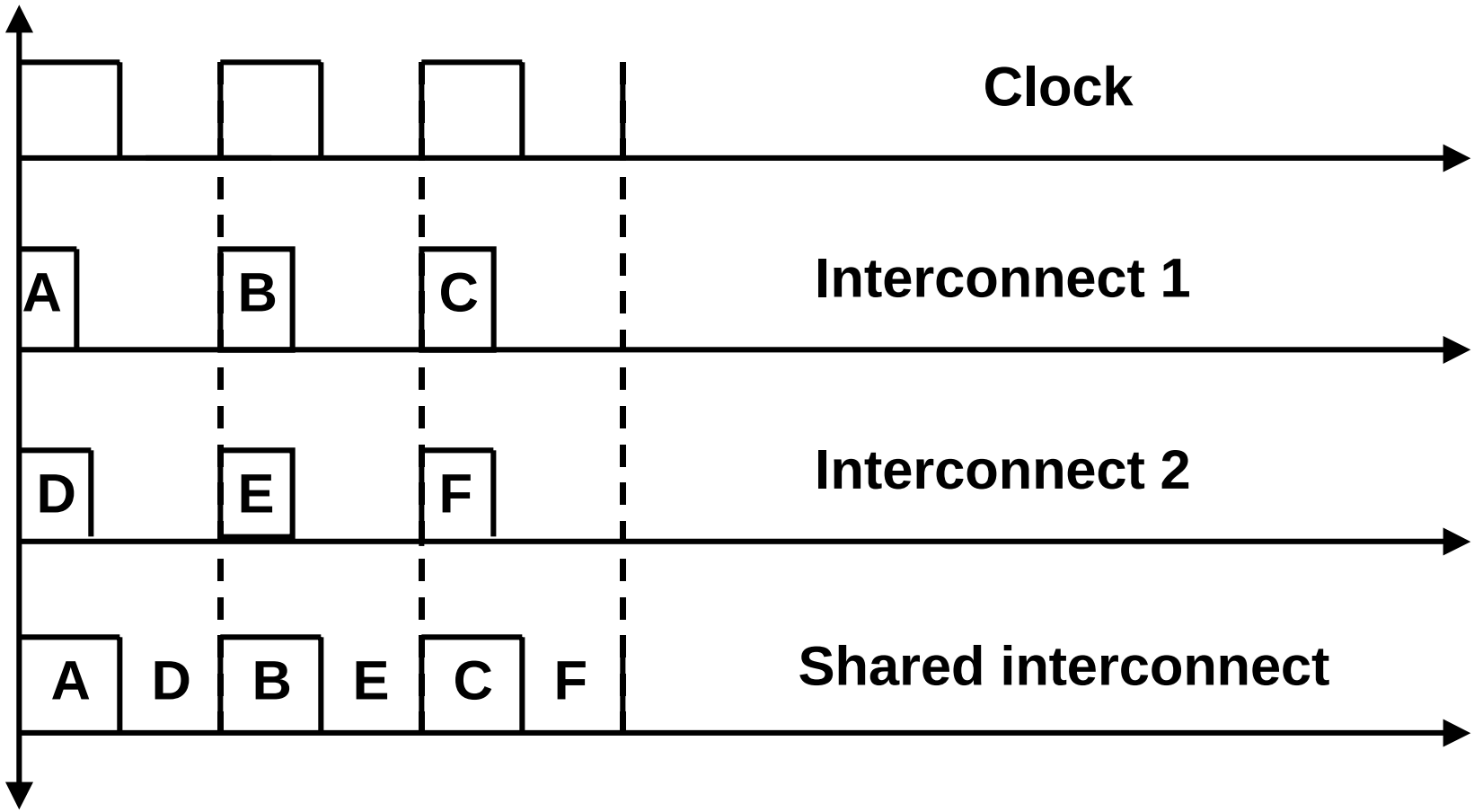
- Network on Chip (NoC) for SoC
  - Complex algorithms *[Dally, DAC '01]*
  - Overhead circuitry *[Bhojwani, VLSI '03]*
  - Needs regularity of logic macrocells *[S. Kumar, ISVLSI '02]*
- Need a simple wire sharing technique that can
  - Capitalize on wire idleness
  - Easily applied to random logic macrocell connections

# Intra-clock Period Idleness

- Clock cycle period ∝ length of longest interconnect
- Interconects idle for more than 60% of clock period
- Intra-clock period idleness…opportunity for wire sharing?
- No microarchitecture change needed



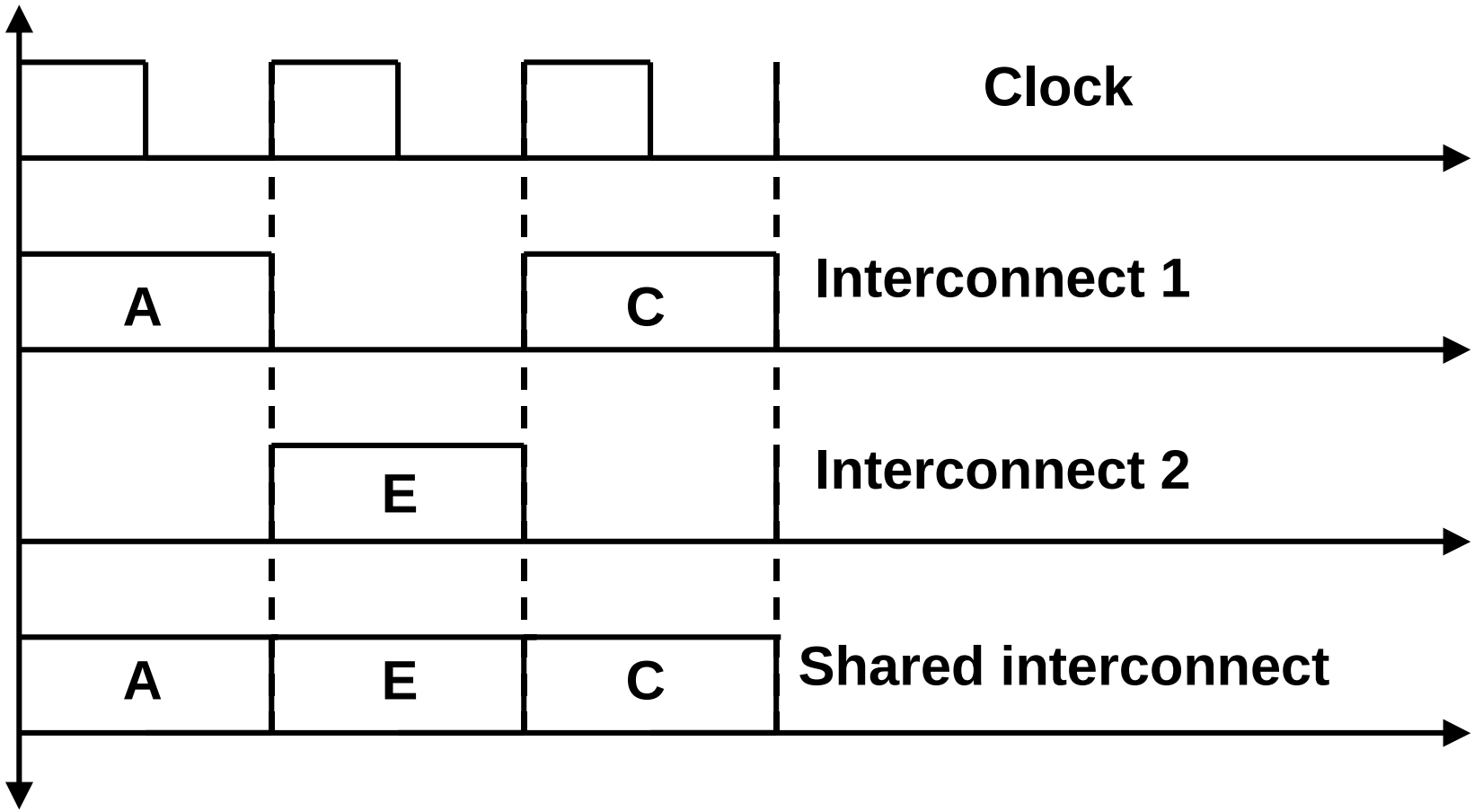
# Intra-clock Period Idleness (contd..)



# Inter-clock Period Idleness

- Activity factor plays a major role
  - 10% activity used for most power calculations
  - Interconnects idle for 9 out of 10 clock cycles
  - Significant opportunity for wire sharing
- Microarchitecture change needed
  - Need mutually exclusive interconnects
  - Buffers not required

# Inter-clock Period Idleness (contd..)



# Key Issue – Physical Layout Constraint

**Source/Sink locations**

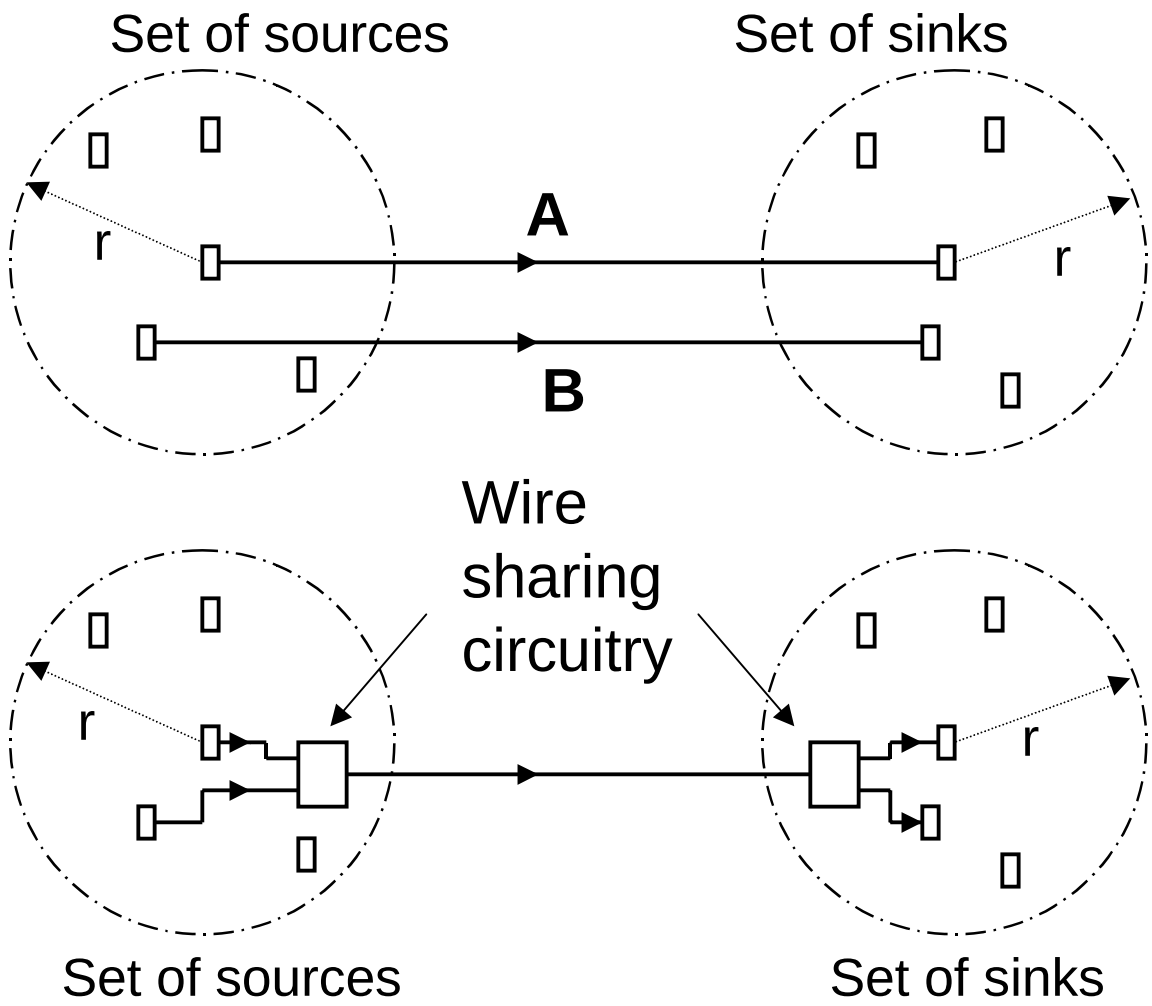
**Shared run length**

**Physical layout of a random logic cell**

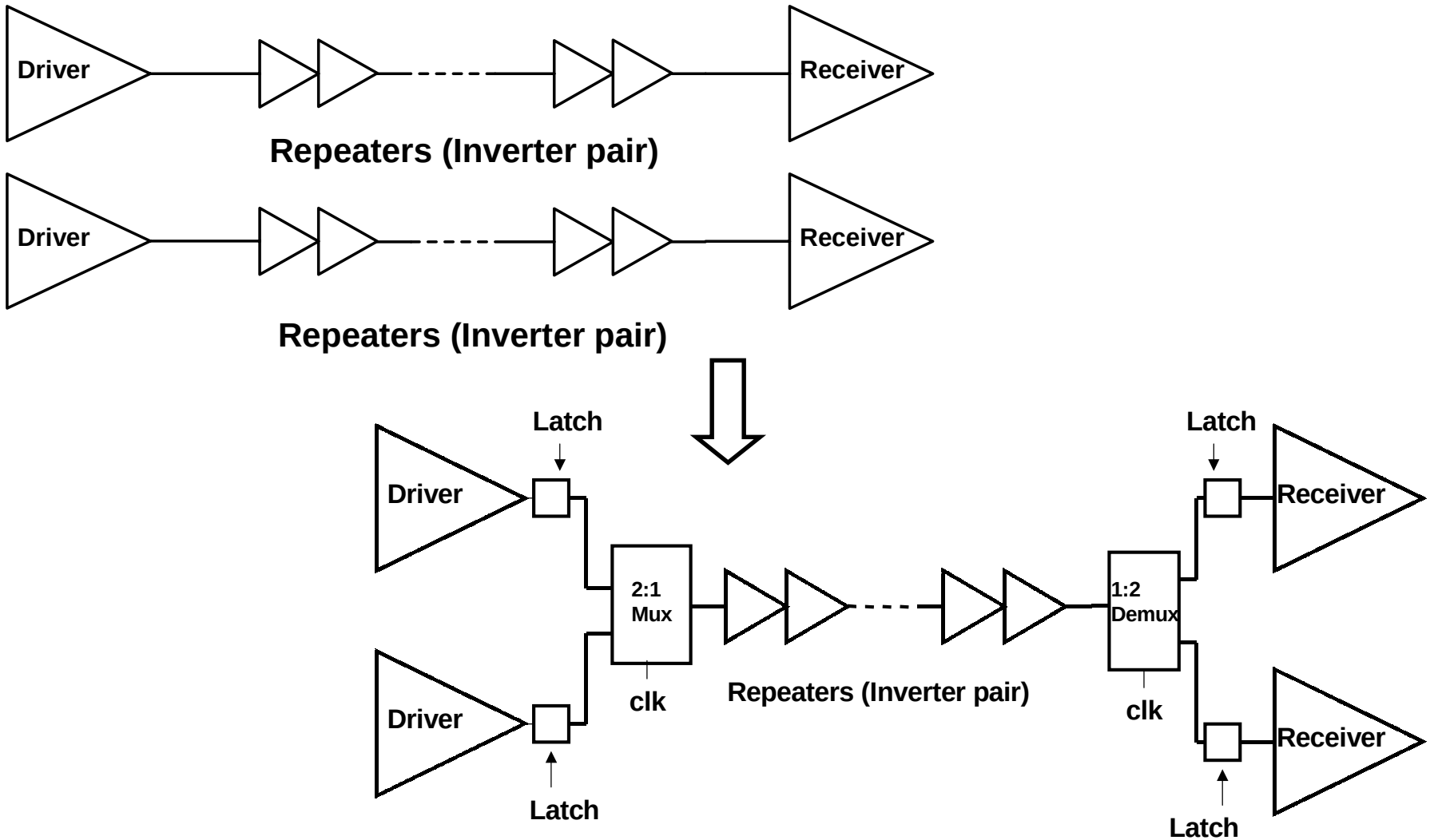
- Wire sharing efficiency
- CAD tools could force higher wire sharing efficiency

# Source/Sink Proximity

- Sources and sinks need to be in the neighborhood
- r <= 1% wire length (r is the neighborhood radius)

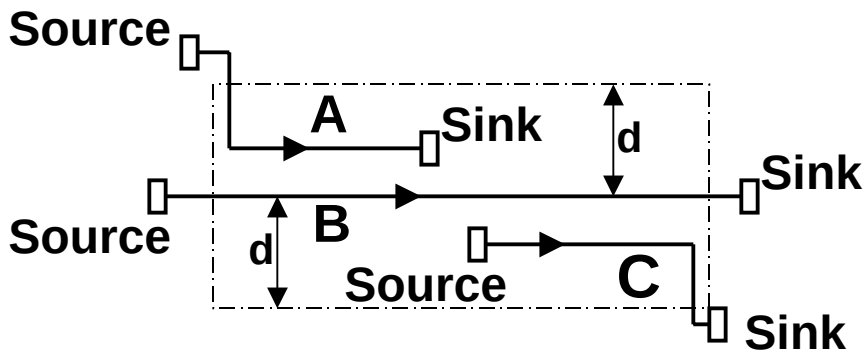


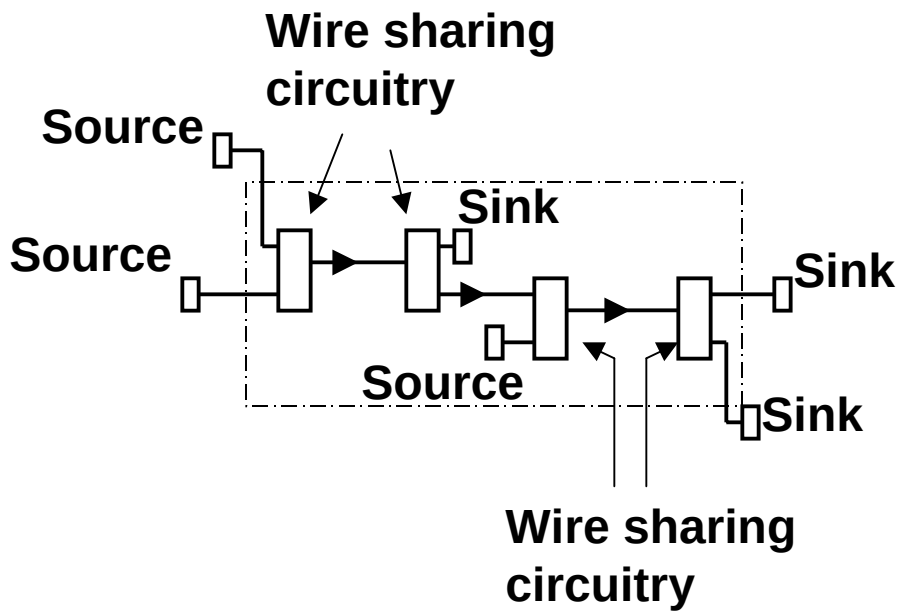
# Layout Example 1 – Source/Sink Proximity



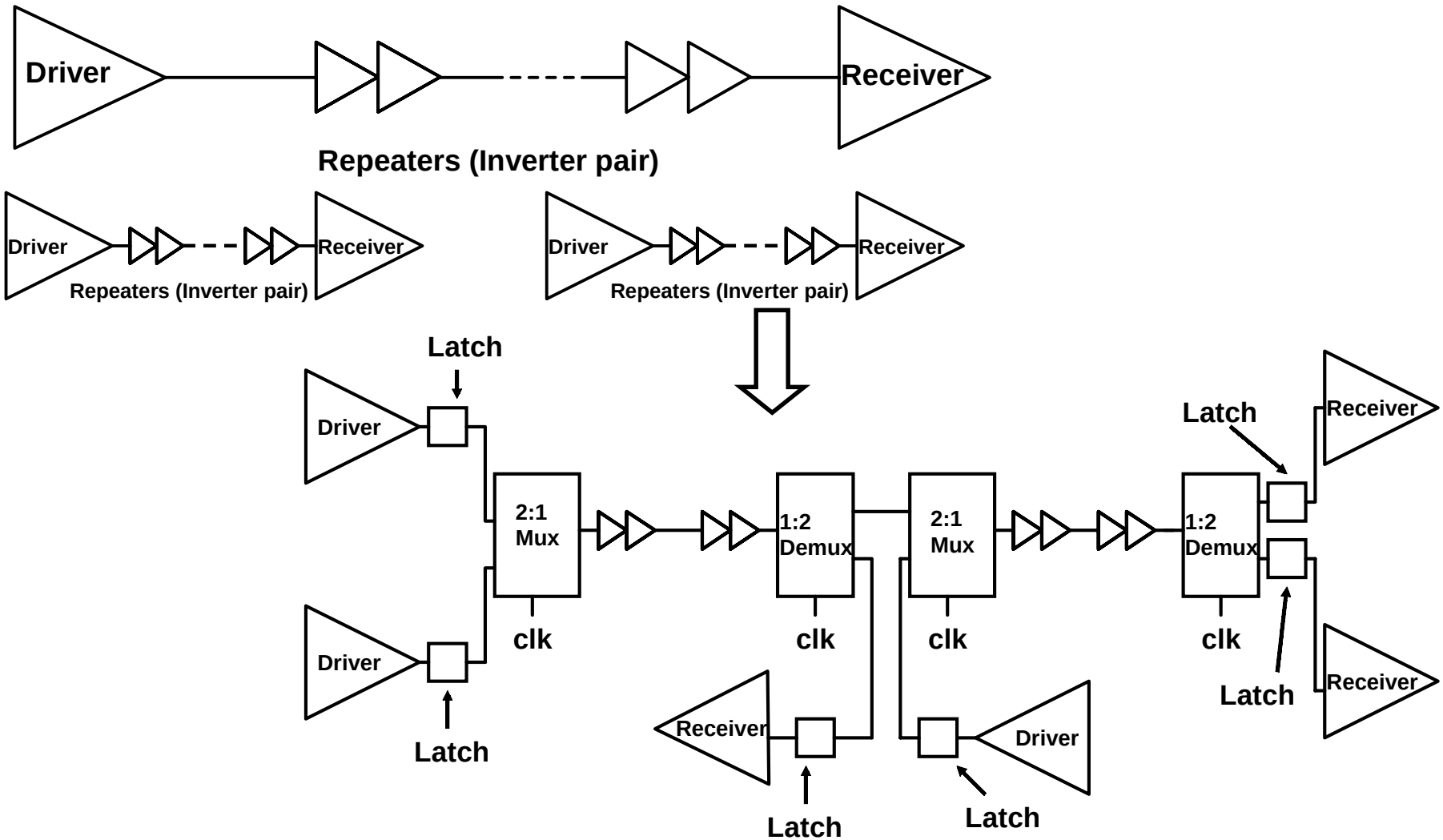
# Run Length Proximity

- TDM technique applied to multiple wires
- d <= 1% of wire length (where d is the neighborhood distance)



# Layout Example 2 – Run Length Proximity



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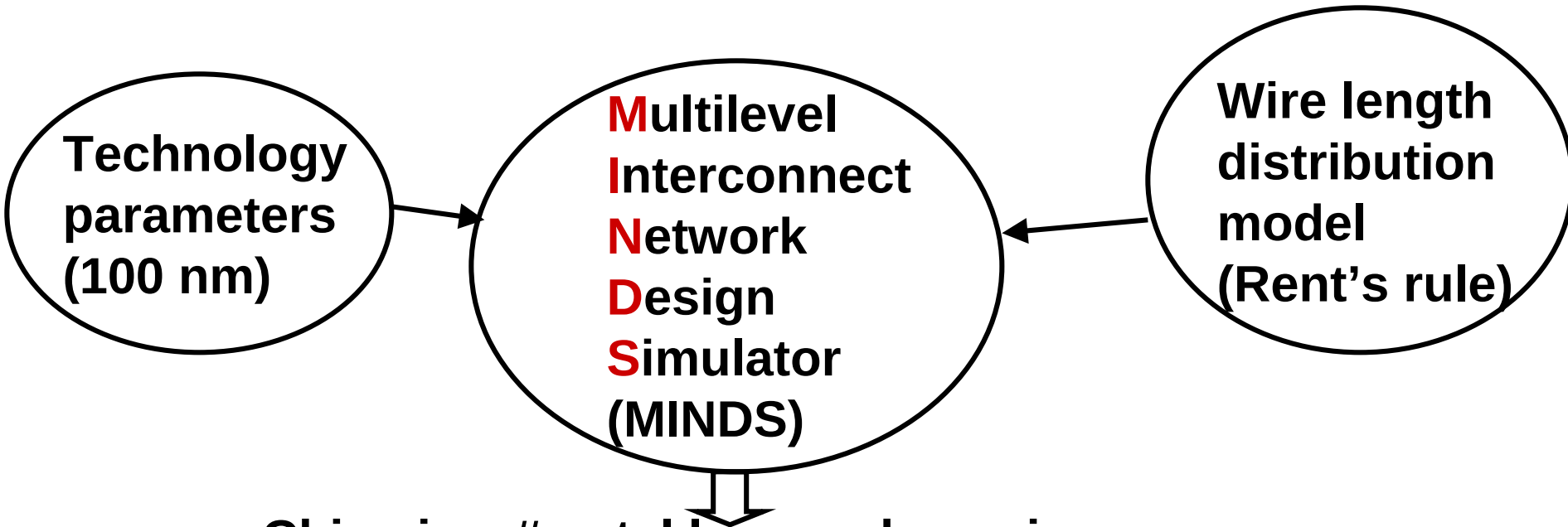
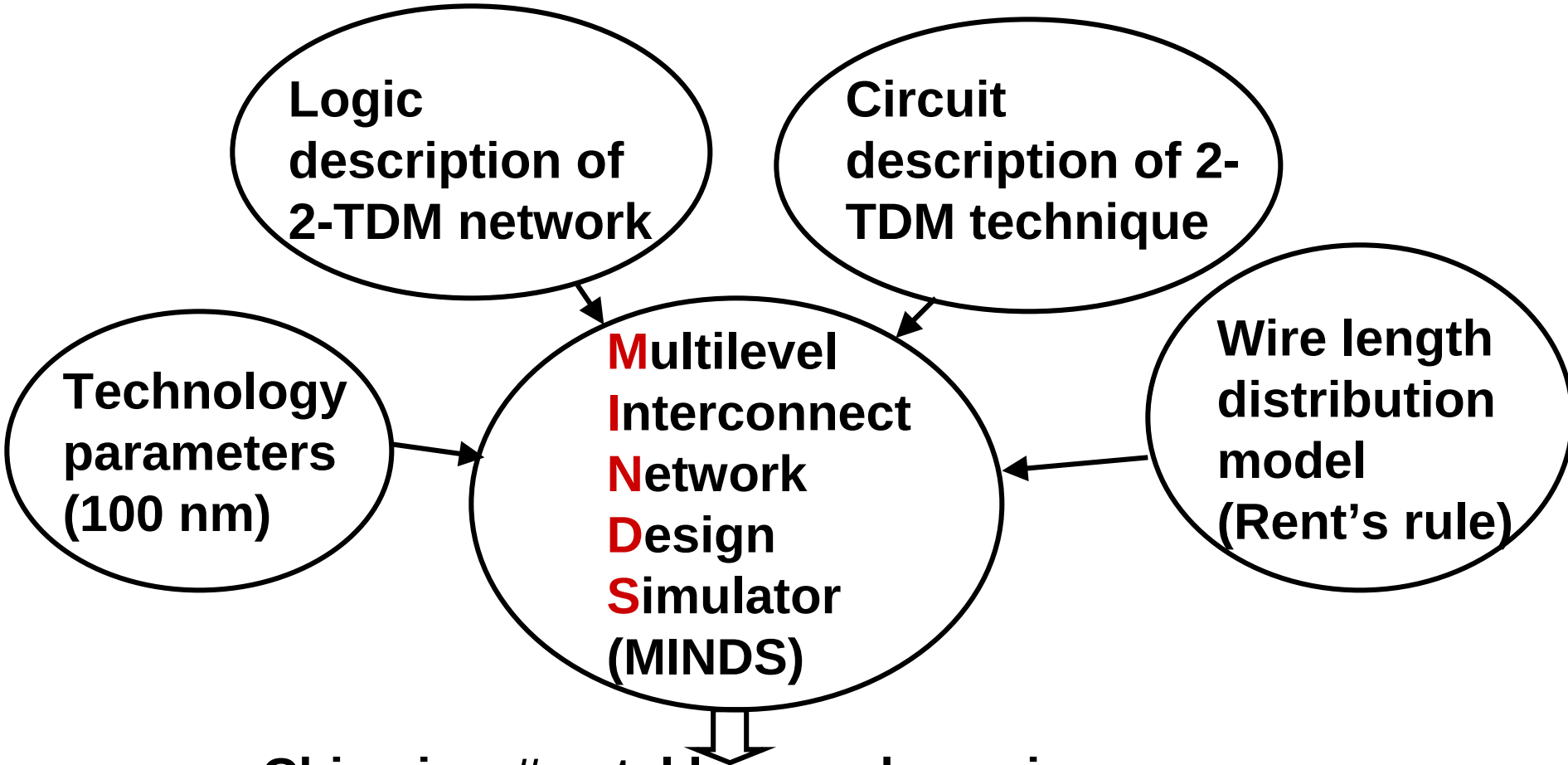
# System Level Model




**Chip size, #metal layers, dynamic power, max. operating frequency, interconnect distribution on various layers**

# System Level Model




**Chip size, #metal layers, dynamic power, max. operating frequency, interconnect distribution on various layers**

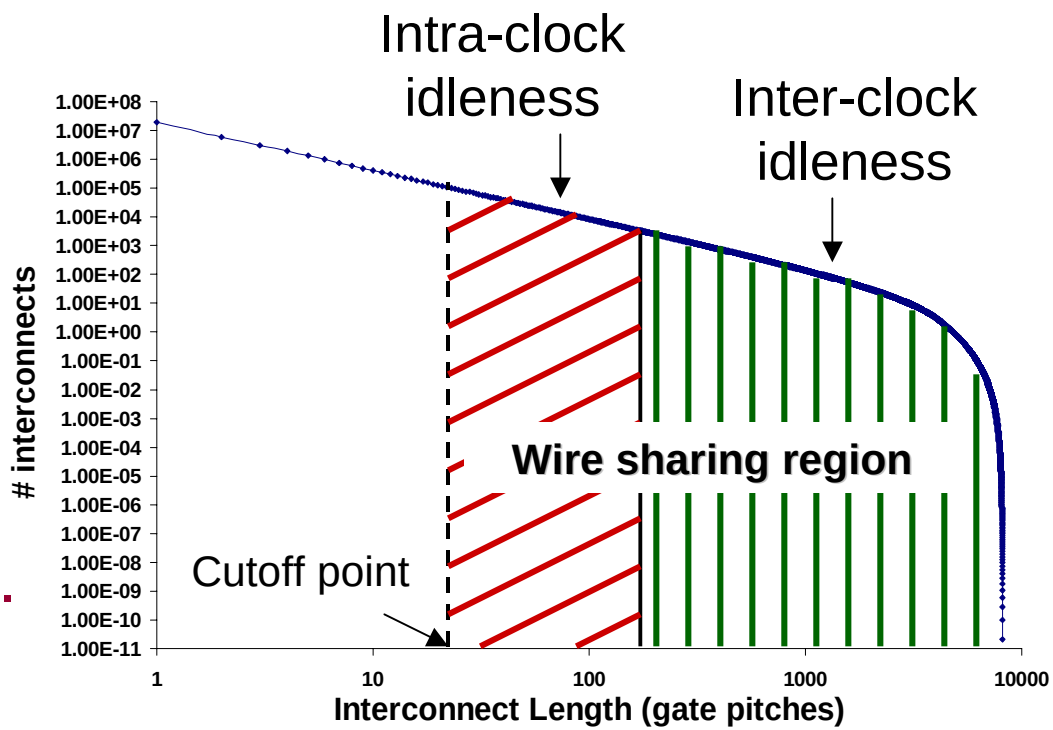
# Case Study

- Wire sharing driven by
  - Interconnect delay / cycle time
  - Activity factor
- Cutoff length
  - # interconnects

shared = $I(l)$ . $e_{share}$

$I(l)$ : wire distr. function

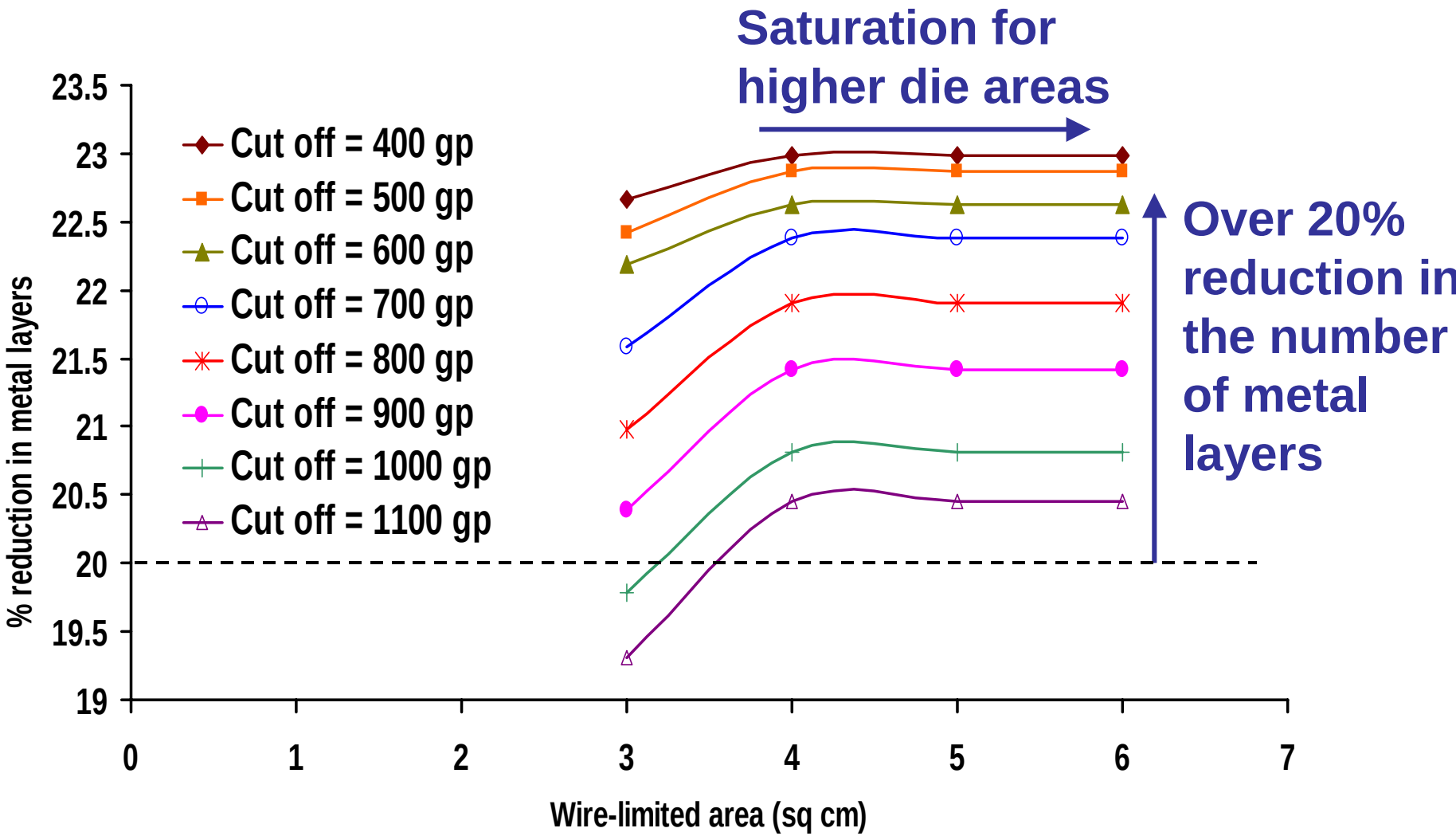
$e_{share}$ : wire sharing eff.



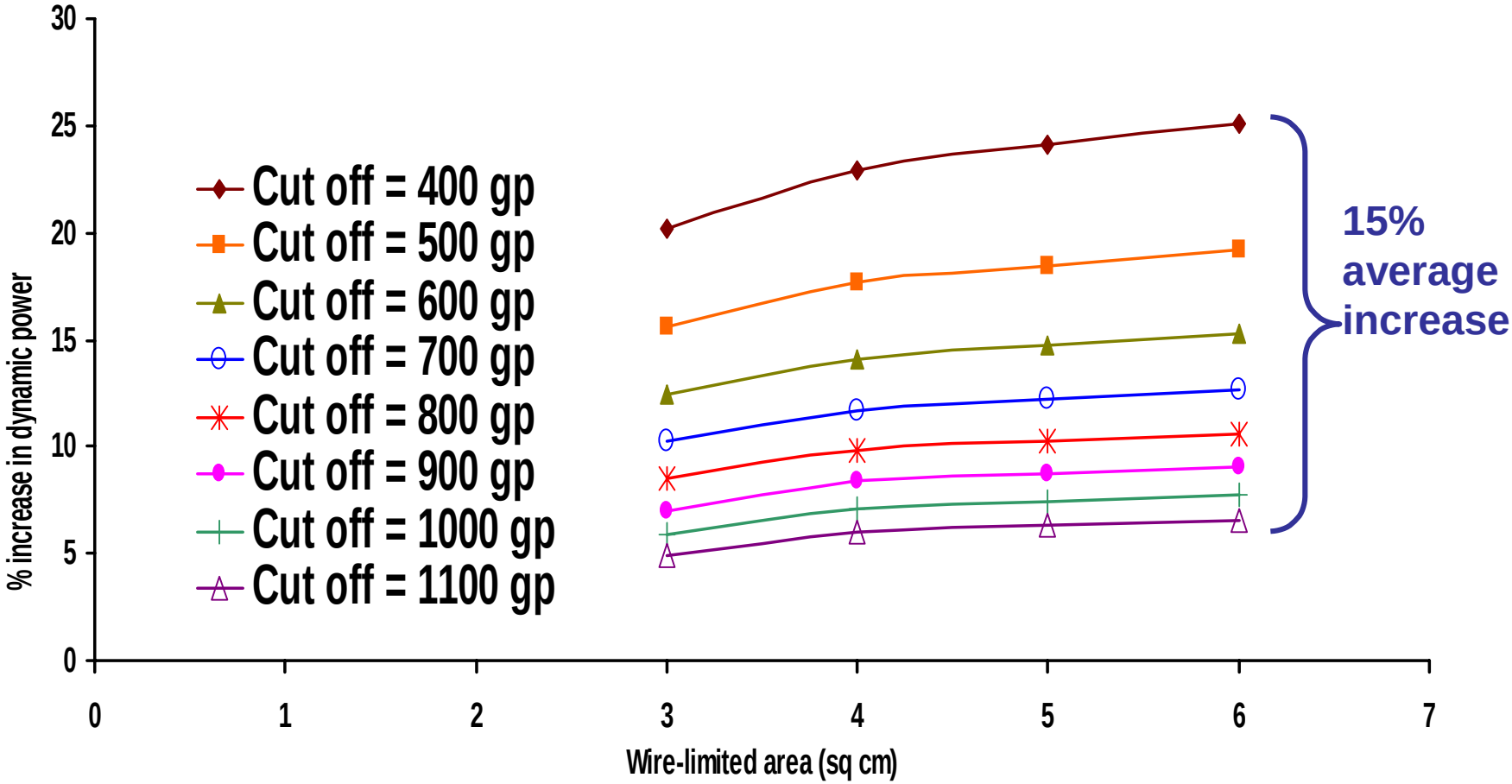
# Assumptions for Case Study

- 0.1µ technology
- 100M transistors distributed uniformly
- Operating Frequency = 1.5 GHz
- 40% Wiring efficiency
- 60% Wire sharing efficiency
- Rent's exponent = 0.66
- Rent's coefficient = 4.0

# Metal Layers

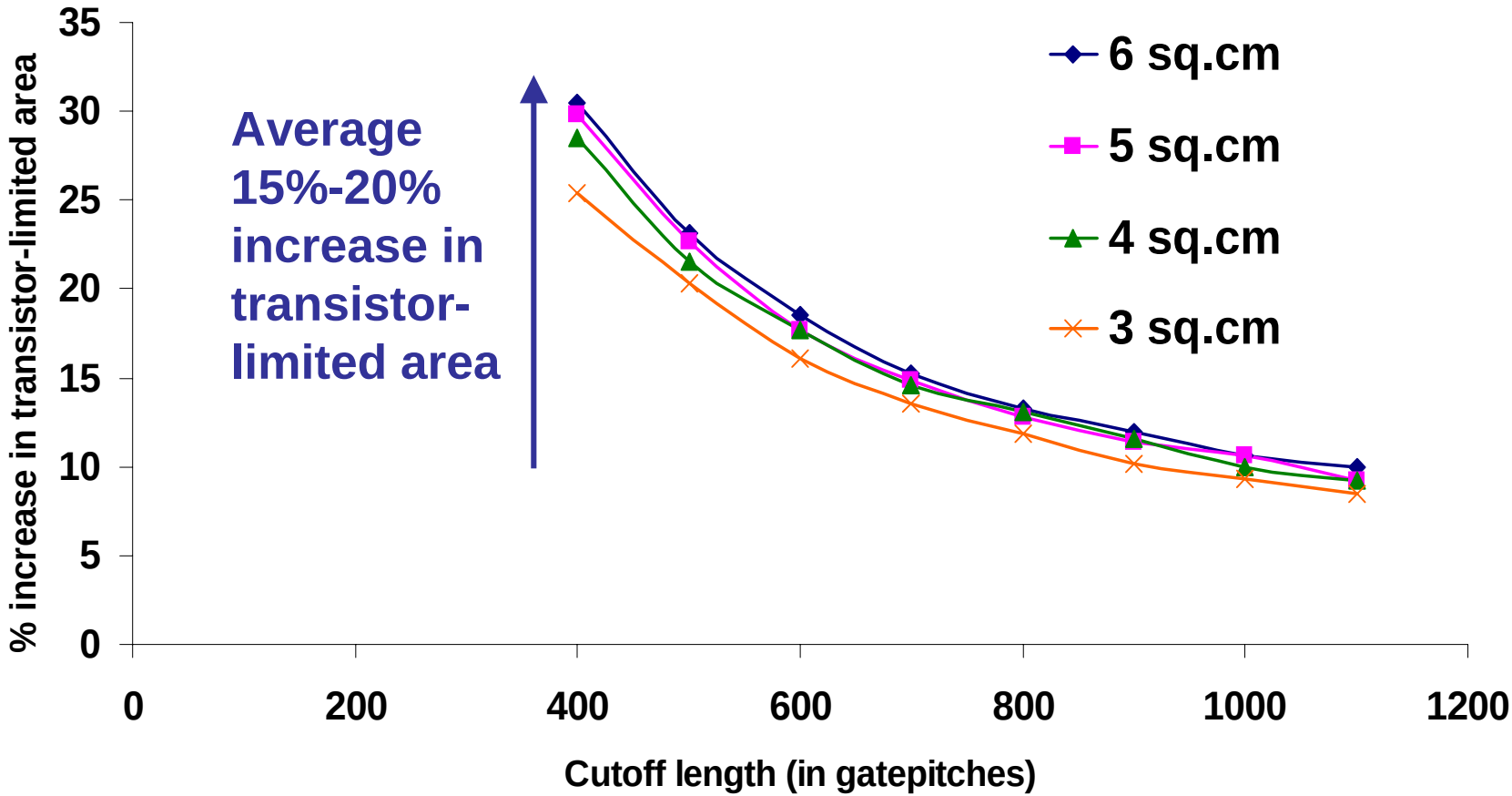


# Dynamic Power



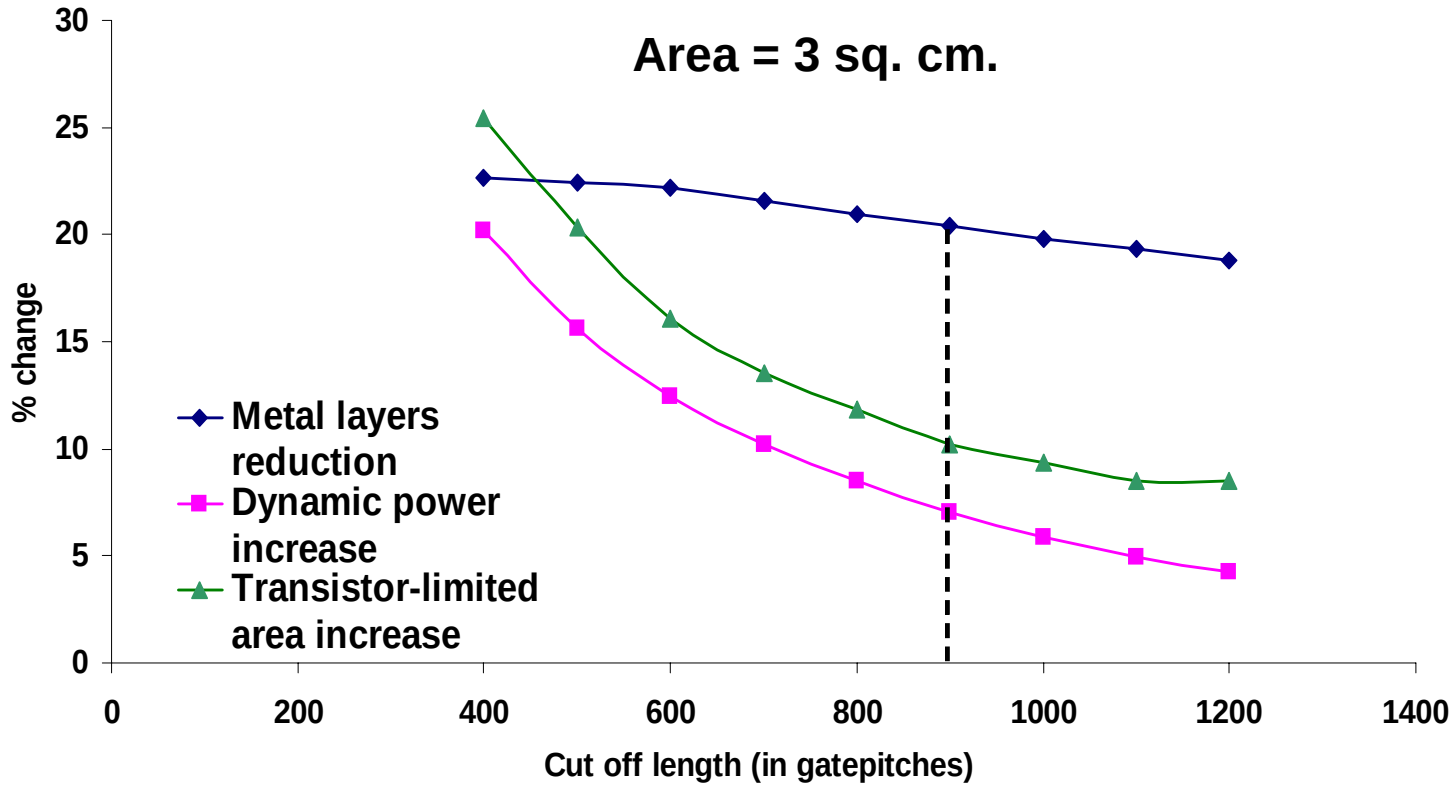

Interconnect elimination does not result in any power reduction

# Transistor-limited Area




No increase in the die area !!

# Test Case




Need to select an balanced design point where

- Significant decrease in #metal layers
- Marginal increase in dynamic power

# Results

- Wire-limited area = 3 sq.cm
- Cut-off length = 900 gatepitches

| Design metric | Metal layers | Dynamic power | Transistor-limited area |
|---|---|---|---|
| Conventional case | 8.34 | 68.03 W | 1.18 sq. cm. |
| After TDM is applied | 6.64 | 72.81 W | 1.3 sq. cm. |

- 20.38% decrease in number of metal layers
- 7.02% increase in dynamic power
- 10.16% increase in transistor limited-area

# Conclusion

- Simple wire sharing technique proposed
- Takes advantage of the interconnect idleness
- Over 20% reduction in the number of metal layers
- 15% average increase in the dynamic power

# Future Work

- Circuit Level Analysis
- Wire sharing efficiency
- Impact of inter-clock period idleness on microarchitecture