NoCIC: A Spice-based Interconnect Planning Tool Emphasizing Aggressive On-Chip Interconnect Circuit Methods

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This work was supported by SRC Tasks 766 & 1075 and a grant from Intel.

Outline

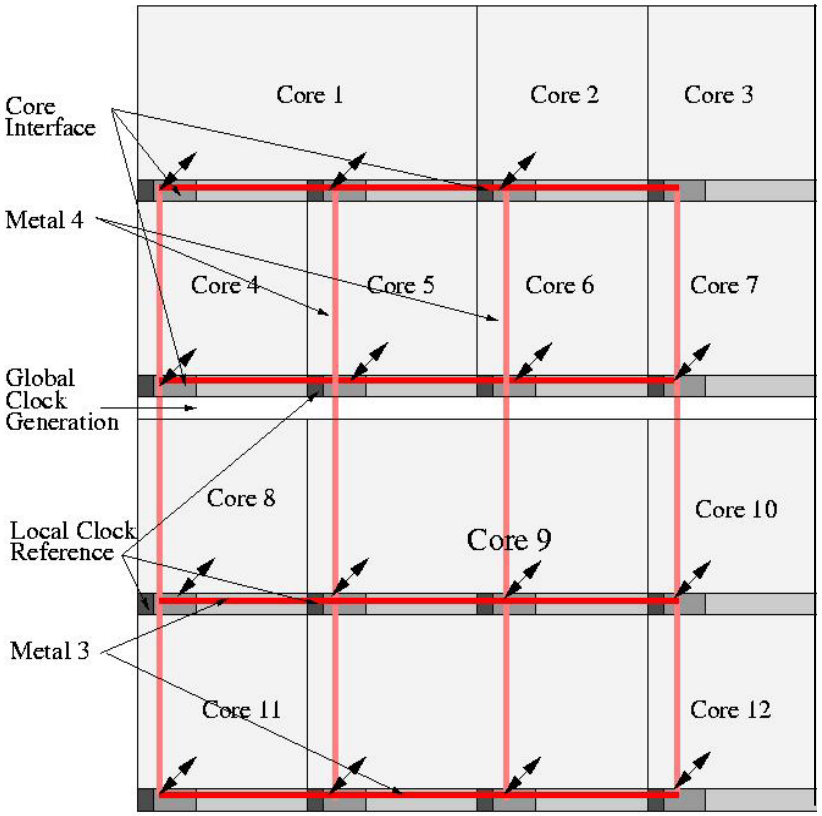
- Motivation.
- An example scenario.
- NoCIC : A solution.
- High performance circuit techniques.
- Sample results from NoCIC.
- An example scenario cont...

Nanometer design challenges

- Wires have become potential showstoppers for performance and power.
- Optimistic predictions estimate propagation delays for highly optimized global wires to be between **6 – 10 clock cycles in 50nm.** [Benini 02]
- Network-on-Chip architecture proposed to cope with interconnect effects.
- Detailed wire information required at pre-floorplan stage for effective design of NoC infrastructure.

Network-on-Chip Architecture

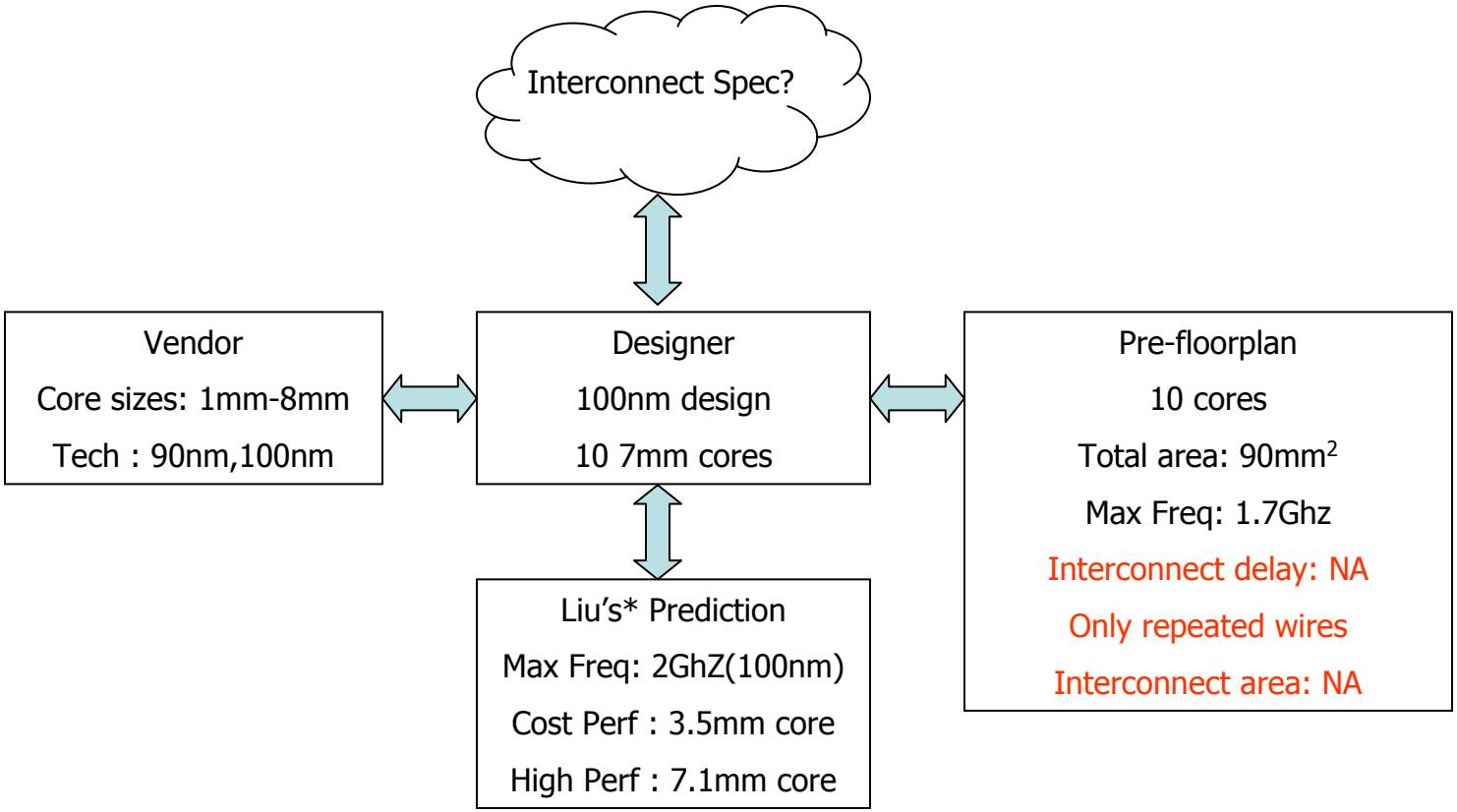
- Tiled architecture with mesh interconnect
- Point to point communication pipeline
- Allows for heterogeneous cores
  - Differing sizes, clock rates, voltages
- Regularity of the architecture eases interconnect design to a point to point communication.
- Allows for reuse of tiles.
- Regular repetition of similar wire segments which are easier to model as DSM interconnects.
- Allows the application of other high performance interconnect techniques including repeaters due to regularity in design.



RECENTLY PROPOSED NOC ARCHITECTURES

[BENINI 02], [KUMAR 02], [DALLY 01]

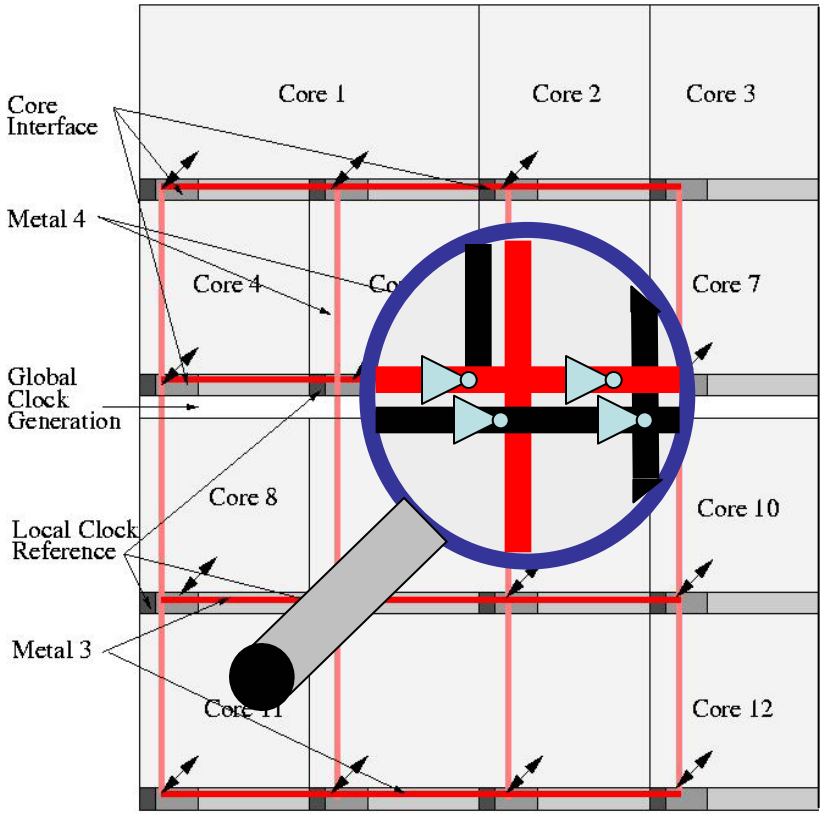
Example Scenario



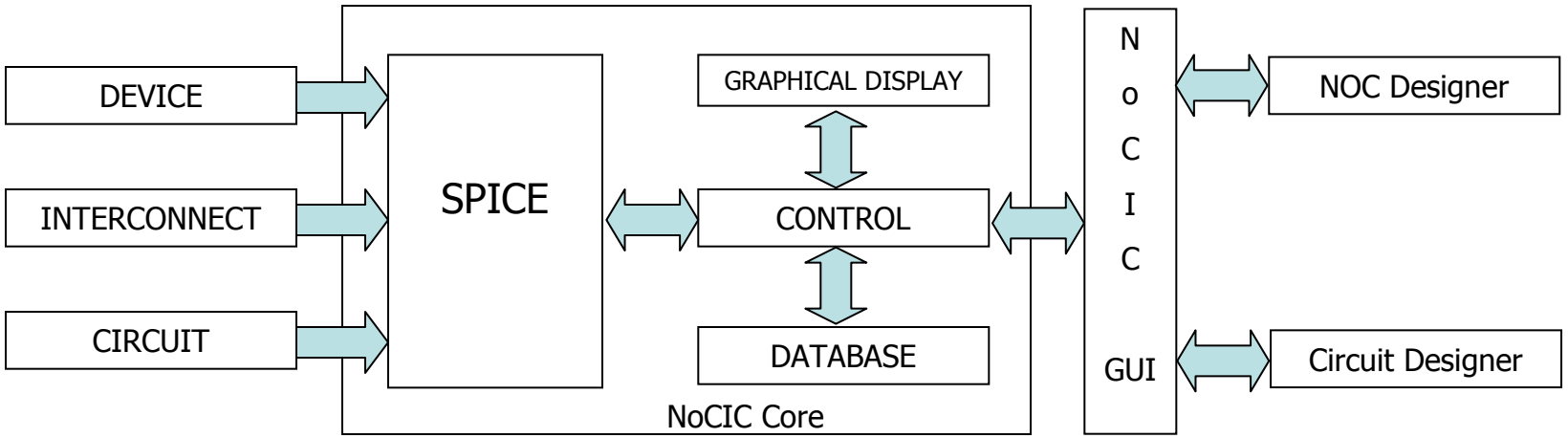
* J. Liu et.al System level interconnect design for network-on-chip interconnect IPs, *in proceedings of the international workshop on System level interconnect prediction, SLIP 2003.*

Questions from system-level designers about interconnects at pre-floorplan stage?

- Dependant parameters
  - Delay?
  - Power?
  - Active area?
  - Signal Integrity?
- Independent parameters
  - Technology scaling?
  - Signaling techniques?
  - Process variation?



NoCIC: Network-on-Chip Interconnect Calculator



- Network-on-Chip Interconnect Calculator, a spice-based tool.
- Accurately evaluate the interconnect design space.
- Choice of alternative signaling options Delay and power for interconnects displayed over a wide range of design space.

Why Spice-based analysis?

- Spice provides a relatively accurate electrical analysis of a circuit.
- These high performance circuit techniques do not have convenient closed form expressions.
- Easier to adapt to changes/advances in device and technology.
- The existing tools do not use Spice based exploration.
- Allows circuit designers see impact on NoC
- When coupled with analytical approach provides an exhaustive analysis of the design space.
- Running Spice takes a lot of design effort and time.
- Depends on the accuracy of device models.
- Does not give a direct relationship between parameters.

Analytical approaches

SUSPENS [Bakoglu 87]

BACPAC [Sylvester 99]

RIPE [Geuskens 97]

GENESYS [Eble 96]

GTX [Caldwell 02]

High Performance Interconnect Circuit techniques

- Repeater Insertion. [Alpert 97], [Adler 98], [Sylvester 99], [Ismail 00]
- Booster Insertion. [Nalmalpu 02]
- Differential current sensing. [Maheshwari 02], [Bashirullah 03]
- Multi-level current signaling. [Dhaou01], [Srinivasan 02]
- Bus-invert coding. [Stan 97]
- Low power bus coding techniques. [Sotiriadis 00]
- Static source-follower driver. [Zhang 00]
- Pseudodifferential interconnect. [Zhang 00]
- Transition Aware Global Signaling. [Kaul 02]
- Near speed-of-light signaling. [Chang 02]

A snapshot of NoCIC

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NoCIC : Network-on-Chip Interconnect Calculator

PARAMETER SELECTION WINDOW

NoC Parameters

Tile Size: 4mm

Bus Size: 8-bit

Supply Voltage: 1.8v

Interconnect Parameters

Signaling Technique: Repeater

Technology: 180nm

Shielding: Unshielded

Analysis

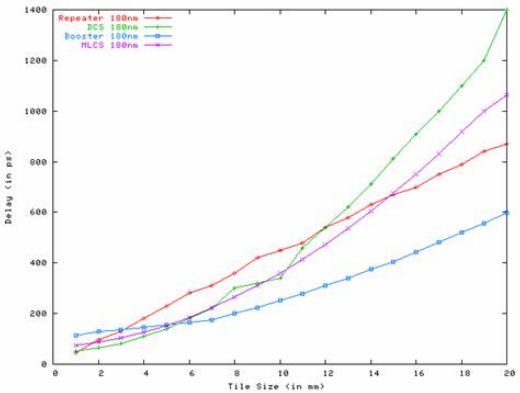
Ouput: Delay

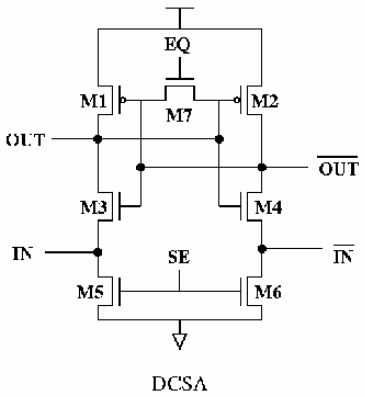
Compare:

- ☐ Repeater
- ☐ Booster
- ☐ Differential Current Sensing
- ☐ Multi-level Current Signaling

Submit Reset

PLOT DISPLAY WINDOW





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NoCIC : Network-on-Chip Interconnect Calculator

PARAMETER SELECTION WINDOW

NoC Parameters

Tile Size: 4mm (4mm, 6mm, 8mm, 10mm)

Bus Size

Supply Voltage: 1.8v

Interconnect Parameters

Signaling Technique: Repeater

Technology: 180nm

Shielding: Unshielded

Analysis

Ouput: Delay

Compare

- ☐ Repeater
- ☐ Booster
- ☐ Differential Current Sensing
- ☐ Multi-level Current Signaling

Submit Reset

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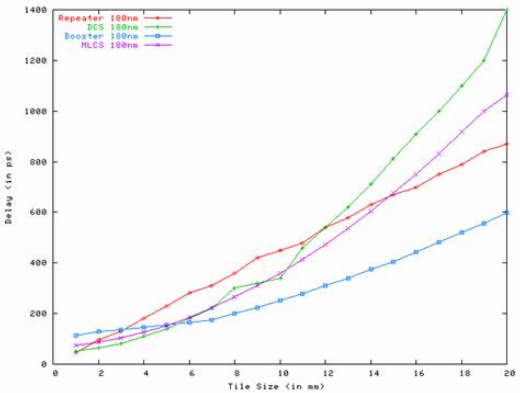

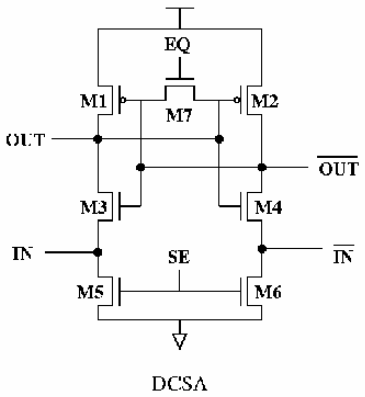

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NoCIC : Network-on-Chip Interconnect Calculator

PARAMETER SELECTION WINDOW

NoC Parameters

Tile Size: 4mm

Bus Size: 8-bit (8-bit, 16-bit, 32-bit, 64-bit)

Supply Voltage

Interconnect Parameters

Signaling Technique: Repeater

Technology: 180nm

Shielding: Unshielded

Analysis

Ouput: Delay

Compare:
- ☐ Repeater
- ☐ Booster
- ☐ Differential Current Sensing
- ☐ Multi-level Current Signaling

Submit Reset

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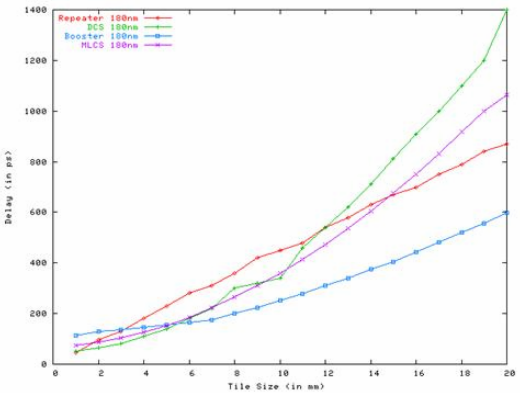

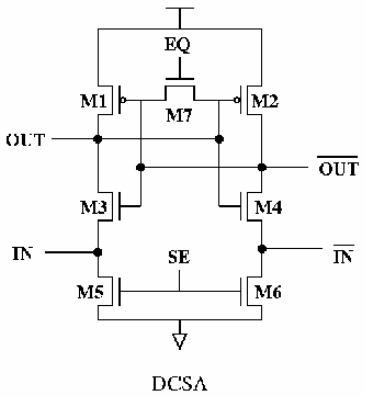

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NoCIC : Network-on-Chip Interconnect Calculator

PARAMETER SELECTION WINDOW

NoC Parameters

Tile Size: 4mm

Bus Size: 8-bit

Supply Voltage: 1.8v (1.8v, 1.3v, 1.1v, 0.7v)

Interconnect Parameters

Signaling Technique: Repeater

Technology: 180nm

Shielding: Unshielded

Analysis

Ouput: Delay

Compare:
- ☐ Repeater
- ☐ Booster
- ☐ Differential Current Sensing
- ☐ Multi-level Current Signaling

Submit Reset

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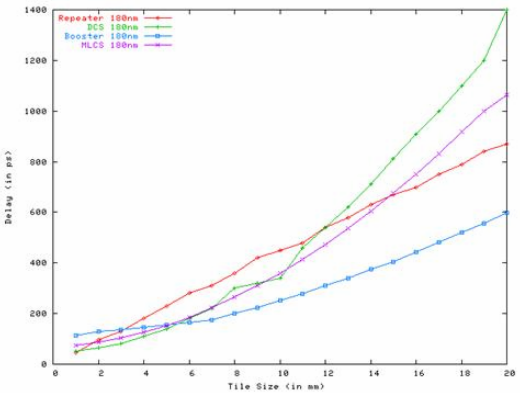

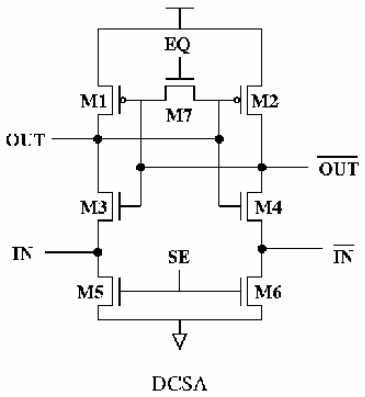

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PARAMETER SELECTION WINDOW

NoC Parameters

Tile Size: 4mm

Bus Size: 8-bit

Supply Voltage: 1.8v

Interconnect Parameters

Signaling Technique: Repeater

Technology

Shielding: Unshielded

- Repeater
- Booster
- Differential Current Sensing
- Multi-level current signaling

Analysis

Ouput: Delay

Compare

- ☐ Repeater
- ☐ Booster
- ☐ Differential Current Sensing
- ☐ Multi-level Current Signaling

Submit Reset

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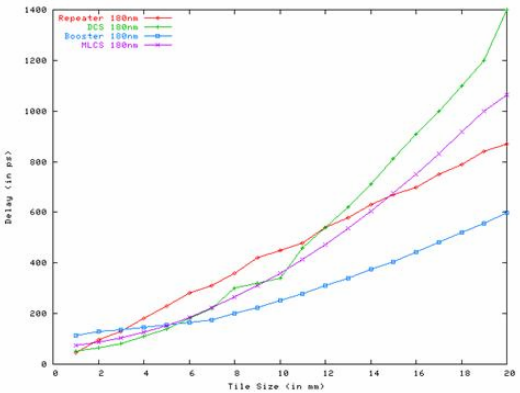

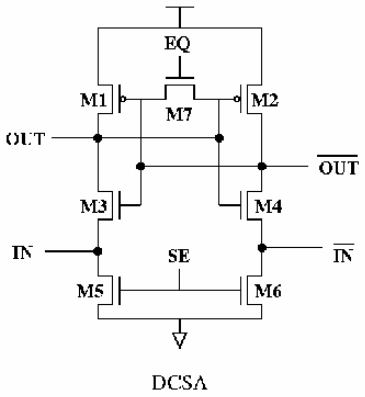

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NoCIC : Network-on-Chip Interconnect Calculator

PARAMETER SELECTION WINDOW

NoC Parameters

Tile Size: 4mm

Bus Size: 8-bit

Supply Voltage: 1.8v

Interconnect Parameters

Signaling Technique: Differential Current Sensing

Technology: 180nm (180nm, 130nm, 100nm, 70nm)

Shielding: d

Analysis

Ouput: Delay

Compare:
- ☐ Repeater
- ☐ Booster
- ☐ Differential Current Sensing
- ☐ Multi-level Current Signaling

Submit Reset

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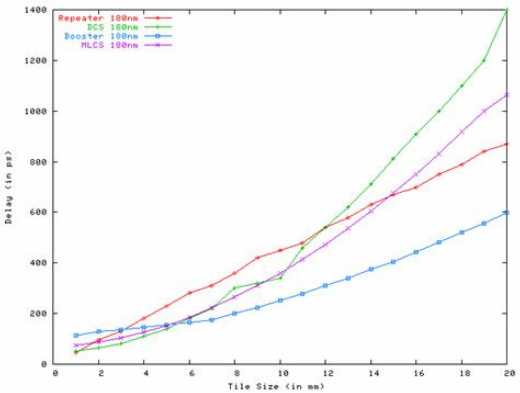

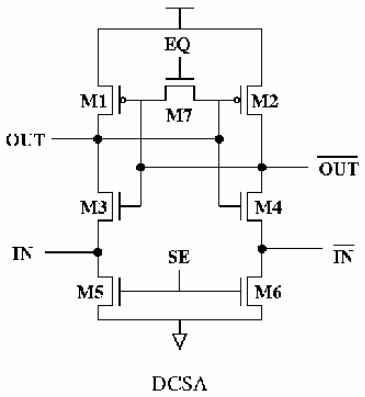

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NoCIC : Network-on-Chip Interconnect Calculator

PARAMETER SELECTION WINDOW

NoC Parameters

Tile Size: 4mm

Bus Size: 8-bit

Supply Voltage: 1.8v

Interconnect Parameters

Signaling Technique: Differential Current Sensing

Technology: 180nm

Shielding: Unshielded (Unshielded / Full shielding)

Analysis

Ouput: Delay

Compare:
- ☐ Repeater
- ☐ Booster
- ☐ Differential Current Sensing
- ☐ Multi-level Current Signaling

Submit Reset

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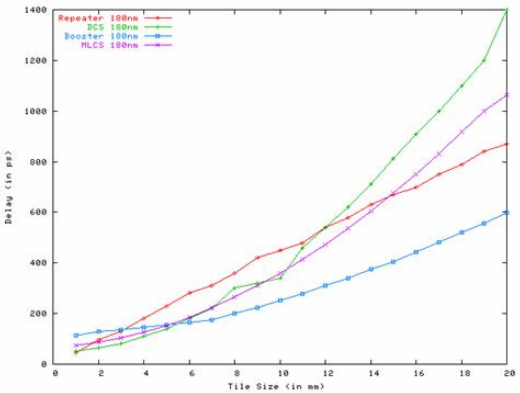

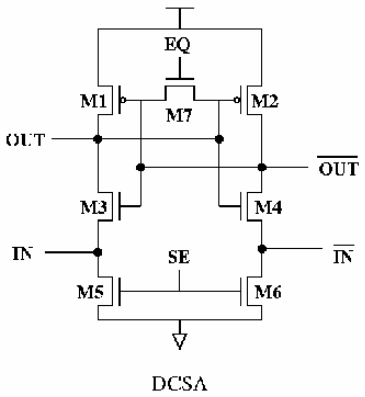

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NoCIC : Network-on-Chip Interconnect Calculator

PARAMETER SELECTION WINDOW

NoC Parameters

Tile Size: 4mm

Bus Size: 8-bit

Supply Voltage: 1.8v

Interconnect Parameters

Signaling Technique: Differential Current Sensing

Technology: 180nm

Shielding: Unshielded

Analysis

Ouput: Delay (Delay, Power, Active Area, Signal Integrity)

Compare

Booster

Differential Current Sensing

Multi-level Current Signaling

Submit Reset

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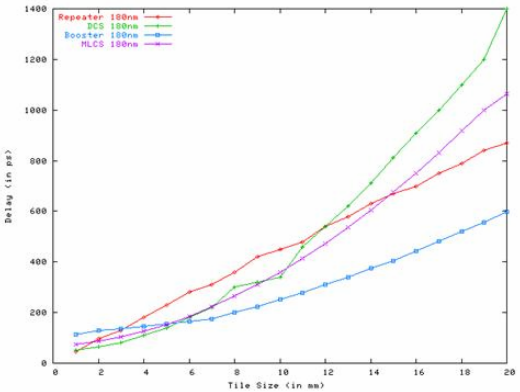

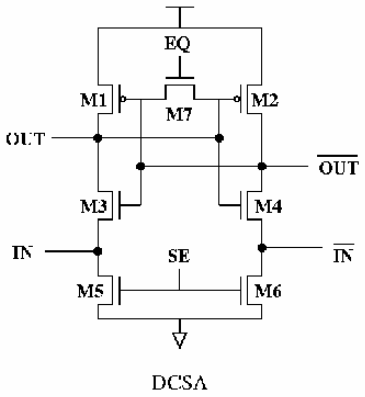

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Advantages of NoCIC

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NoCIC : Network-on-Chip Interconnect Calculator

PARAMETER SELECTION WINDOW

NoC Parameters

Tile Size: 4mm

Bus Size: 8-bit

Supply Voltage: 1.8v

Interconnect Parameters

Signaling Technique: Differential Current Sensing

Technology: 180nm

Shielding: Unshielded

Analysis

Ouput: Delay

Compare:
- [x] Repeater
- [x] Booster
- [ ] Differential Current Sensing
- [x] Multi-level Current Signaling

Submit Reset

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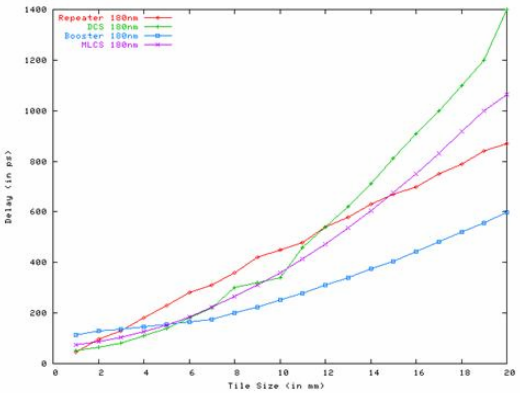

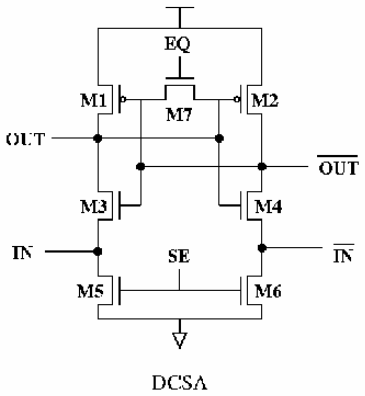

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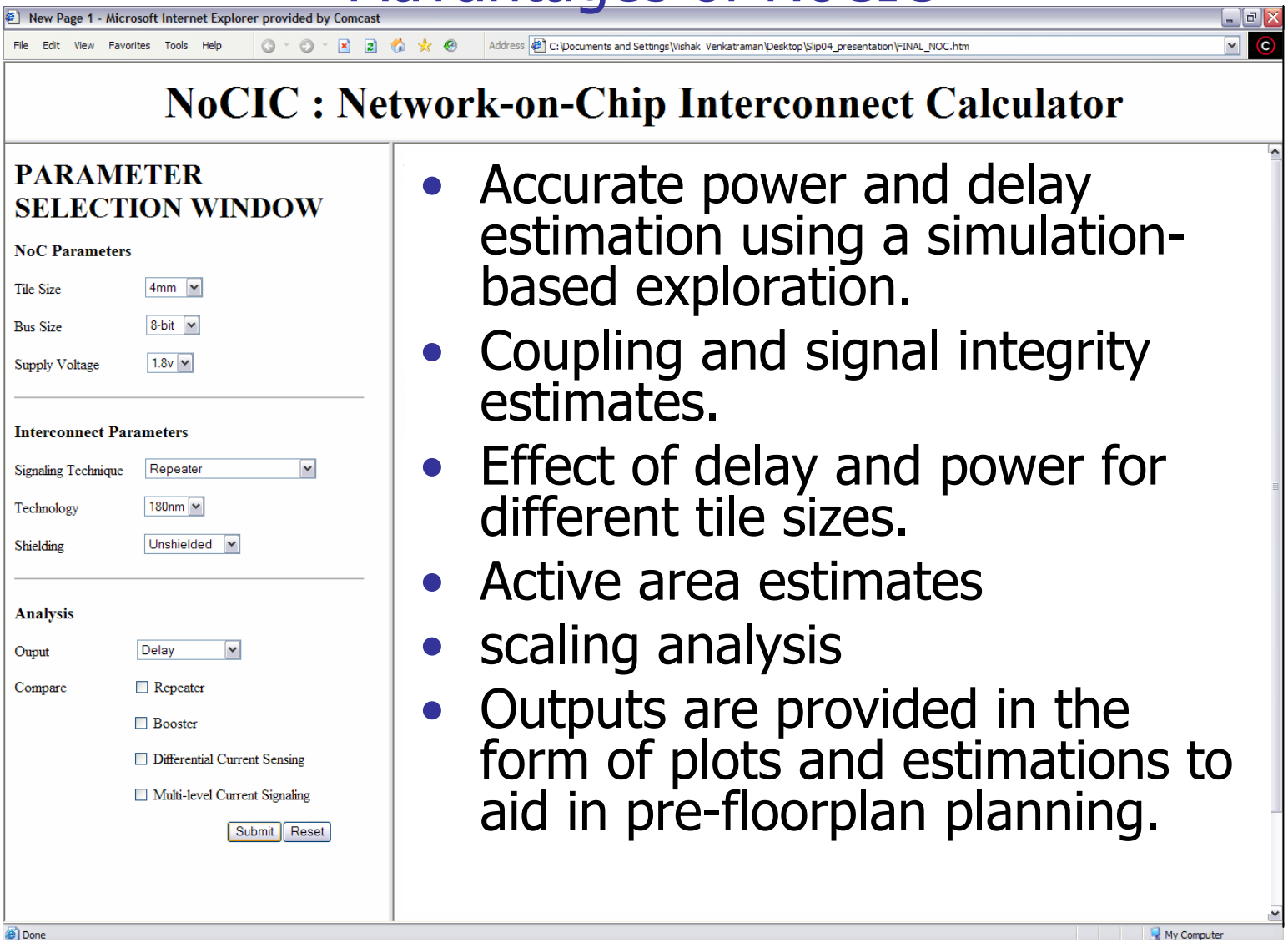
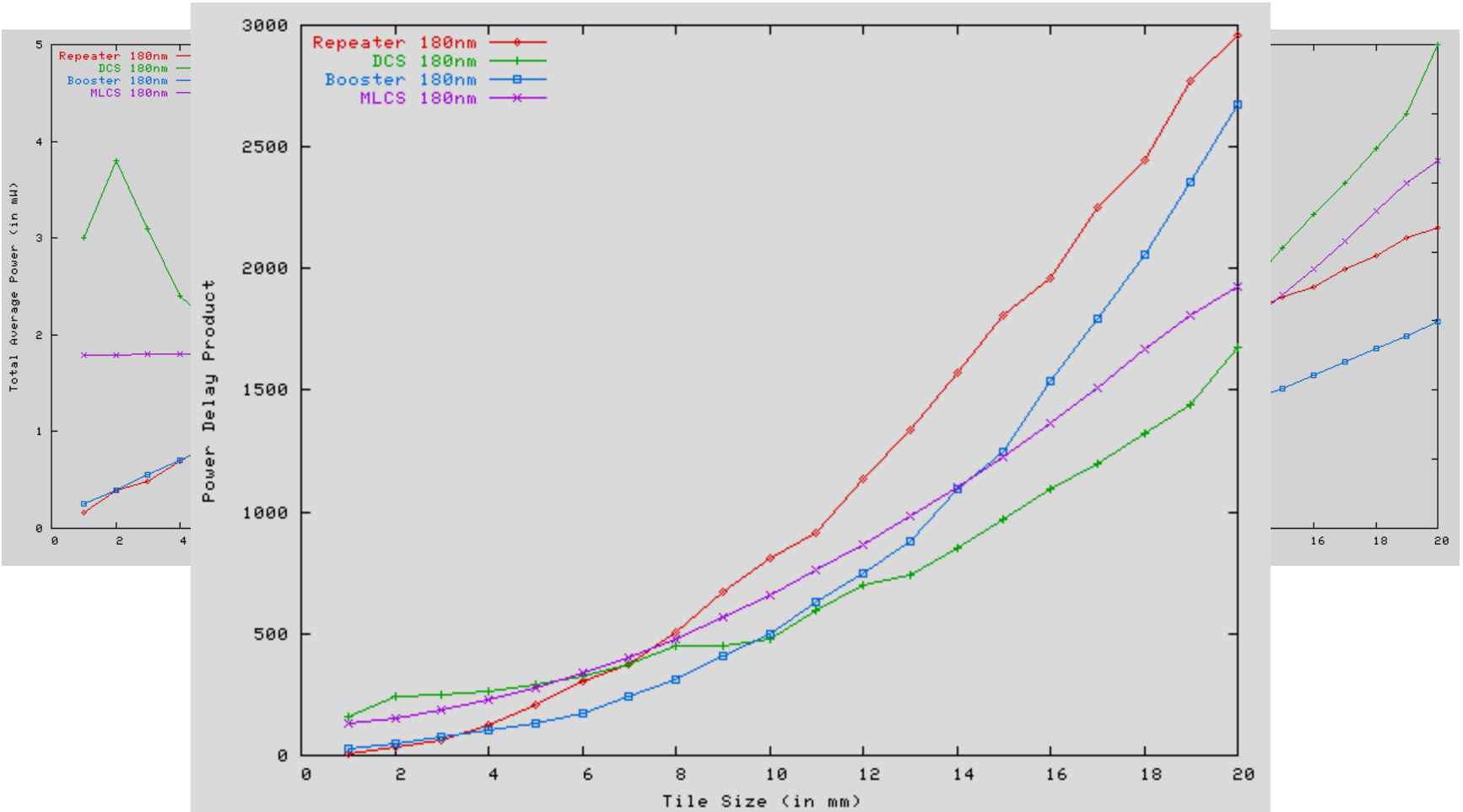
Advantages of NoCIC



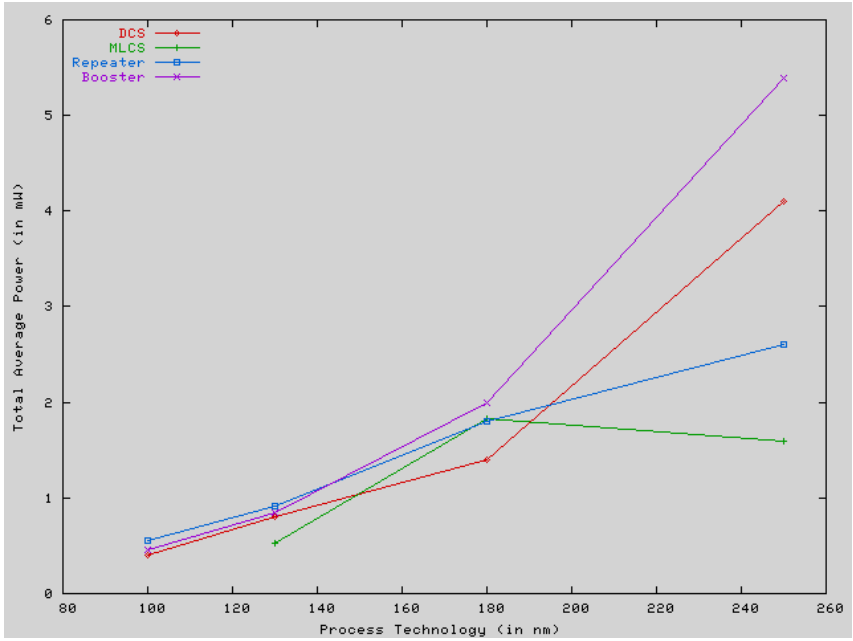
- Accurate power and delay estimation using a simulation-based exploration.
- Coupling and signal integrity estimates.
- Effect of delay and power for different tile sizes.
- Active area estimates
- scaling analysis
- Outputs are provided in the form of plots and estimations to aid in pre-floorplan planning.

Effects of tile size

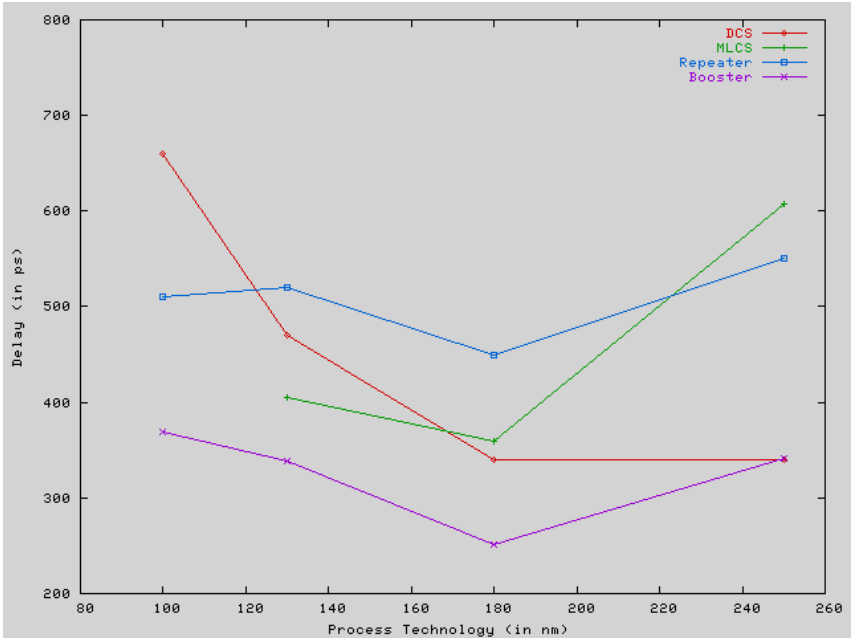


POWER DELAY PRODUCT

Scaling analysis

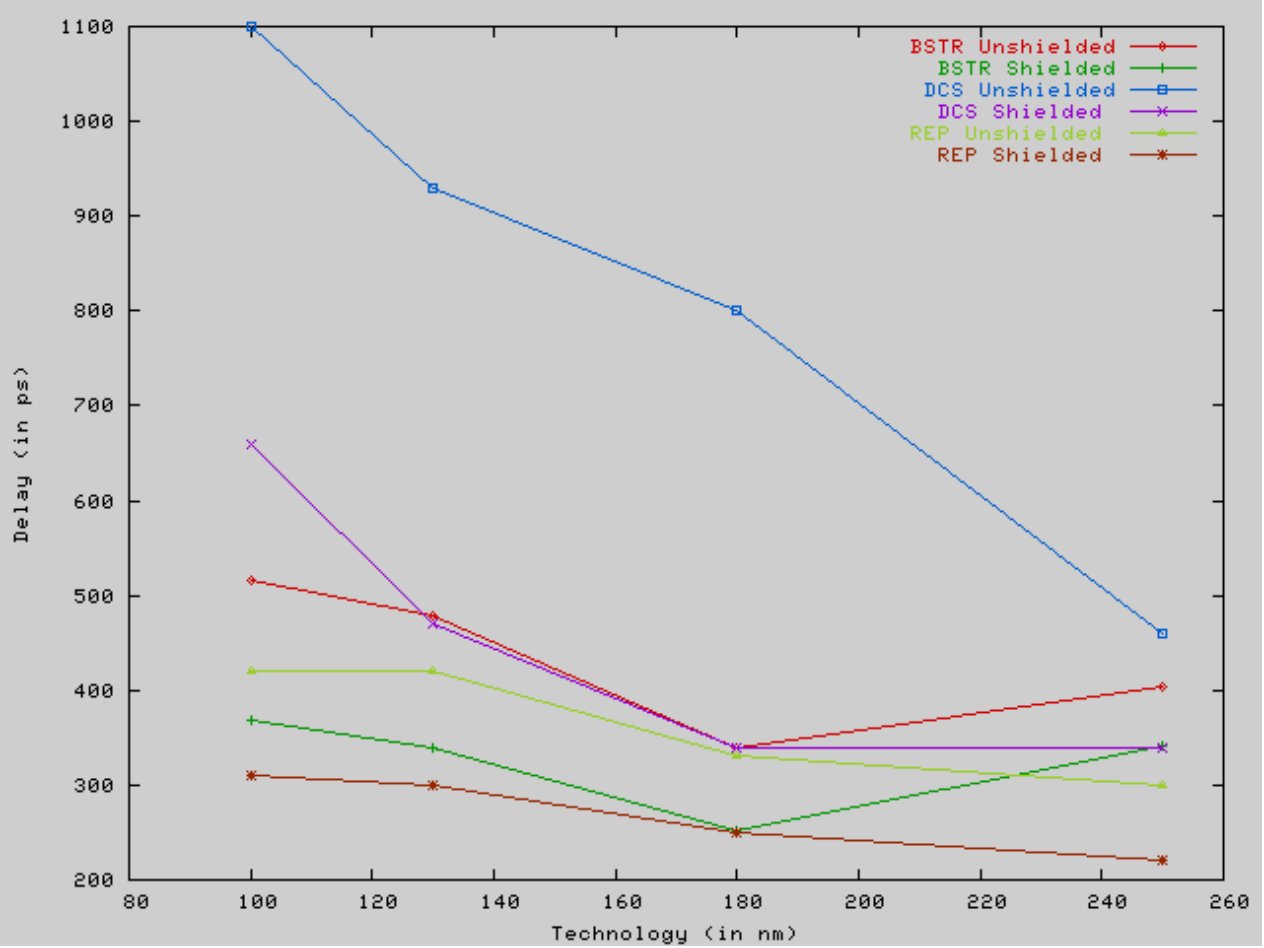


Power

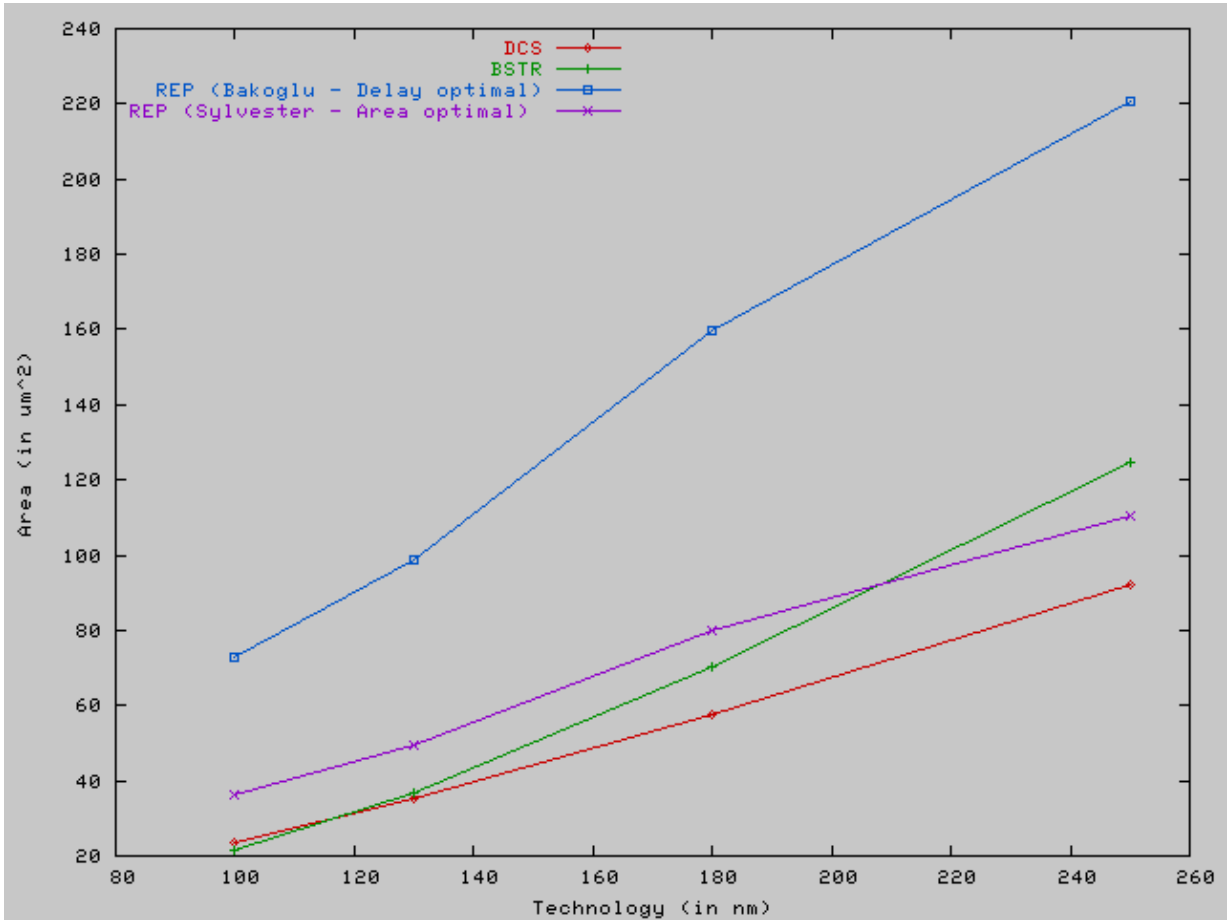


Delay

Coupling analysis



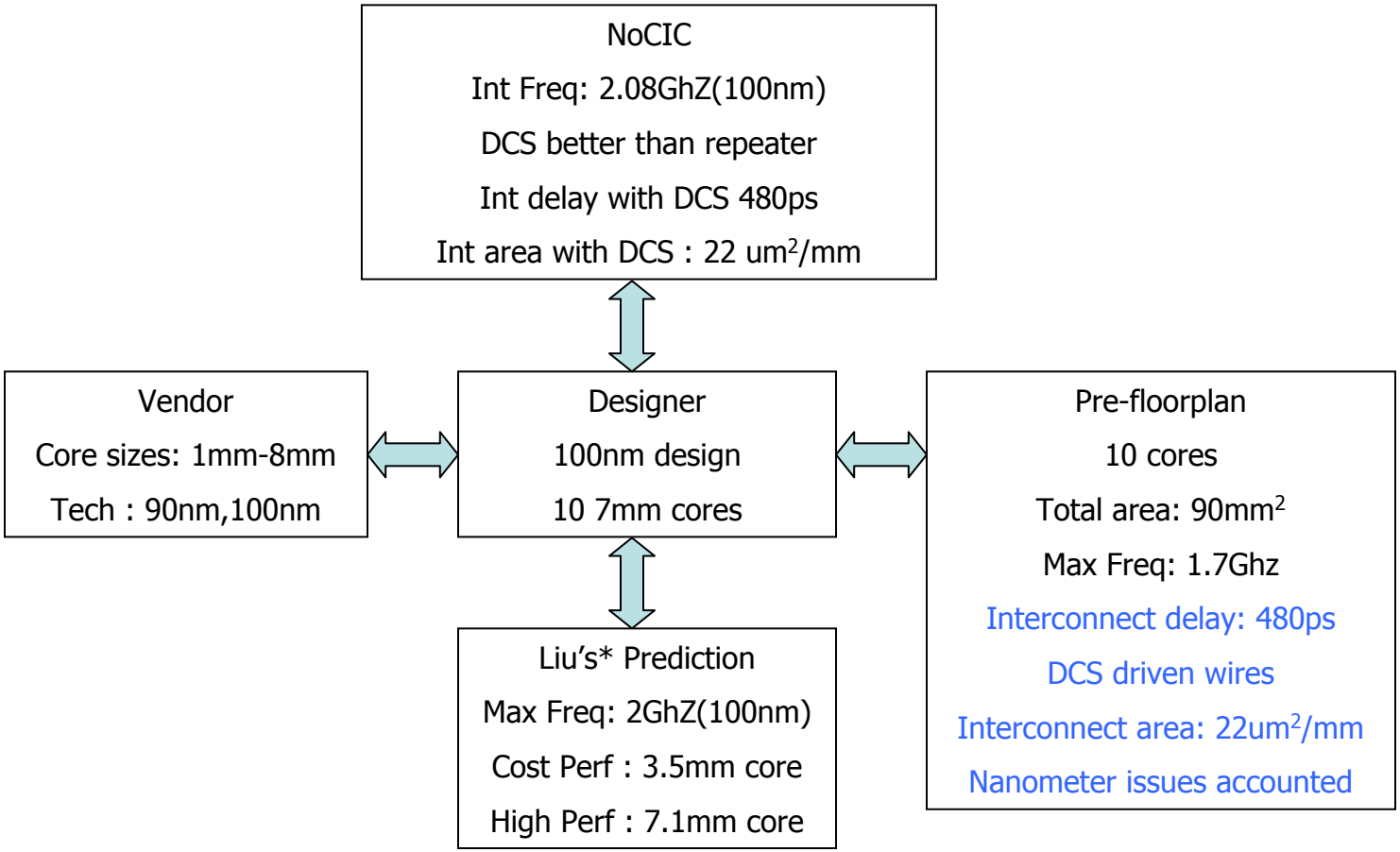
Active area analysis



Modeling error Vs NoCIC (Spice)

Technology	Absolute Error (ps)		Relative Error	
	Mean	Standard Deviation	Mean	Standard Deviation
70nm	128.10	69.77	0.37	0.03
100nm	146.45	81.52	0.33	0.05
130nm	132.00	81.26	0.28	0.09
180nm	88.65	63.86	0.21	0.09

Example Scenario cont…



∗ J. Liu et.al, System level interconnect design for network-on-chip interconnect IPs, *in proceedings of the international workshop on System level interconnect prediction, SLIP 2003*.

Conclusion

- NoCIC, a spice-based interconnect tool was implemented.
- Sample results from NoCIC was presented
  - Area and coupling analysis.
  - Effects of tile size.
  - Scaling analysis.
- This tool hopes to aid NoC architects to efficiently evaluate interconnect issues.
- Serve as a pre-floorplan tool providing detailed interconnect information.
- Provides a bridge between circuit and NoC.
- Can be used to develop new analytical models.

Future work

- Add more signaling techniques.
- Run real-time HSPICE simulations on user given values.
- Interconnect synthesis tool with optimization techniques.
- Add new parameters.
- Study of inductance effects, signal integrity and reliability.
- Feasibility of NoCIC to be added as a signaling technique analysis tool in GTX.

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