Invited Talk
Optical Solutions for System-Level Interconnect

Ian O'Connor, F. Gaffiot, F. Mieyeville
G. Tosik, F. Tissafi-Drissi, M. Brière

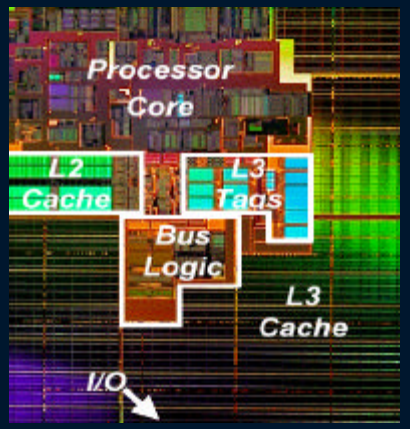
Laboratory of Electronics, Optoelectronics and Microsystems
Ecole Centrale de Lyon
36 avenue Guy de Collongue, F-69134 Ecully, France

Outline

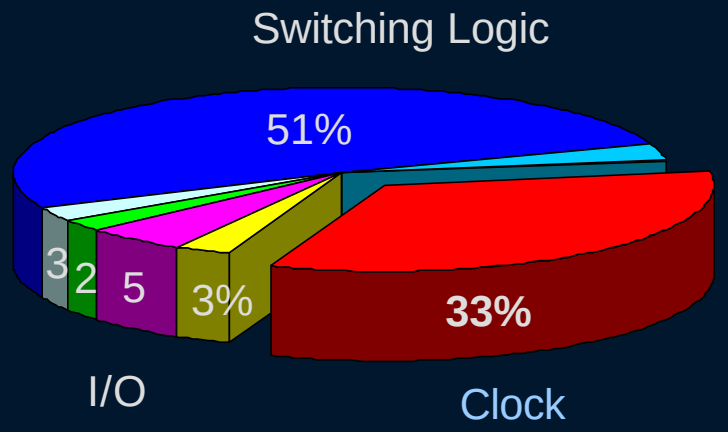
- Context and motivations for optical interconnect
  - ITRS
  - Optical interconnect technology
  - Target applications
- Clock distribution
  - Structure and global design methodology
  - Interface circuit characteristics
  - Calculating losses in passive devices
  - Electrical-optical comparison
- Wavelength-reconfigurable networks on chip
  - Target functionality
  - Modelling and design environment
  - Architecture of reconfigurable network

Context

- the interconnect problem: **"For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, RF, or vertical integration ... will deliver the solution"** (International Technology Roadmap for Semiconductors 2003)



Itanium IA-64

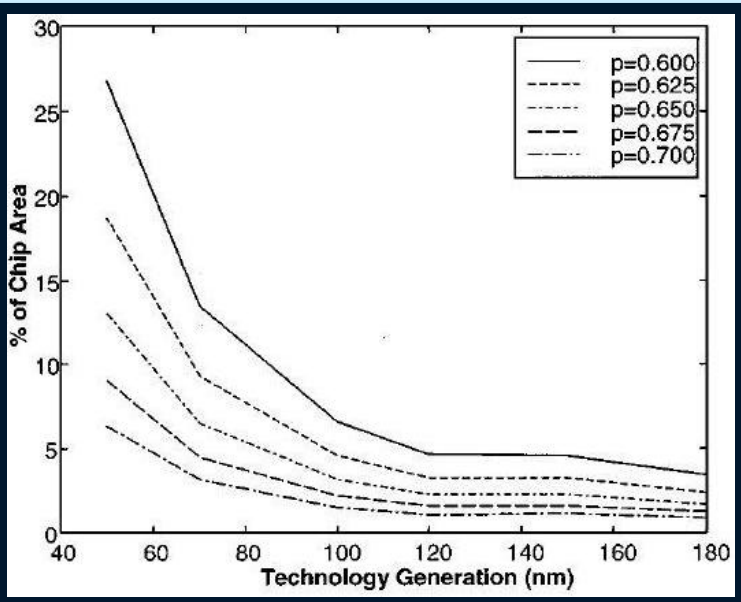


The optical alternative

- optical interconnect to:
  - increase throughput
  - reduce power dissipation
  - alleviate thermal constraints
  - reduce crosstalk
  - decrease skew
  - reduce signal distortion
  - simplify place-and-route for complex circuits
- but:
  - requires high-speed low-power interface circuits
  - process modifications
  - few quantitative analyses exist

Target applications

- point-to-point (1-1) links?
  - routing complexity
  - number of repeaters
    - power
    - silicon real estate

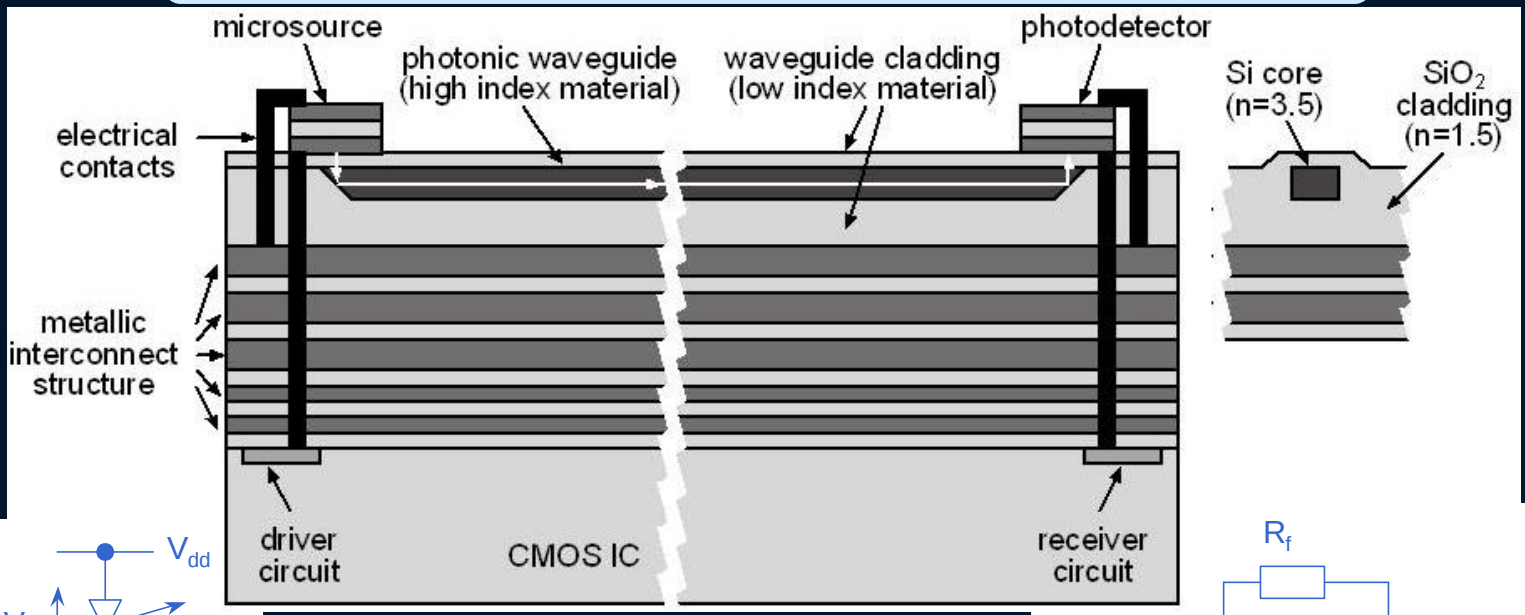


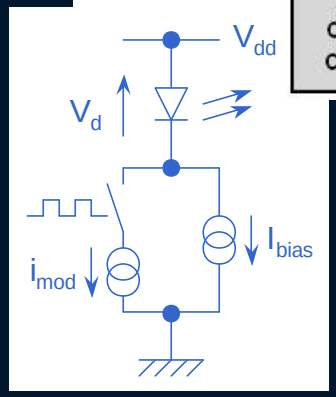
K. Banerjee et al., Proc. IEEE, May 2001

- broadcast (1-N) links (clock distribution)
  - timing
  - clock noise
  - power and thermal issues
- network (N-N) links
  - throughput

Structure of integrated optical interconnect

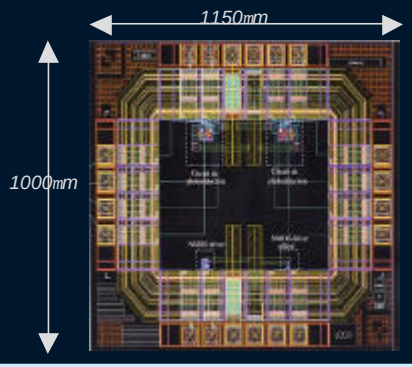
heterogeneous III-V on Si intégration

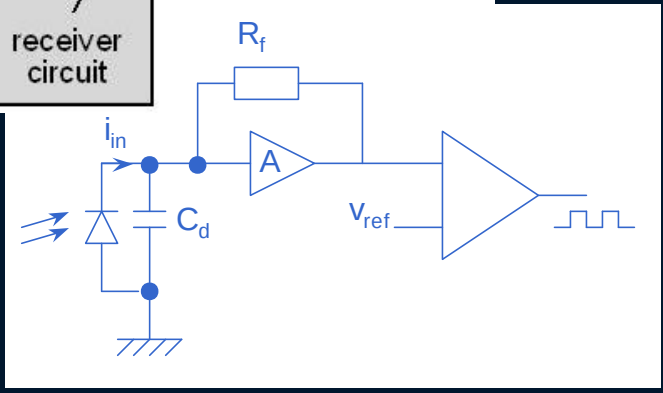




driver circuit

2.5Gb/s realisation (ST CMOS 0.25um)





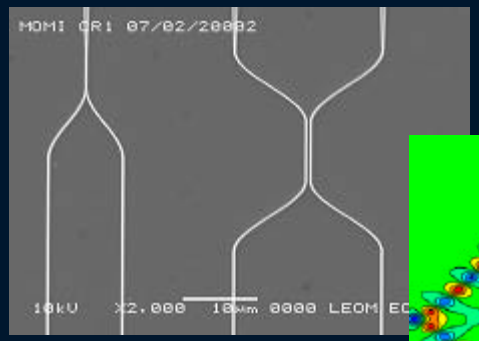
receiver circuit

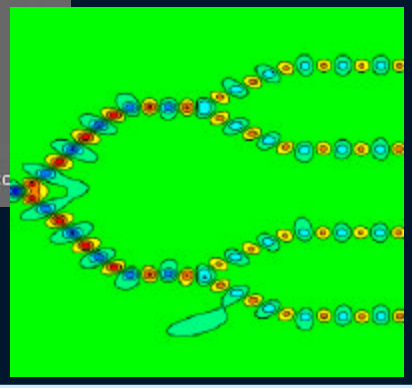
Passive photonic devices

couplers, filters, routers

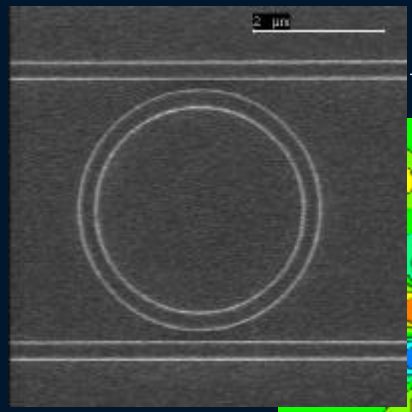
- SOI guides
- Transmission at 1,55µm
- intra-chip optical links

signal transport = waveguides and couplers

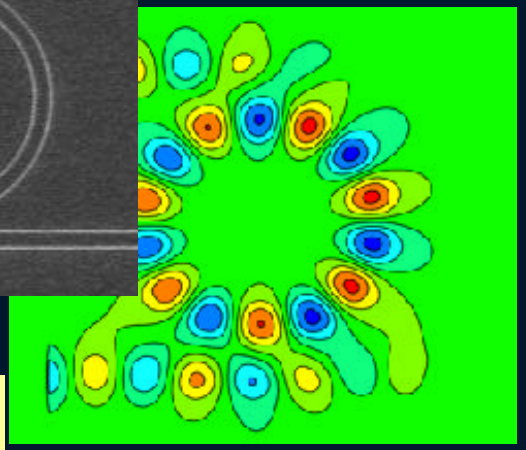




$\lambda_i \rightarrow$



$\rightarrow$ if $\lambda_i \neq \lambda_k$



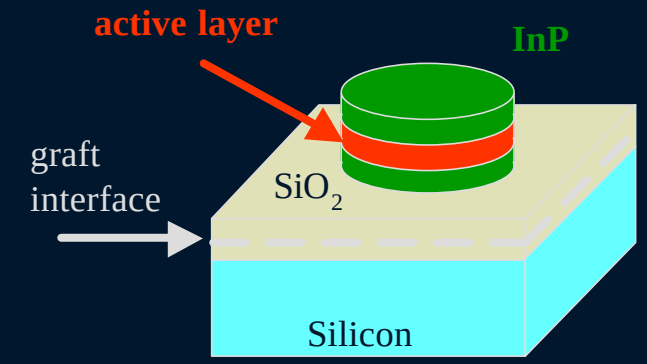
if $\lambda_i = \lambda_k \leftarrow$

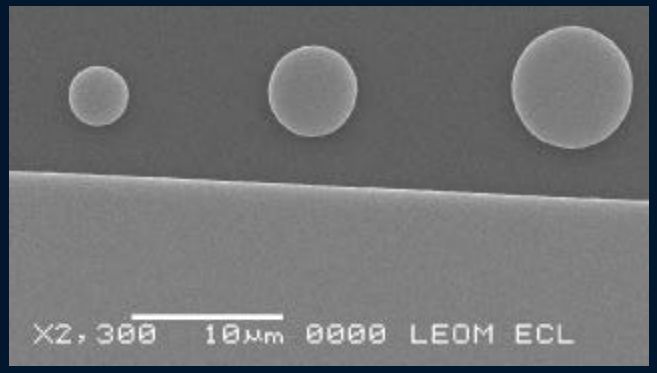
1-switch = add-drop filter

- resonance mode λ_k depends on disc radius (um)

Active devices

lasers





C. Seassal et al., IEE Electron. Lett., 2001

VCSEL
(vertical cavity surface emitting laser) :
- high-wavelength & low-threshold difficult
- coupling difficult (vertical emission)

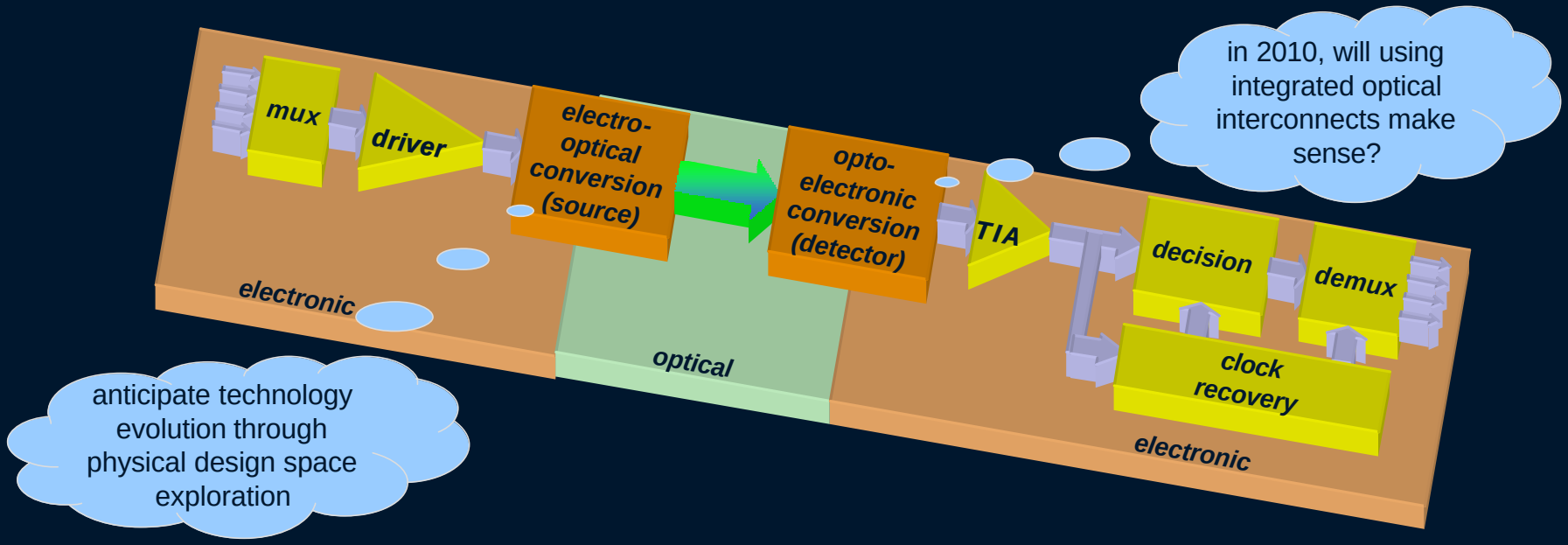
850nm, 70uA threshold current, 2.6um diameter CMOS compatible VCSEL
(Liu, J.J. et al., Ultralow-threshold sapphire substrate-bonded top-emitting 850-nm VCSEL array, *IEEE Phot. Lett.*, 14, 1234, 2002)

Microlasers :
- heterogeneous integration (InP on Si)

Technological simplification
- Coupling to passive SOI guide
- Thermal dissipation → low threshold

Photonic crystals ...

Optical interconnect design problems



- concurrent design of electronic and optical parts for optical interconnect
  - use of predictive models (technology does not yet exist)
  - generic design methodologies and models

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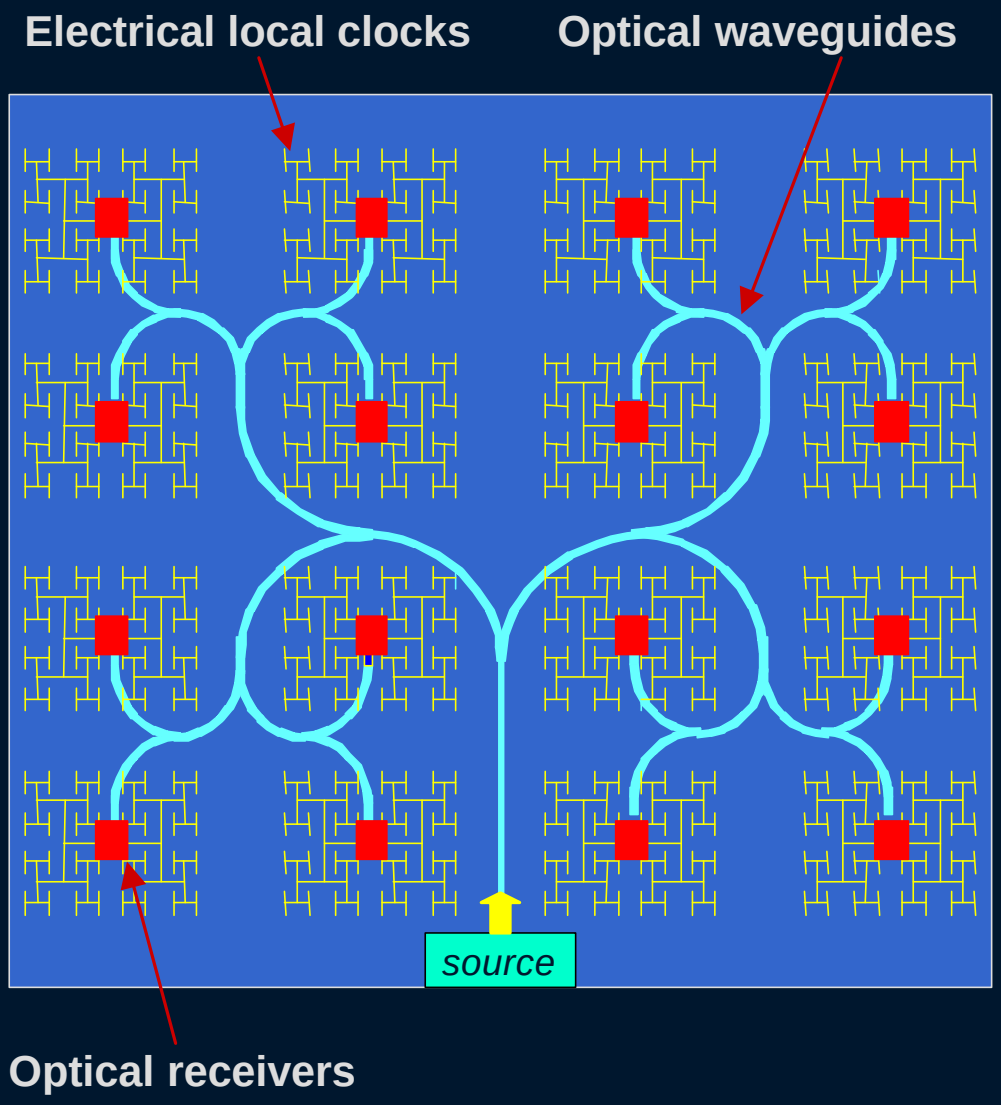
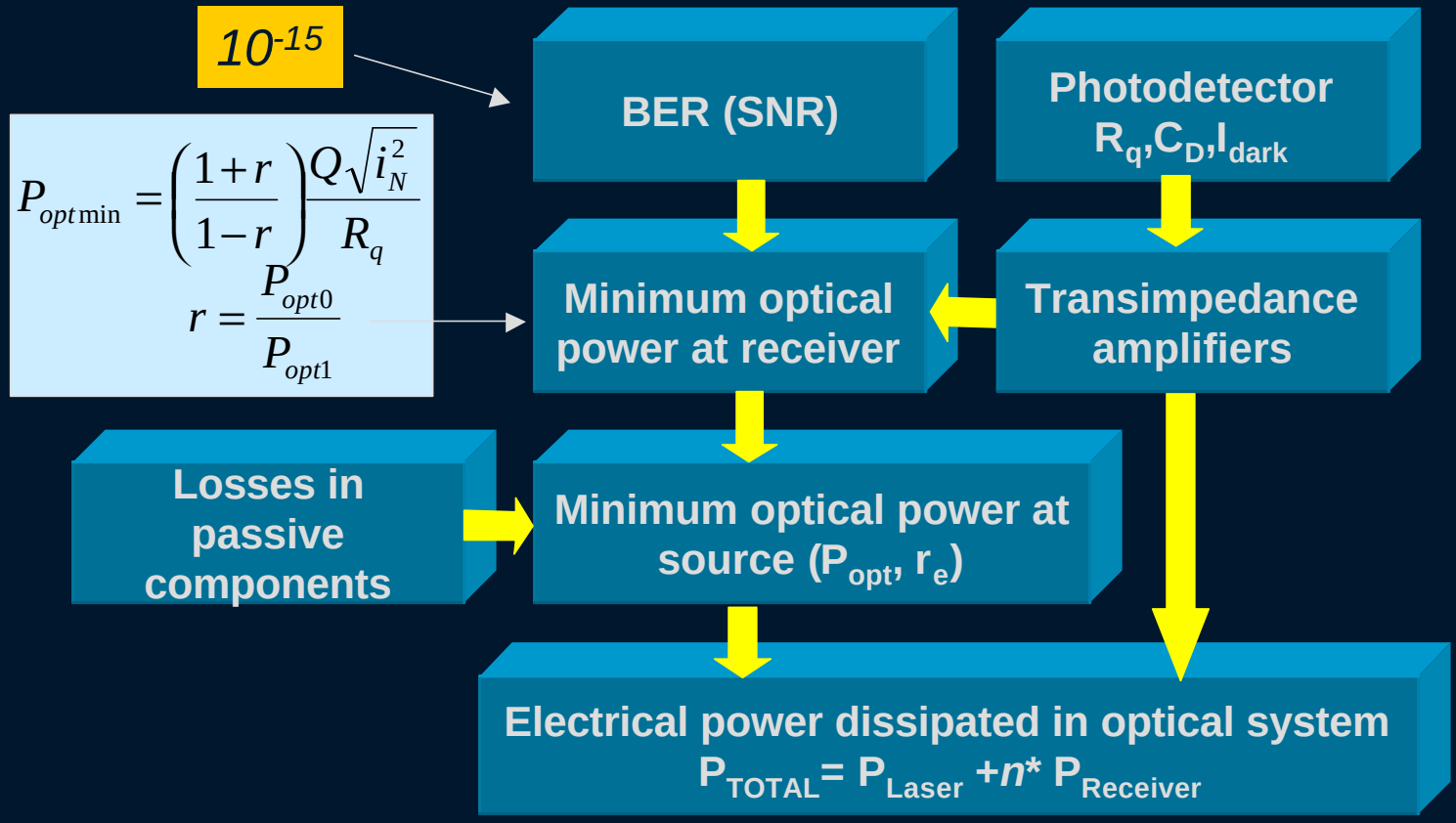
Clock distribution network (1-N)



Calculating the power budget

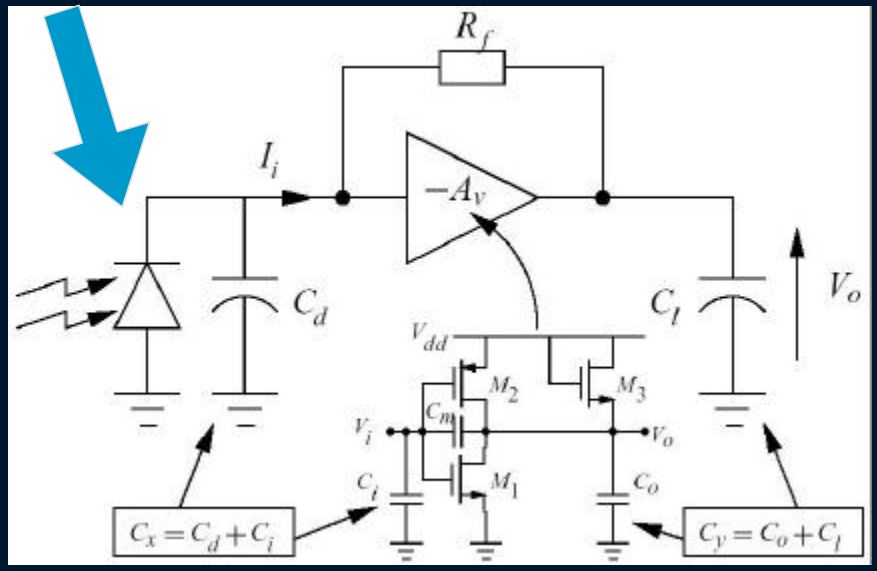
- the route to calculating overall optical interconnect power is based on required signal quality (BER)



Determining TIA characteristics

- simple analytical equations for transistor characteristics insufficient (>100% error)
- but extraction requires transistor-level schematics
- synthesis

R_q critical for power
C_d critical for data rate

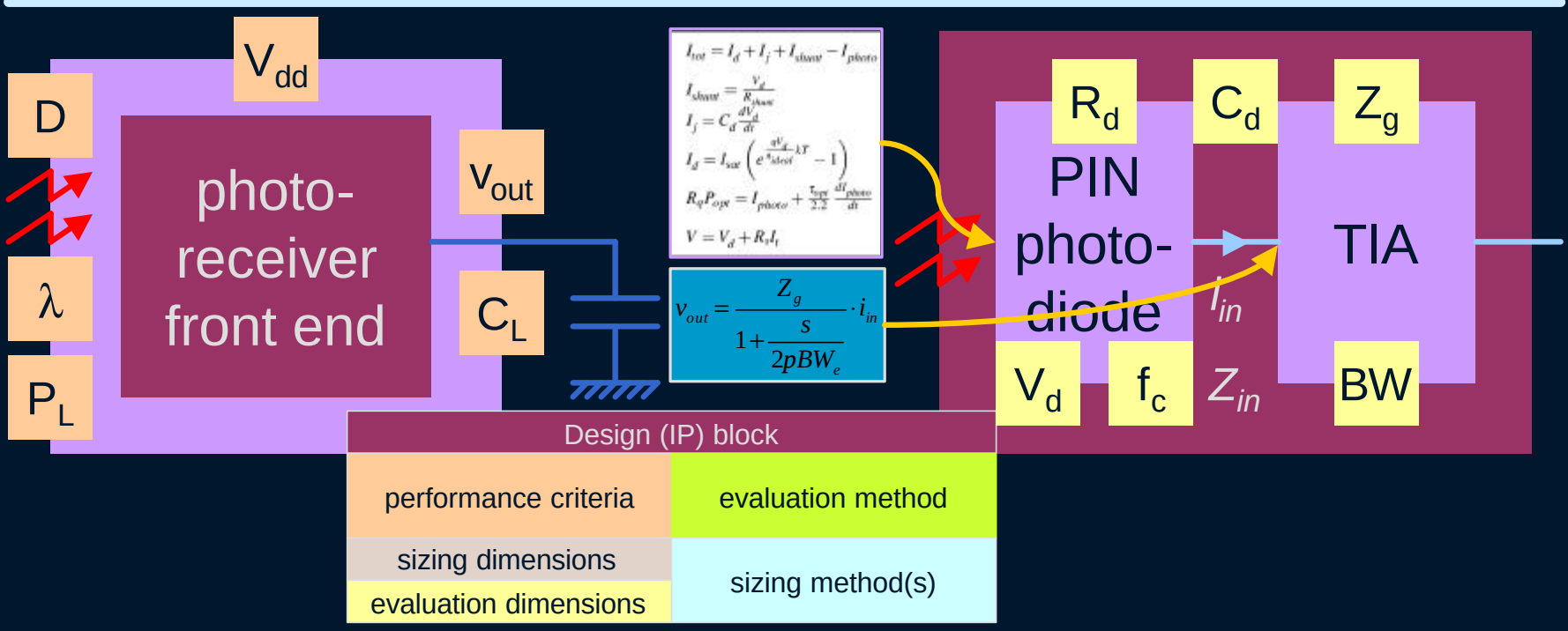


total noise at photoreceiver

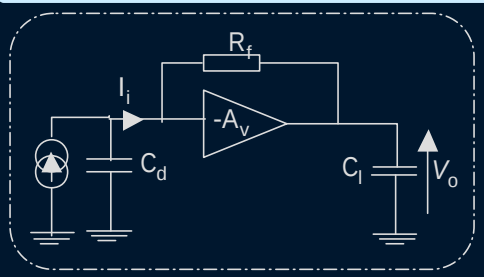
$$\sqrt{\overline{i_N^2}} = \left(2q\left(I_{gate} + I_{dark}\right) + \frac{4kT}{R_f} \right) \frac{C}{4D} + 4kT\Gamma \frac{C^2}{16p^2 DE} \frac{\left(2pC_T\right)^2}{g_m}$$

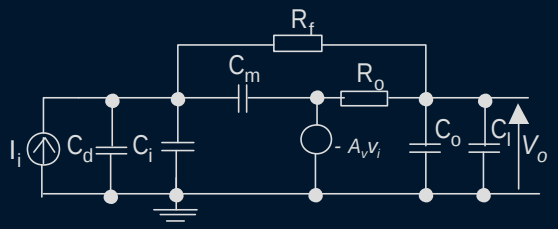
J.J. Morikuni et al., IEEE J. Lightwave Tech., July 1994

Photoreceiver front-end IP block



TIA synthesis





$$Z_{g0} = \frac{R_o - R_f A_v}{1 + A_v}$$

$$w_0 = \frac{1}{R_0 Cy}\sqrt{\frac{1 + A_v}{M_f\left(M_x + M_m + M_x M_m\right)}}$$

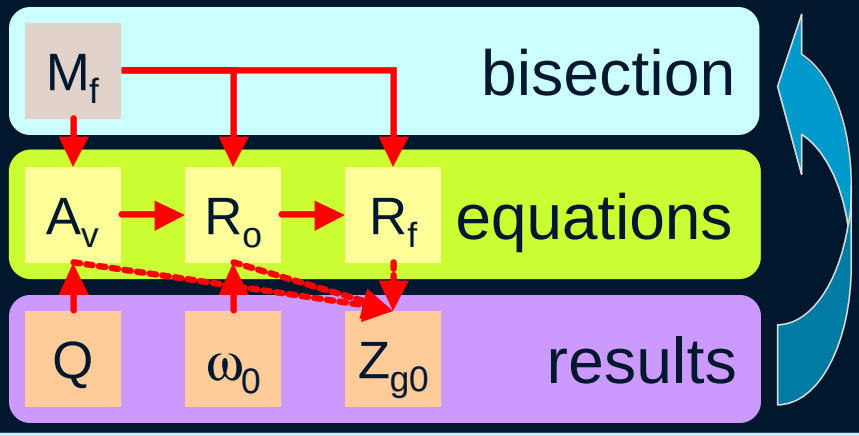
$$Q = \frac{\sqrt{M_f(1 + A_v)\left(M_x + M_m(1 + M_x)\right)}}{1 + M_x(1 + M_f) + M_m M_f(1 + A_v)}$$

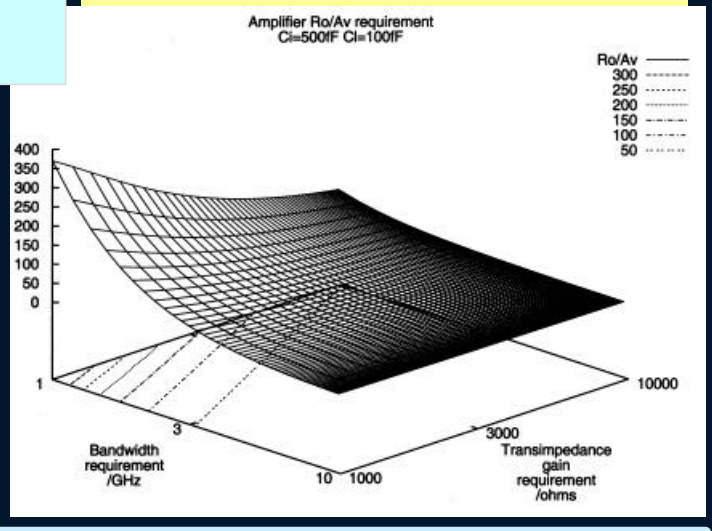
- sizing TIA with iterative procedure
- accurate specification tolerance
- systematic convergence

$Q = 1/\sqrt{2}$ ➡ Maximize bandwidth

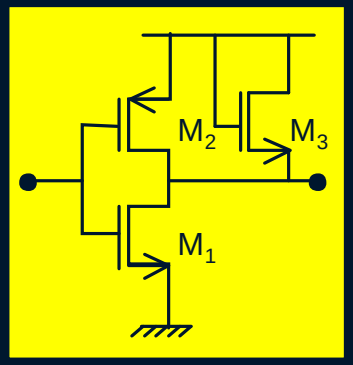
Design (IP) block	
performance criteria	evaluation method
sizing dimensions evaluation dimensions	sizing method(s)

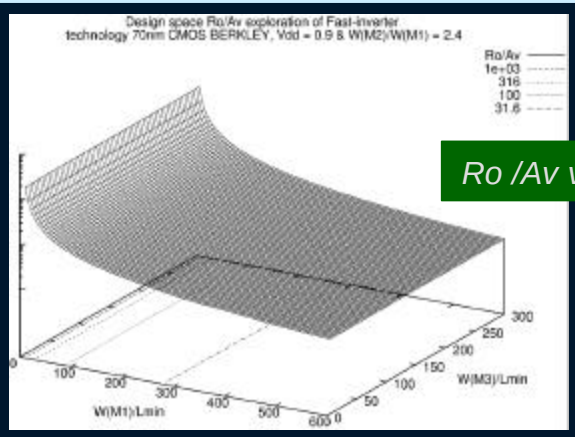
"Design ease" R_o/A_v against bandwidth and transimpedance gain





Fast inverter IP block





Ro /Av vs W_i

A_{v0}	> 7	7.32
R_0	< 1kΩ	221Ω
Pwr	< 4.5mW	4.3mW
F_i	= 1	1.005
V_o	= 0.5V	0.472

100nm CMOS

Design (IP) block	
performance criteria	evaluation method
sizing dimensions	sizing method(s)
evaluation dimensions	

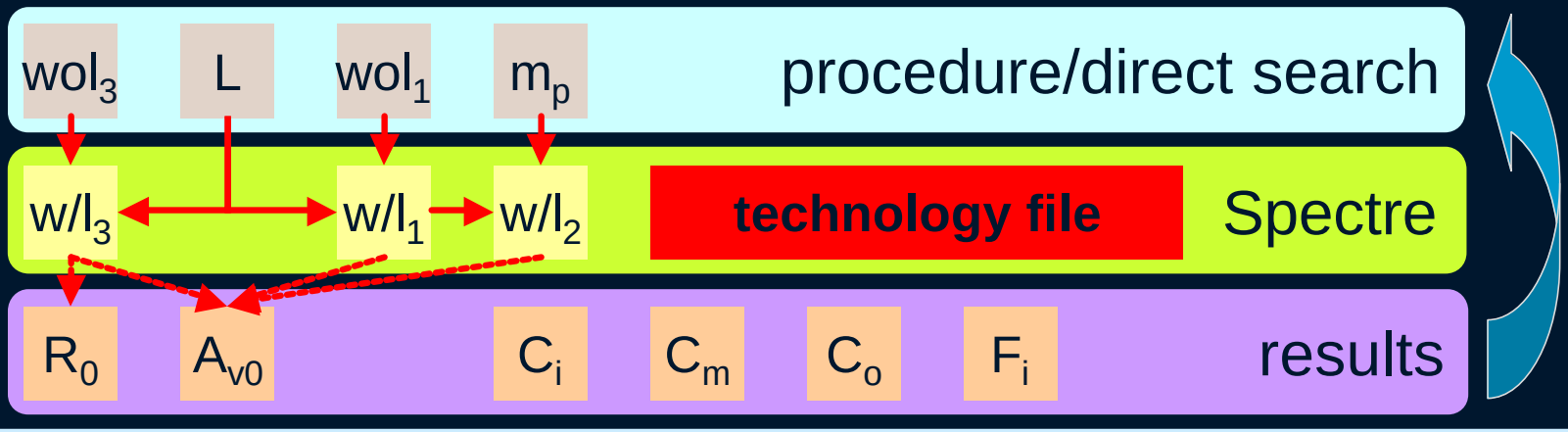
relations

$g_{mt} = g_{m1}+g_{m2} = A_v/R_o$

g_{m1}/g_{m2} 🕓 v_{gst2}/v_{gst1}

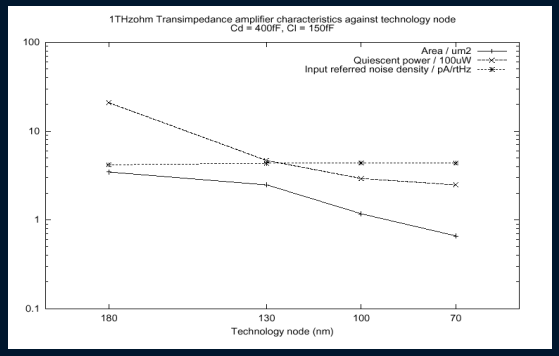
$g_{m3}+g_{mb3}+g_{d3} = 1/R_o - (g_{d1}+g_{d2})$

$F_i = I_1/(I_2+I_3)$



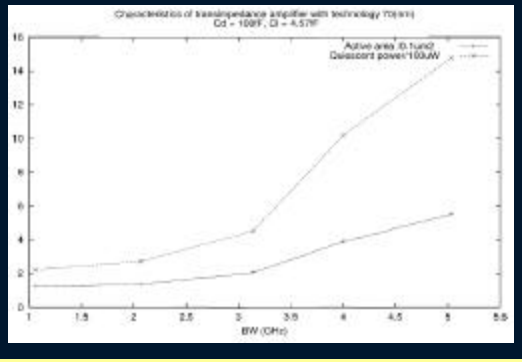
Predictive design space exploration

- sizing for process nodes 180-130-100-70nm : quantitative predictions for technological evolution
- use of BSIM3v3 transistor model parameters from UC Berkeley (Cao *et al.*, CICC 2000)
- more details at DATE (session 3D Tuesday 16:45)



power / 10
noise constant
area / 5

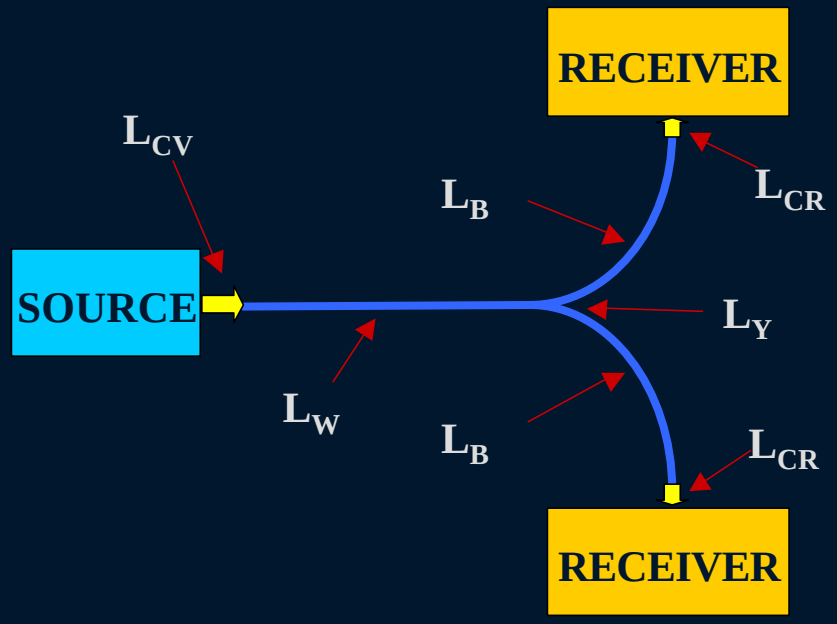
ITHzW TIA design with identical specifications for different technology nodes: validate traditional "shrink" predictions



TIA design @ 70nm node for various BW requirements (all other specifications remain identical)

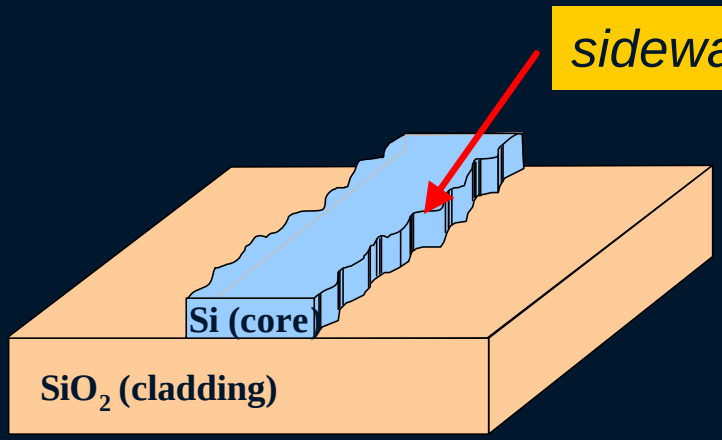
Losses in an optical link

- L_{TOTAL} (dB) = L_{CV}+ L_W+ L_Y+ L_B+ L_{CR}
  - L_{CV} Source-waveguide coupling coefficient
  - L_W Transmission Loss
  - L_Y Y-coupler Loss
  - L_B Bending Loss
  - L_{CR} Waveguide-detector coupling coefficient

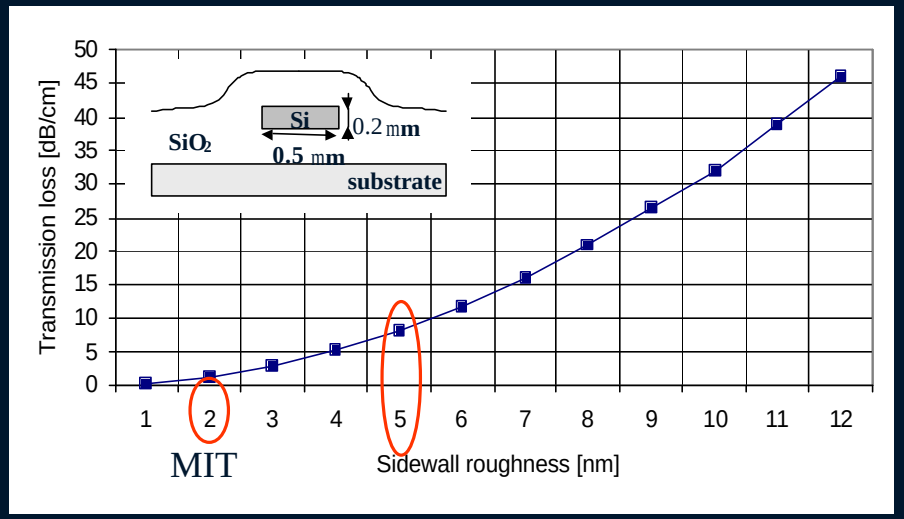


Transmission loss

- L_{TOTAL} (dB) = L_{CV}+ L_W+ L_Y+ L_B+ L_{CR}



$$L_W = \frac{\sigma^2}{\sqrt{2}\, k_0 d^4 n_1}\, g(V) f_e(x,\gamma)$$

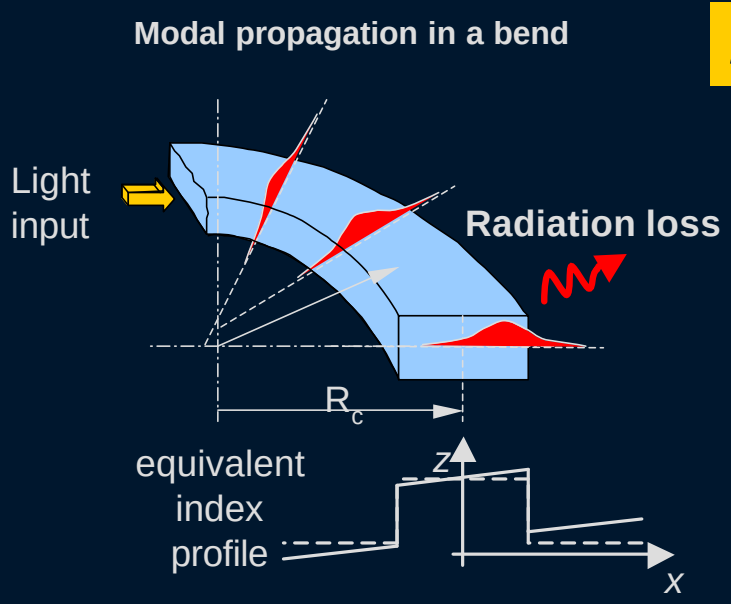


σ=2nm ⇒ 1.3dB/cm

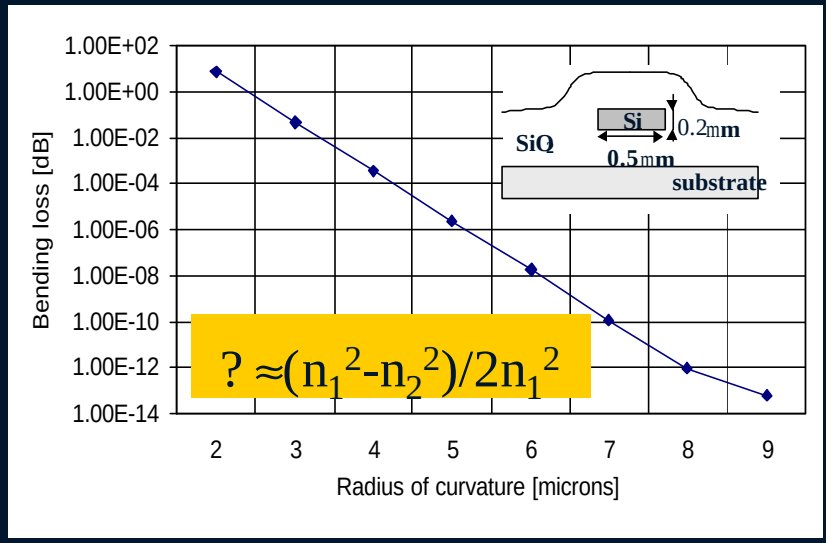
K. K. Lee et al., Optics Letters, 2001

Bending loss

- L_{TOTAL} (dB) = L_{CV}+ L_W+ L_Y+ L_B+ L_{CR}



bends

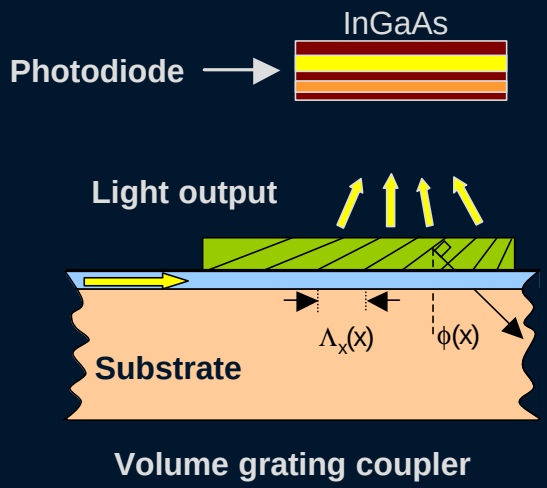


For R > 2µm, L_B = 0

Other losses

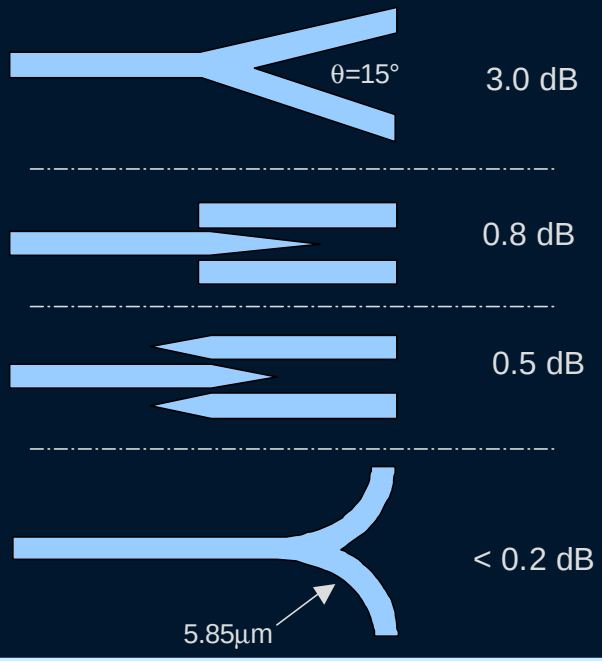
- L_{TOTAL} (dB) = L_{CV}+ L_W+ L_Y+ L_B+ L_{CR}
- L_{CV} Input coupling coefficient (50%=3dB)
- L_Y Y-splitter loss (0.2dB)
- L_{CR} Output coupling coefficient (87%=0.6dB)

Output loss:



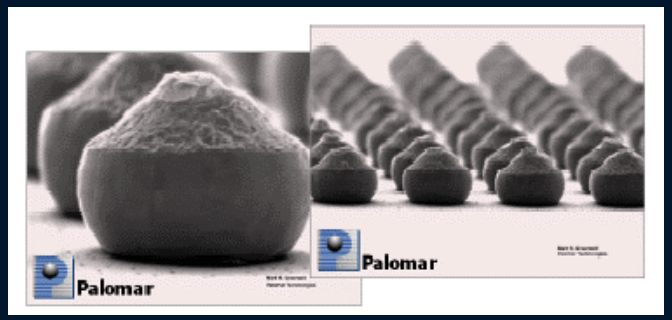
Volume grating coupler

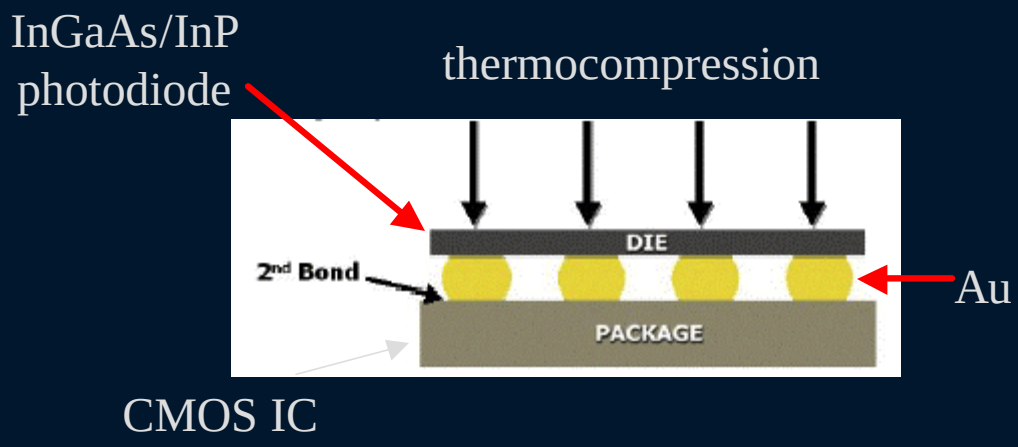
Y-splitter loss



Bonding issues

- flip-chip is today the most effective and proven technique
  - alignment down to 1um accuracy
  - solder bumps under 10um diameter





- in the future:
  - molecular bonding
  - direct wafer bonding
  - ...

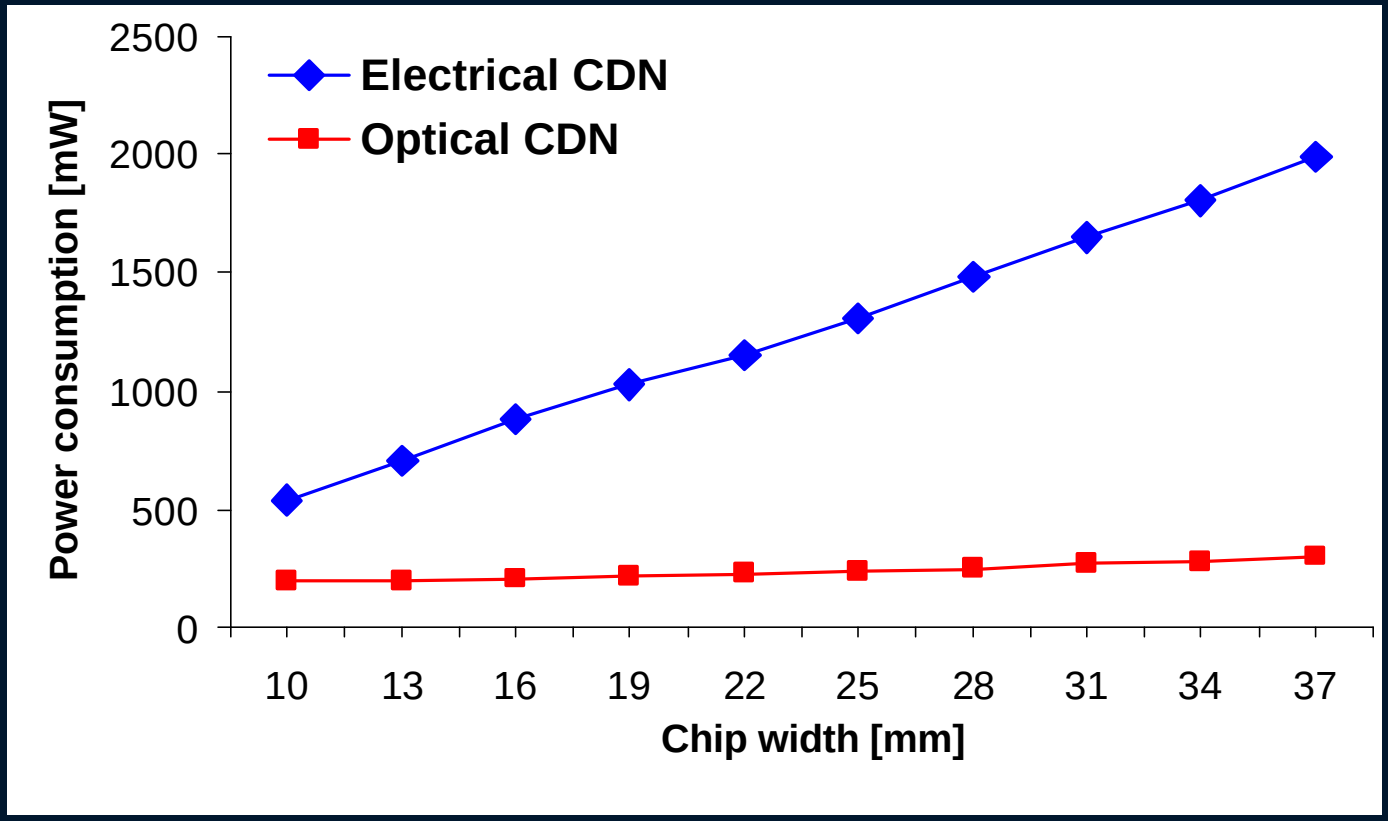
Investigation conditions and program

Electrical CDN		Optical CDN	
Technology parameters		ITRS roadmap	
Transistors		BSIM3v3 and BSIM4 model parameters [Berkeley Univ.]	
Metallic wires	ITRS roadmap	Optical devices	Existing technology
		InGaAs Photodiode	G8376-02 Hamamatsu Corp.
		(InGaAl)As/InP VCSEL	Amann TU Munchen

- comparison of optical and electrical clock distribution networks:
  - power vs. chip size
  - power vs. operating frequency
  - power vs. number of distribution points
  - power vs. technology node
  - power vs. sidewall roughness

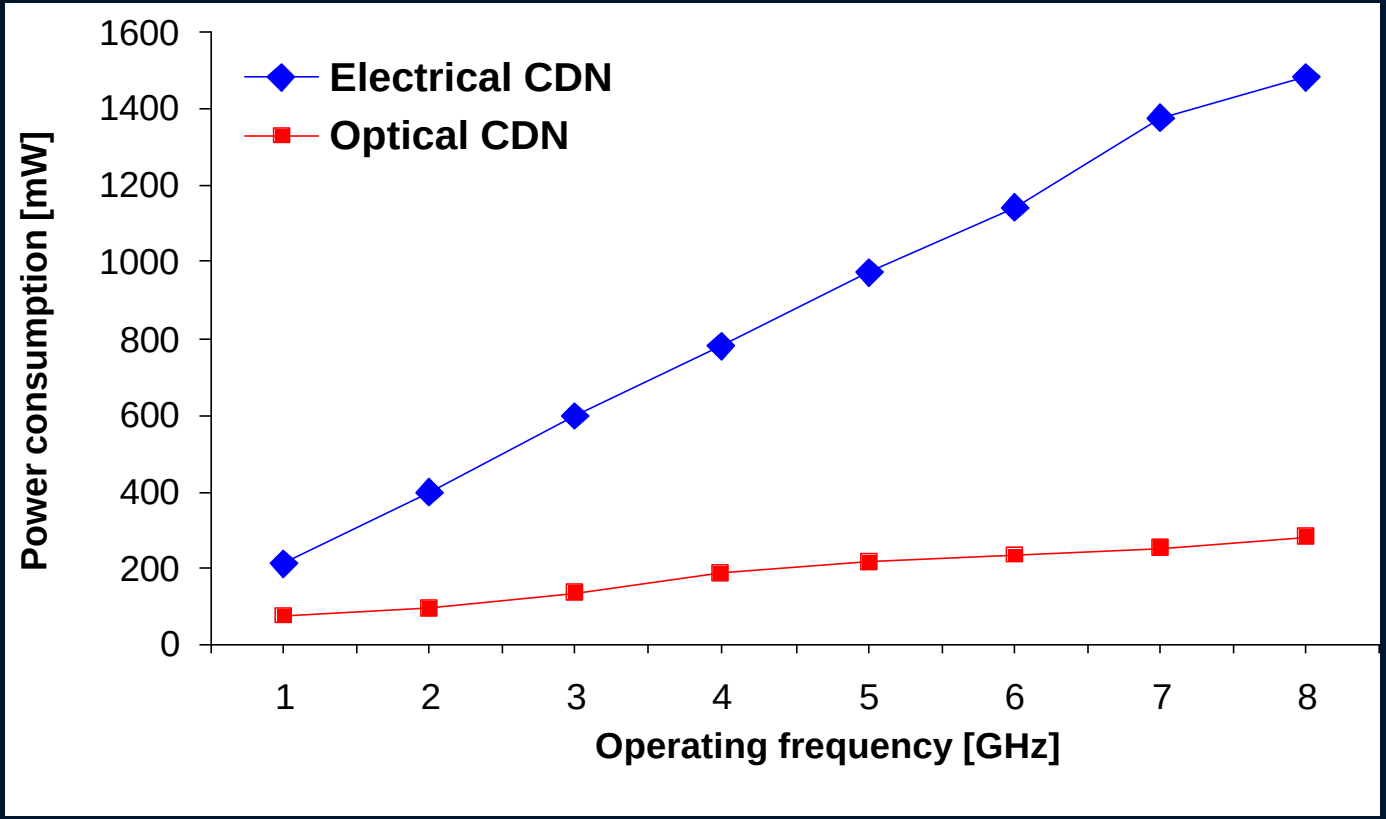
Electrical-optical comparison

- comparing optical clock distribution power dissipation for varying chip size
- @70nm node, 5.6GHz, 256 drop points



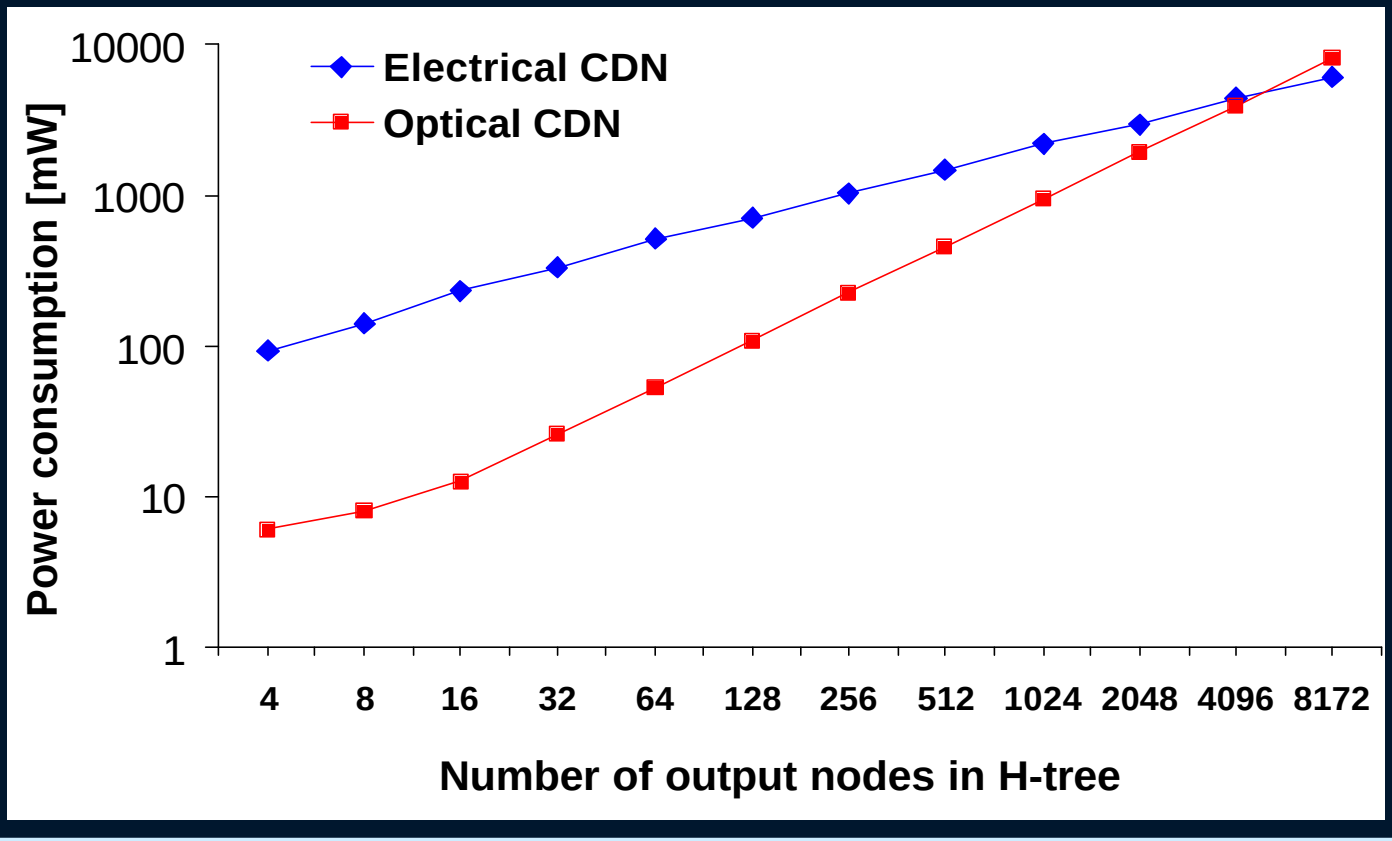
Electrical-optical comparison

- comparing optical clock distribution power dissipation for varying operating frequency
- @70nm node, 20mm chip width, 256 drop points



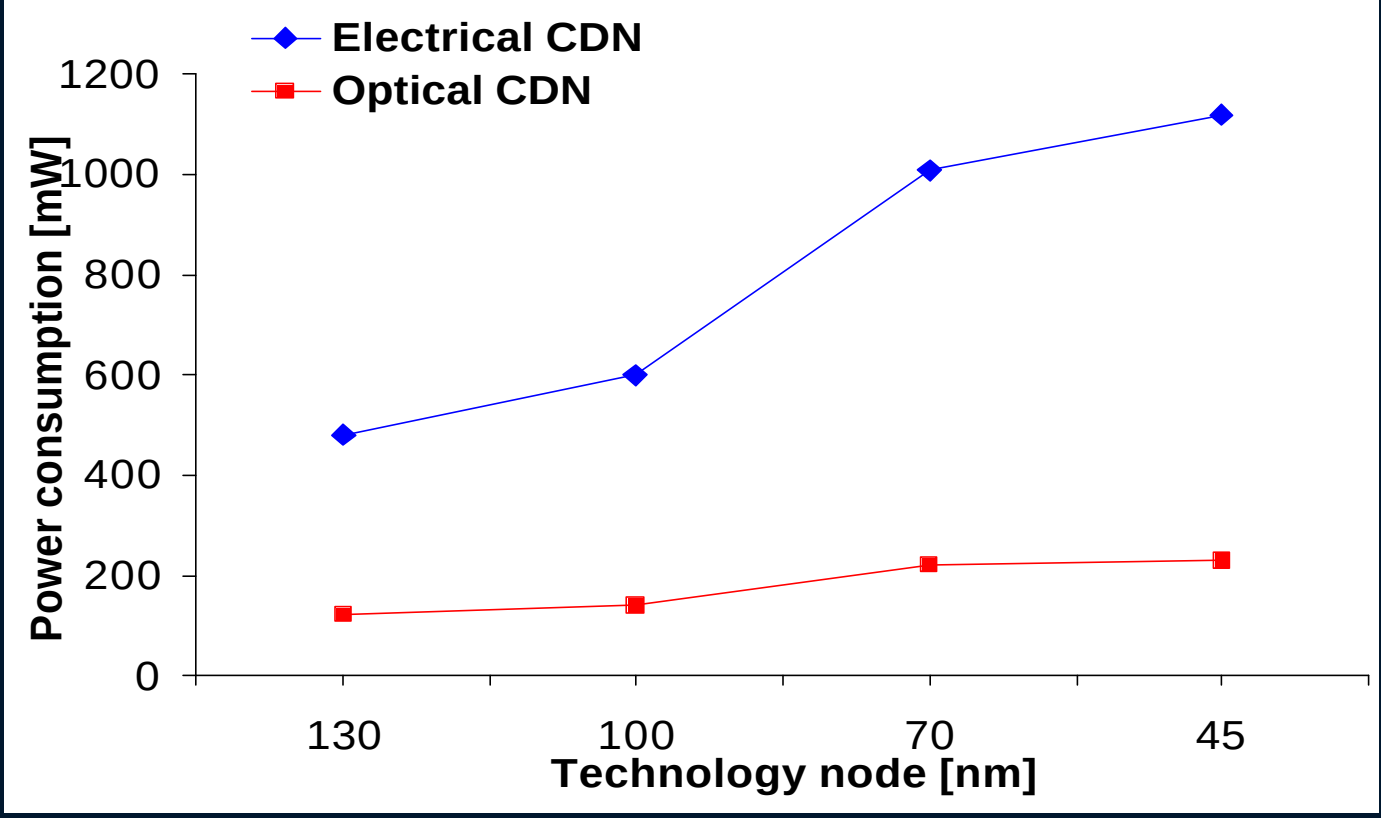
Electrical-optical comparison

- comparing optical clock distribution power dissipation for varying number of drop points
- @70nm node, 5.6GHz, 20mm chip width



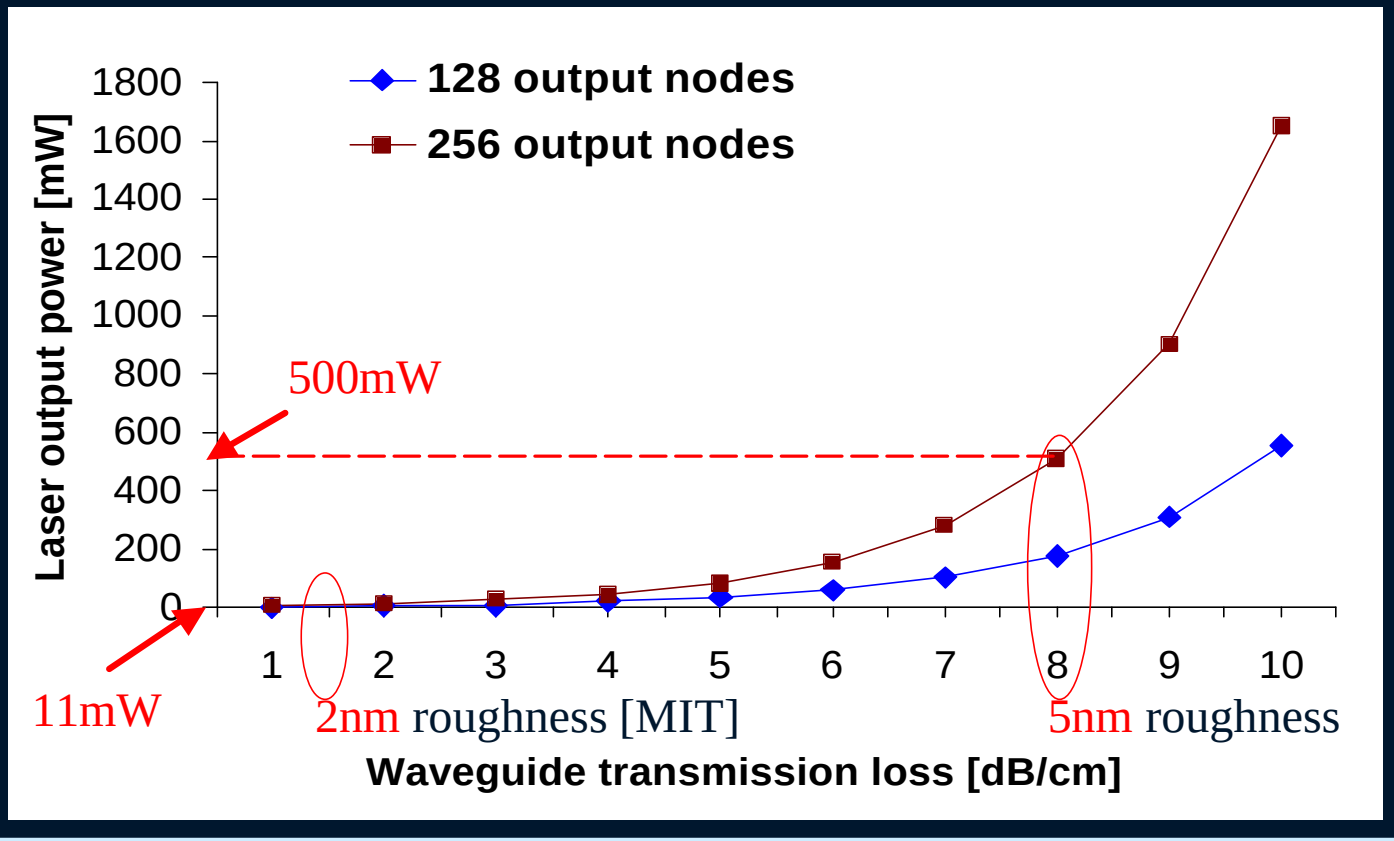
Electrical-optical comparison

- comparing optical clock distribution power dissipation for varying technology node
- 20mm chip width, 256 drop points



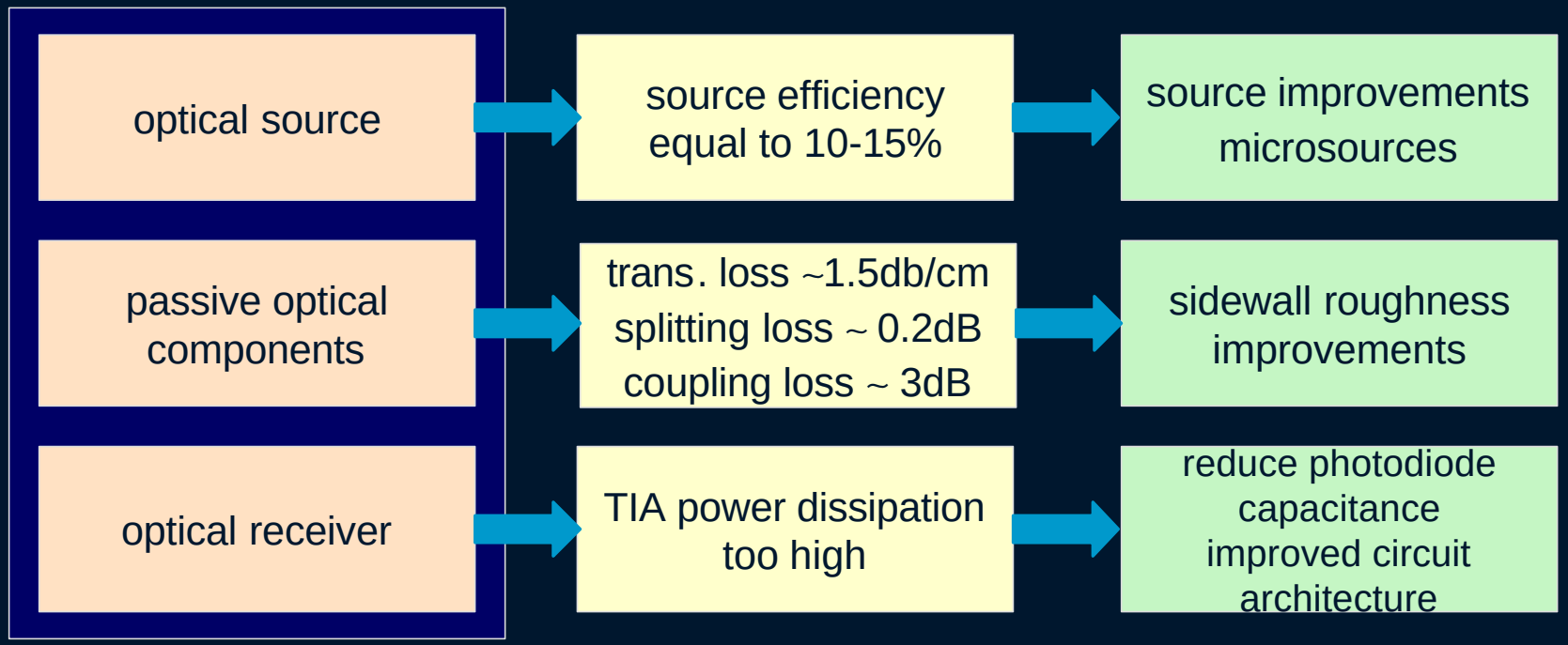
Electrical-optical comparison

- comparing optical clock distribution power dissipation for varying sidewall roughness
- @70nm node, 5.6GHz, 20mm chip width, BER=10^{-15}



Clock distribution conclusions

- optical clock distribution gives a five-fold improvement in power dissipation at 5GHz
- this factor will increase as optical technology improves and operating frequencies rise
- where is work needed?



- more details at DATE Wednesday session 5G 12:00

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  - ITRS
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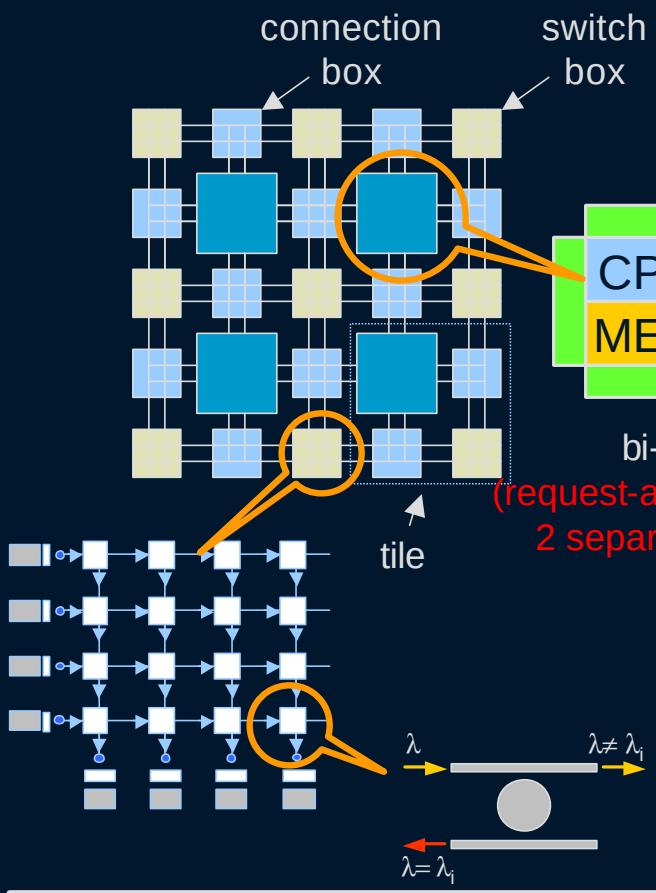
  - Structure and global design methodology
  - Interface circuit characteristics
  - Calculating losses in passive devices
  - Electrical-optical comparison
- Wavelength-reconfigurable networks on chip
  - Target functionality
  - Modelling and design environment
  - Architecture of reconfigurable network

Reconfigurable optical NoCs (N-N)



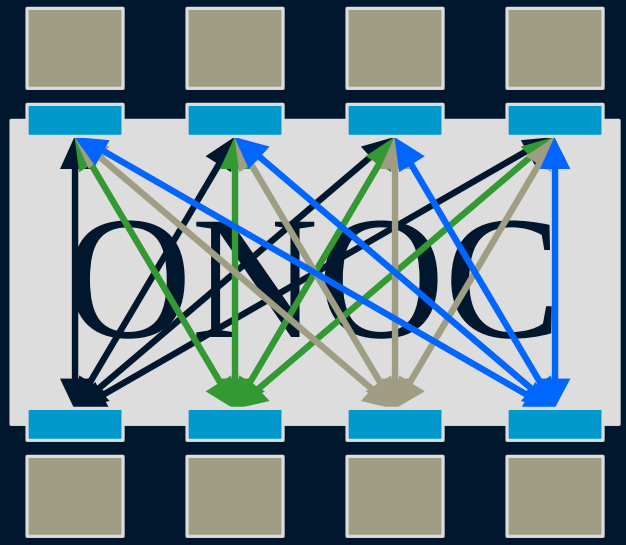
bi-directionality
(request-acknowledge)
2 separate networks

message
address
data (32 bits)
validation

data rate
3Gbits/s

SoC architectures
- distributed heterogeneous resources

Targets:1 to 32
locally synchronous



Masters: 1 to 32
locally synchronous

no contention
➔buffers in wrappers

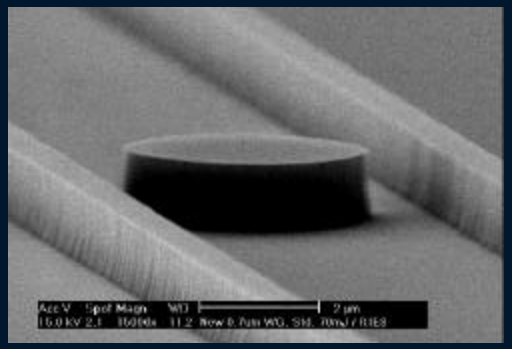
wrappers:
serialisation
conversion
decode address
synchronisation

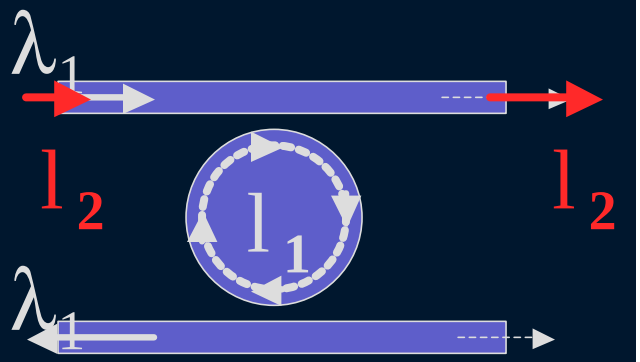
MMP architectures
- distributed memory, and/or
- memory accessible through CPU

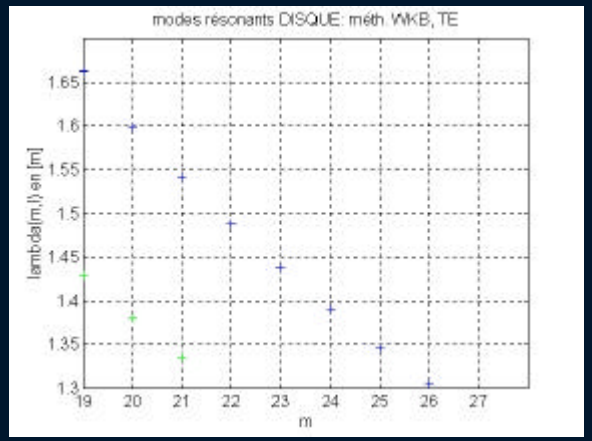
Comparison with SPIN (LIP6)

Microring resonator

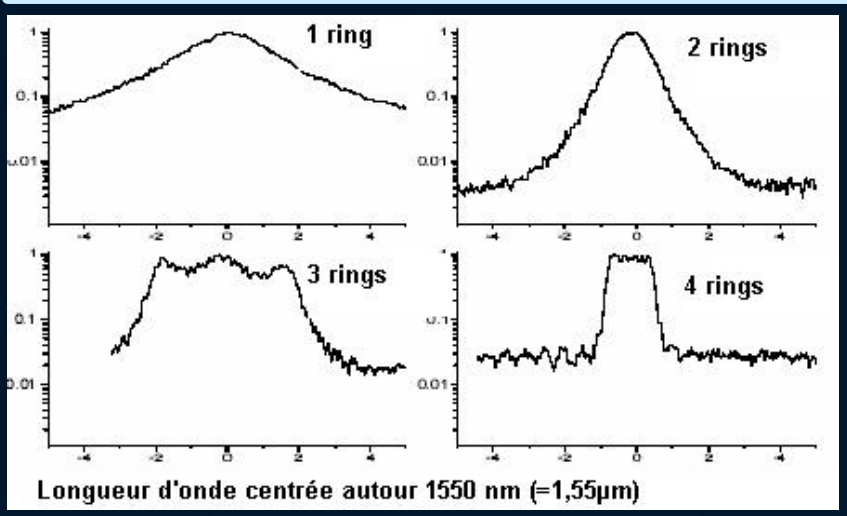
- depending on the disc material parameters and dimensions, several resonant wavelengths exist
- lightwave will couple into the disc (and then out via the other waveguide) if its wavelength is equal to one of the microring's resonant wavelengths
- otherwise there is no coupling and the lightwave propagates normally
- selectivity critical factor in number of channels
- estimation of sensitivity of λ_k to mismatch ...

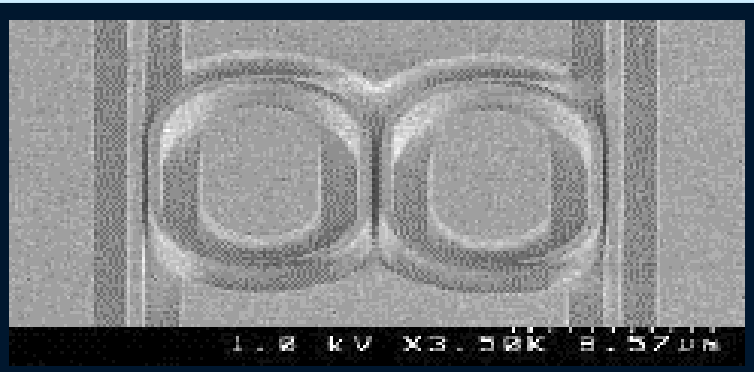






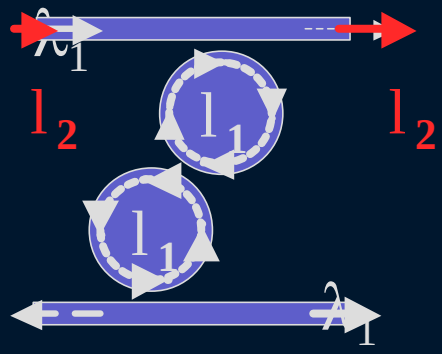
Microring selectivity and FSR

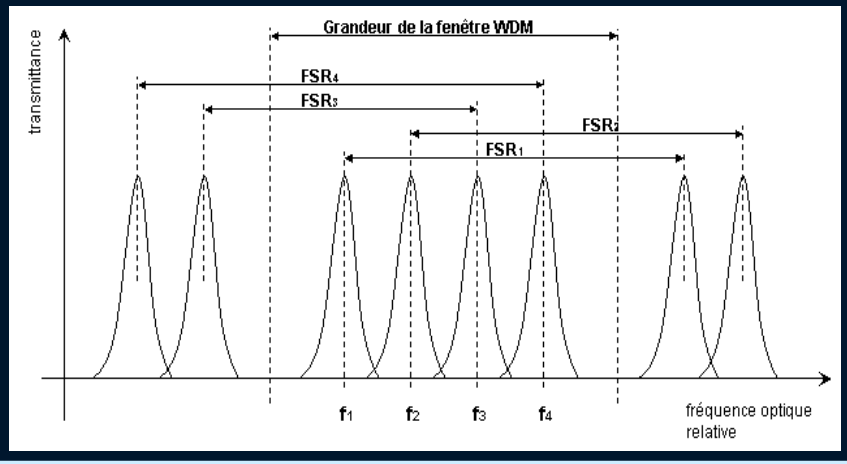


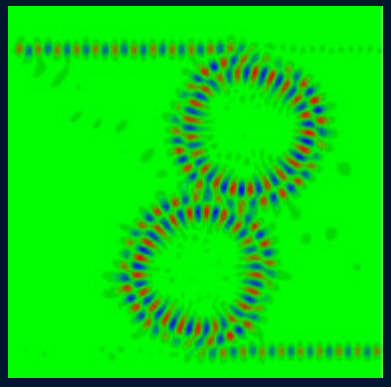


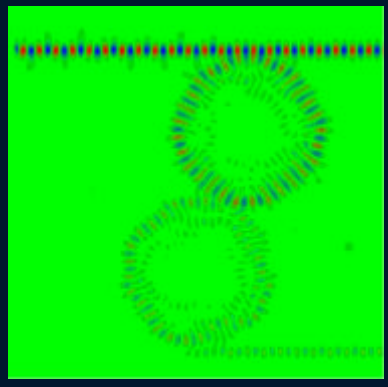
$$P(w) = \left(\frac{4/t_0^2}{4/t_0^2 + (w - w_0)^2} \right)^N$$

$$\begin{cases} \frac{\partial \vec{H}}{\partial t} = -\frac{1}{m} \nabla \times \vec{E} \\ \frac{\partial \vec{E}}{\partial t} = \frac{1}{e} \nabla \times \vec{H} \\ \nabla \cdot \vec{D} = 0 \\ \nabla \cdot \vec{B} = 0 \end{cases}$$



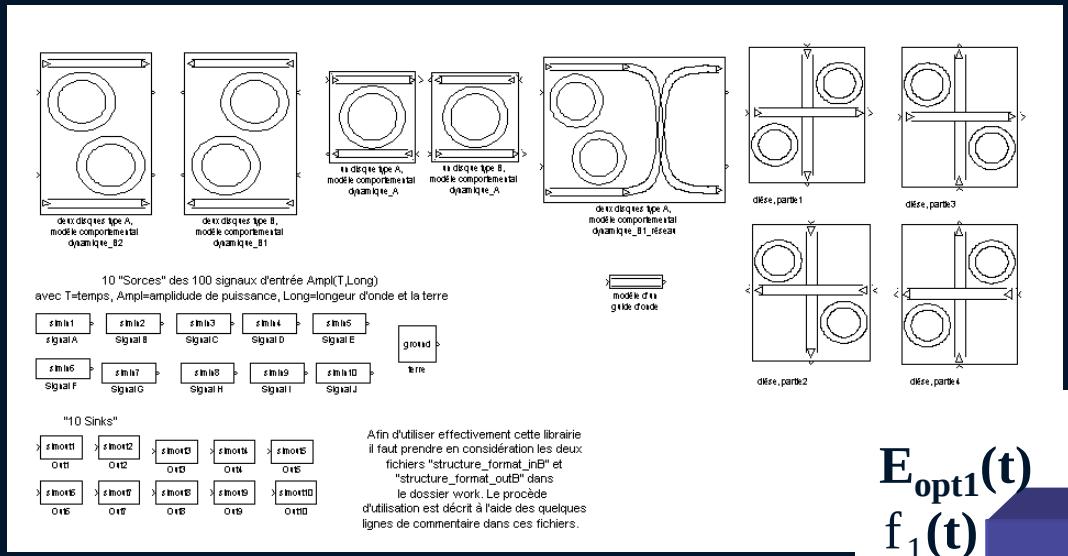


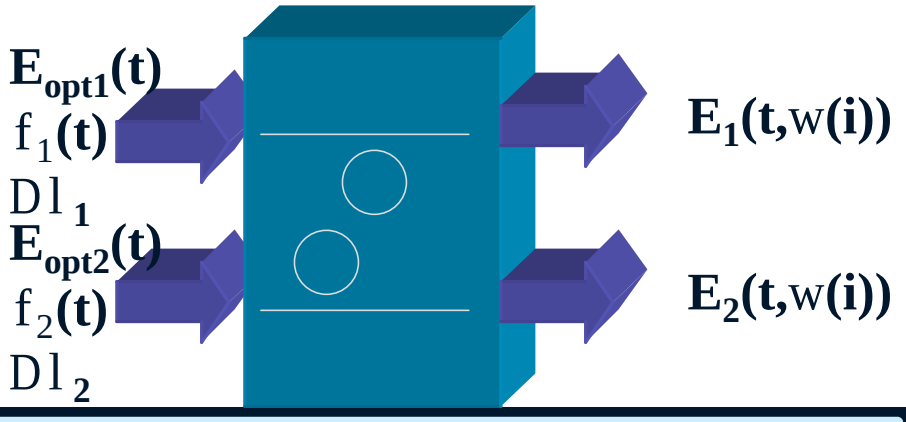




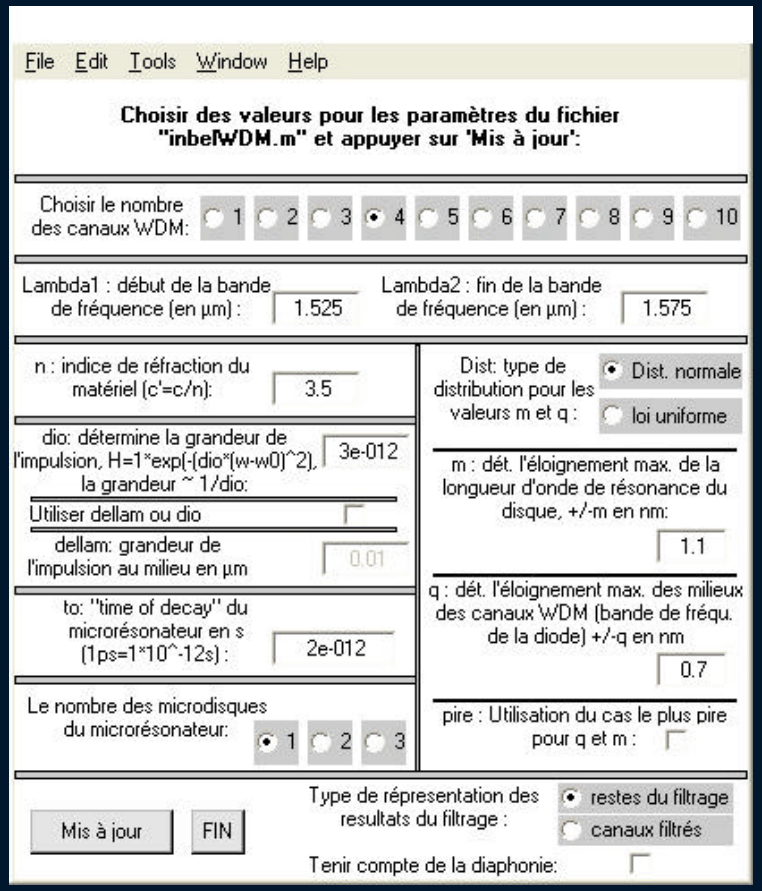
Models for system design

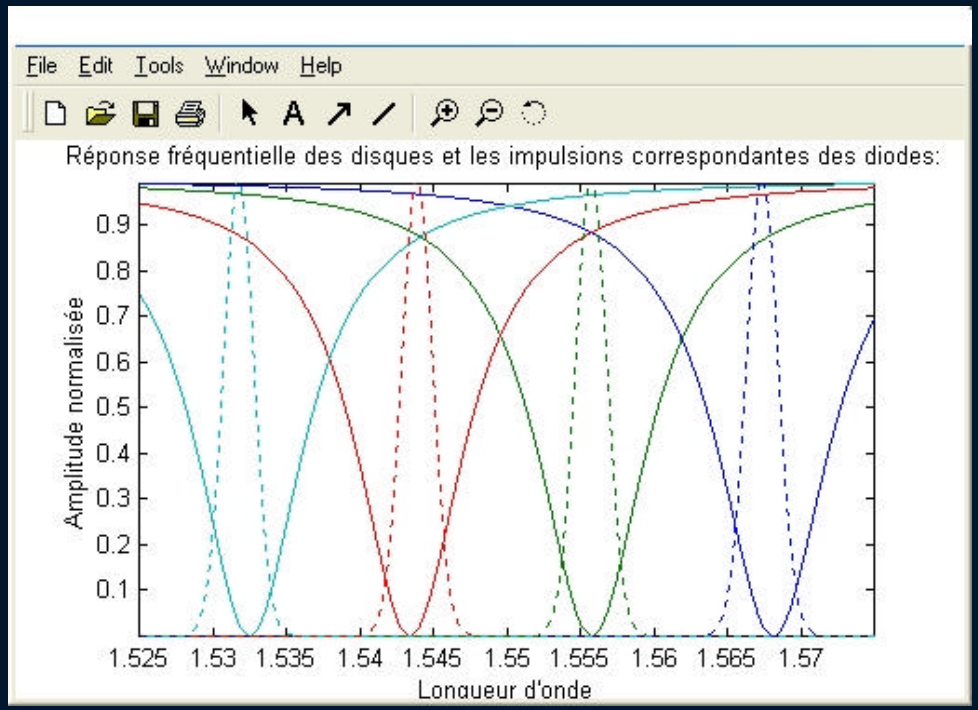
- library of building blocks (Matlab and VHDL-AMS)
  - equation capture for all elements
  - parameter extraction for model simulation
  - simulation results: power, attenuation, data rate ...



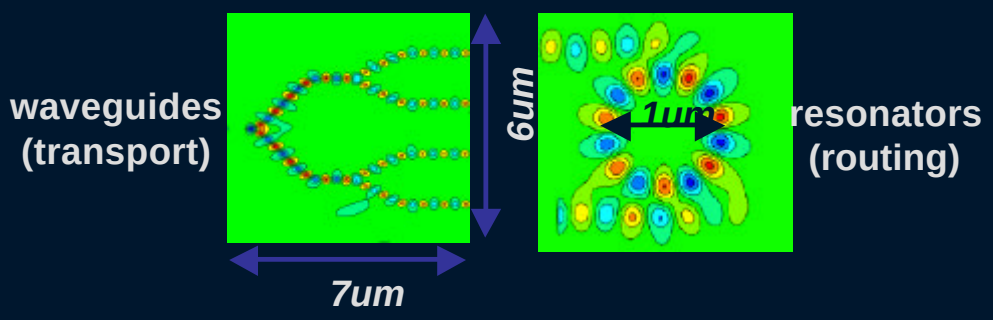


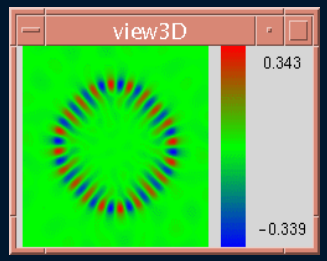
Design environment

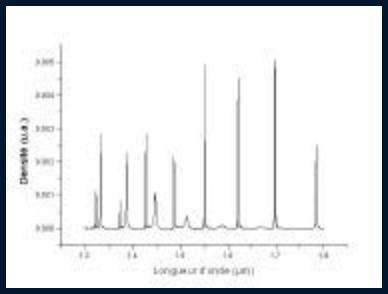




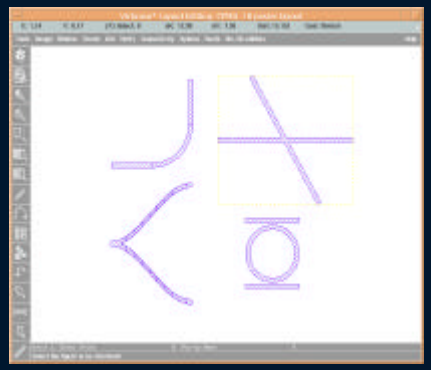
Photonic device simulation tools

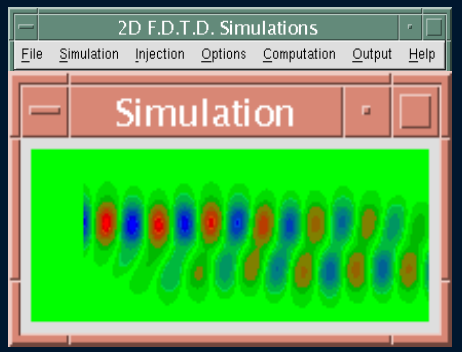




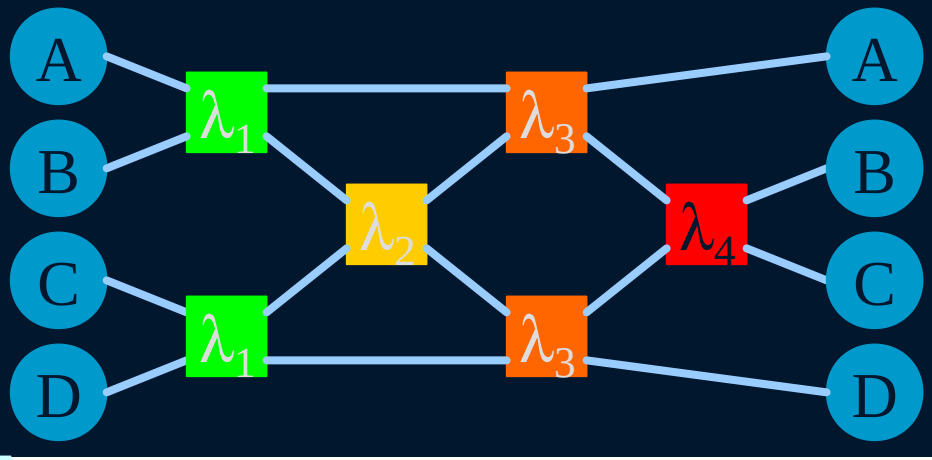


- 2D-3D FDTD (finite difference time domain) method
- simulation engine integrated into standard EDA environment (Cadence)
- parallel execution and memory bus usage optimization

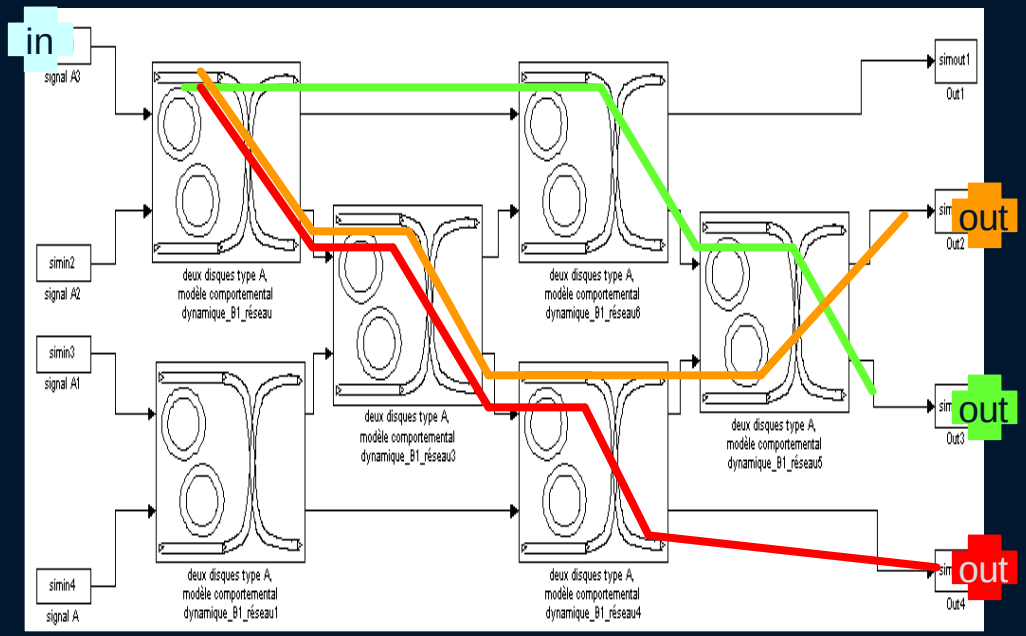




Modelling and simulation of an optical crossbar

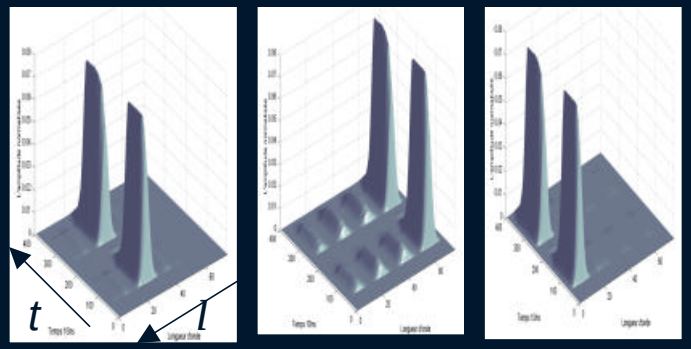


emitter \ receiver	A	B	C	D
A	λ_2	λ_3	λ_1	λ_4
B	λ_3	λ_4	λ_2	λ_1
C	λ_1	λ_2	λ_4	λ_3
D	λ_4	λ_1	λ_3	λ_2

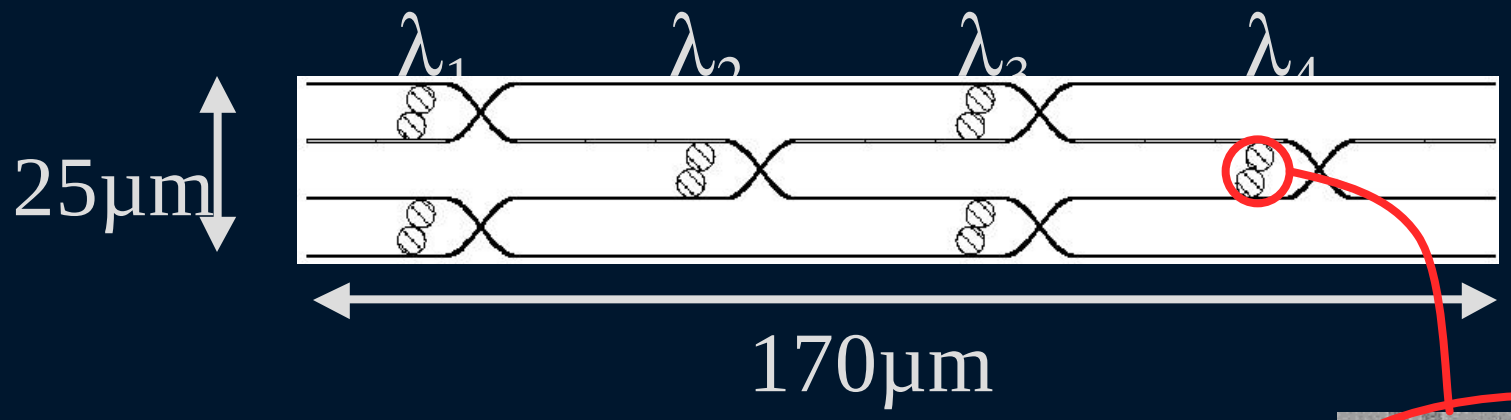


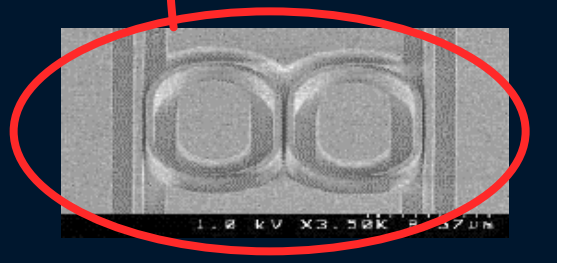
Injection in port #1

Port #2 *Port #3* *Port #4*



4x4 optical cross-bar

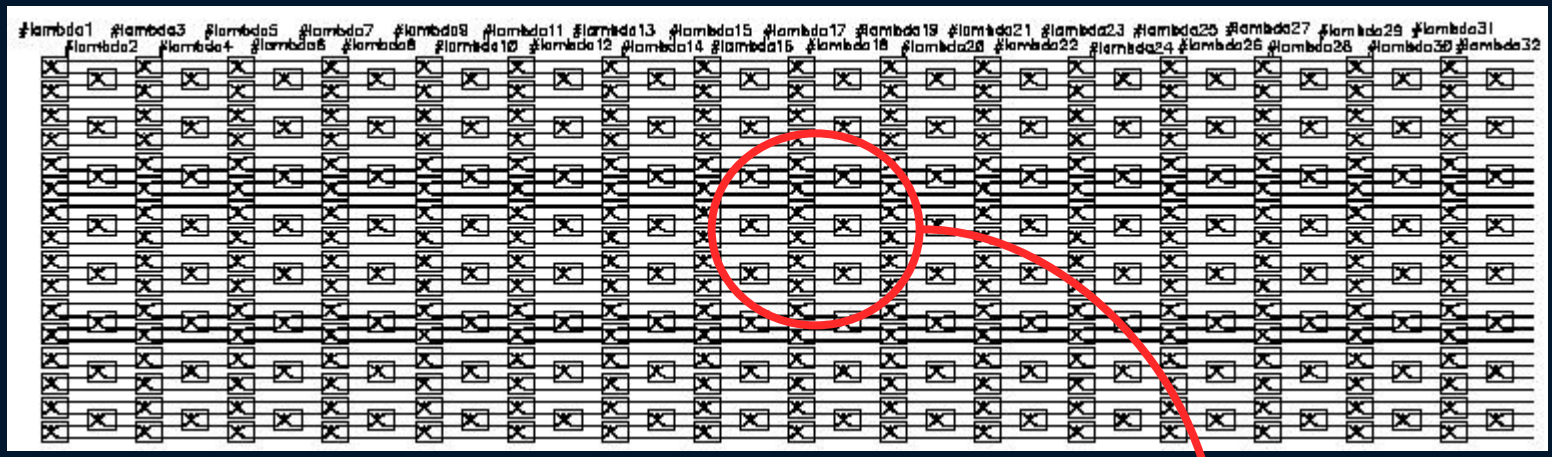




Total area for passive network: 0.00425 mm²

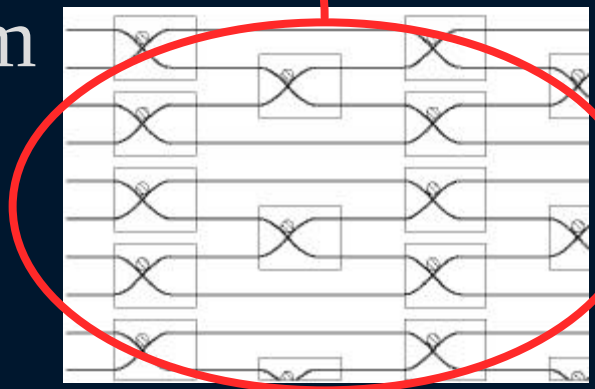
↳ + Connections to SoC IP blocks

32x32 optical cross-bar



200µm

730µm



Total area for passive network: 0.146 mm²

Conclusion

- optical links are moving into the chip
- first quantitative comparisons show an advantage for optical clock distribution over electrical schemes
- but is it enough?
- do we really need global clock distribution?
- optical network on chip promising:
  - scalable passive structure developed, test under way
  - low real estate, high throughput, should be full-duplex
- high-level models necessary for design (SystemC)
- watch this space for quantitative comparison
- more details at DATE:
  - Wednesday session 4E 10:30 and session IP3 11:00
  - Friday W2 Parallel optical interconnects inside electronic systems