Prediction of Interconnect Adjacency Distribution: Derivation, Validation, and Applications

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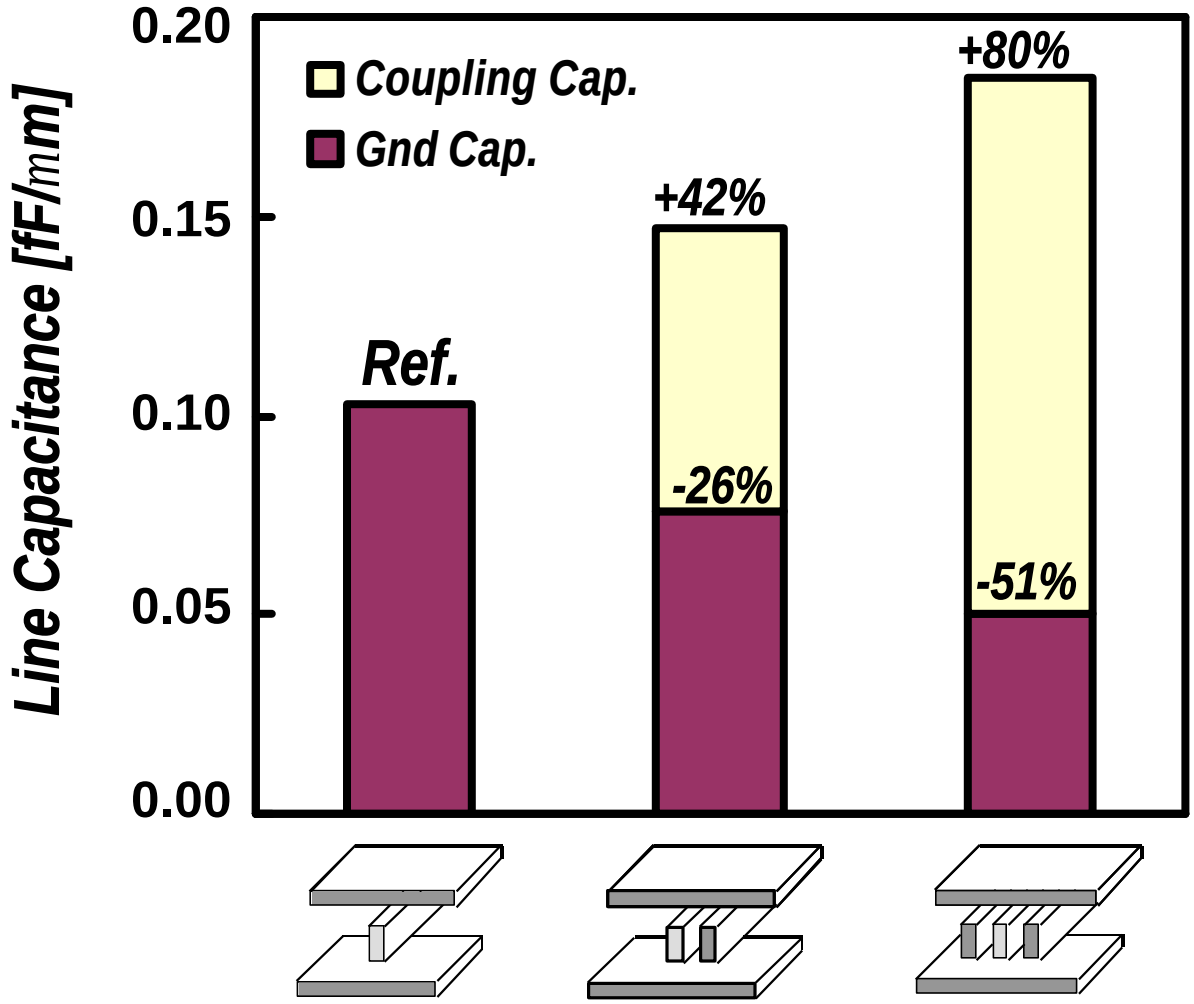
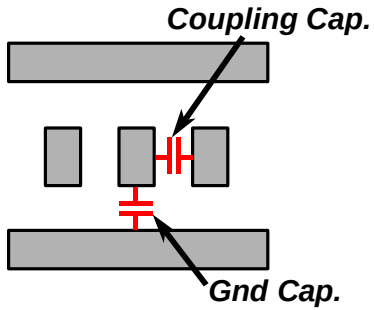
Outline

- **Motivation**
- **Interconnect Adjacency Model**
  - **Derivation**
  - **Validation**
  - **Applications**
- **Conclusion**

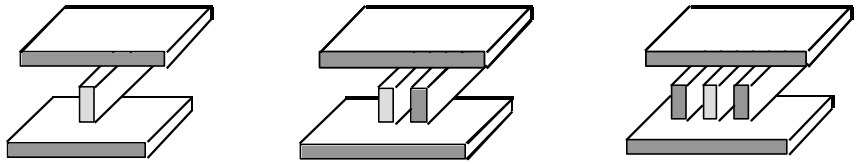
Effect of Geometry on Capacitance





Motivation

- **How to choose the geometry for system level modeling of interconnect capacitance:**



- **A real system is a mix of many cases.**
- **A statistical approach is required to predict the capacitance distribution more realistically.**
- **We will derive the interconnect geometry distribution that produces circuit variations.**

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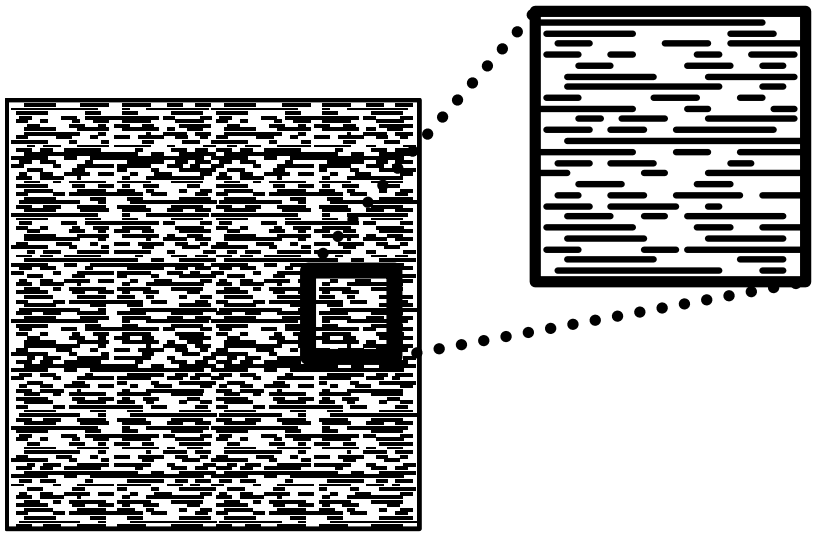
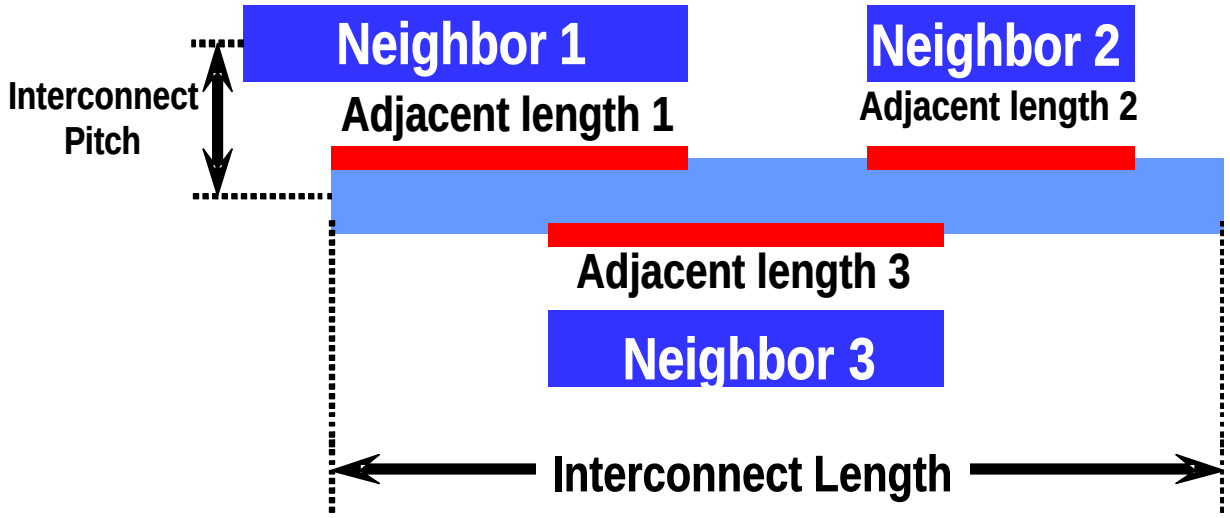
Assumptions

- **Wire placement in a random logic network is complex and irregular enough to be modeled by a probability distribution involving “coin flipping”.**
- **Average channel utilization, *p*, is known.**

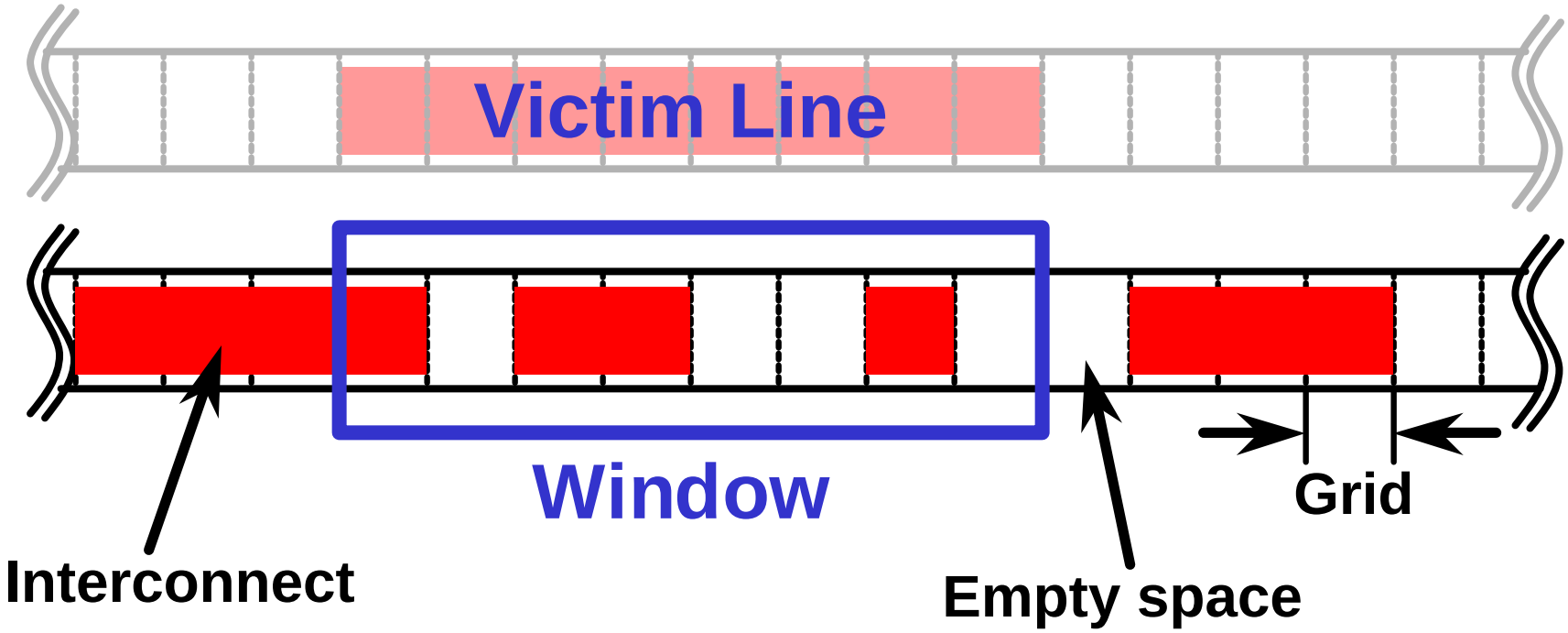


What is Adjacency?

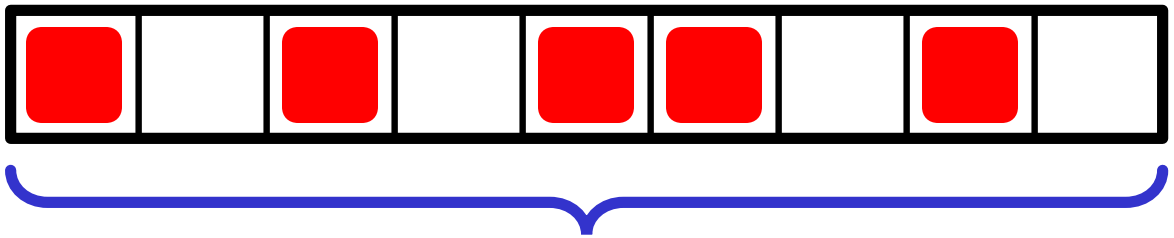
Interconnect adjacency **is the fractional length of an interconnect that possesses neighbors at *minimum spacing*.**



Definitions



Simple Case: Unit Length System



Window of size n=9

$$f(k) = \binom{n}{k} p^k (1-p)^{n-k}$$

Bernoulli Distribution

n = total number of grids
k = number of filled grids
p = probability of filling

Realistic System

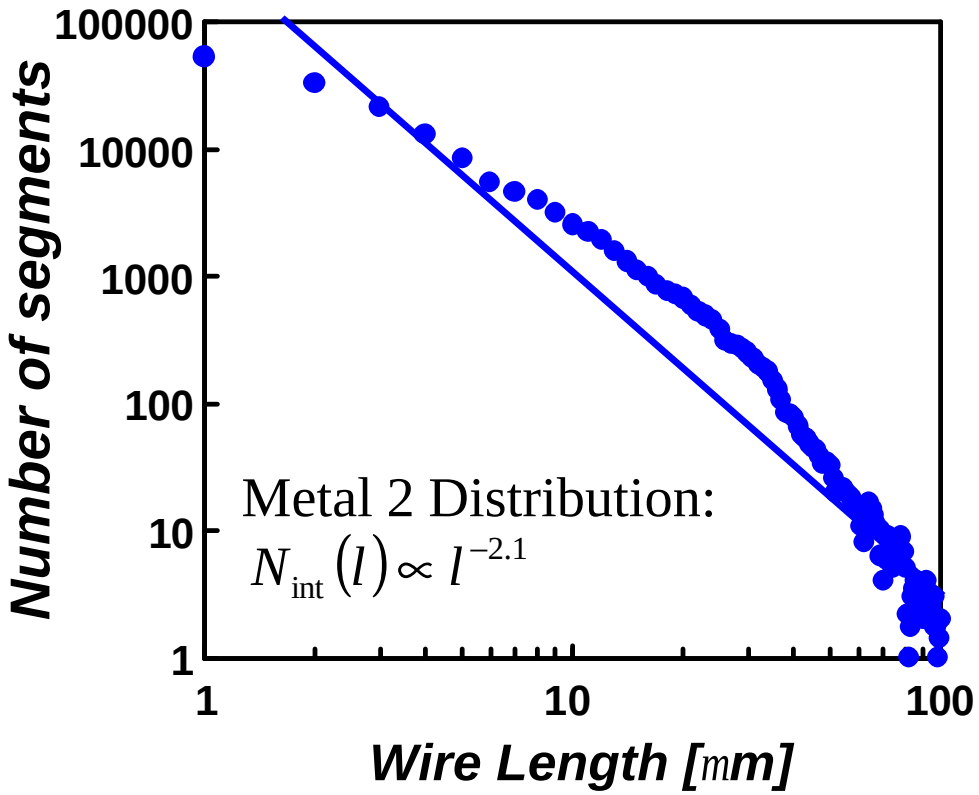
- **Wires are random length (not all unit length).**
- **Window size, *n*, is not constant anymore.**
- **Wires may cross window boundaries.**

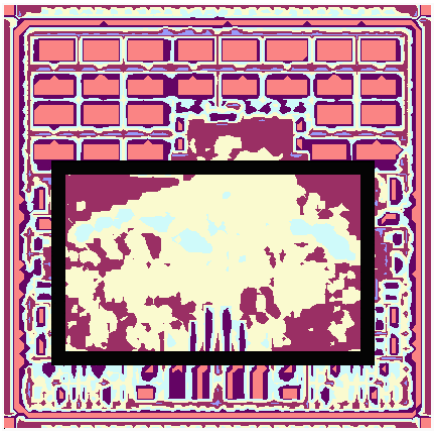
Derivation details available in the paper.

Model Input

- **Average channel utilization, *p*.**
- **Minimum and maximum segment length.**
- **Grid size.**
- **Segment length distribution.**
  - **Can be derived from Rent's rule by partitioning.**
  - **Can be fit empirically.**

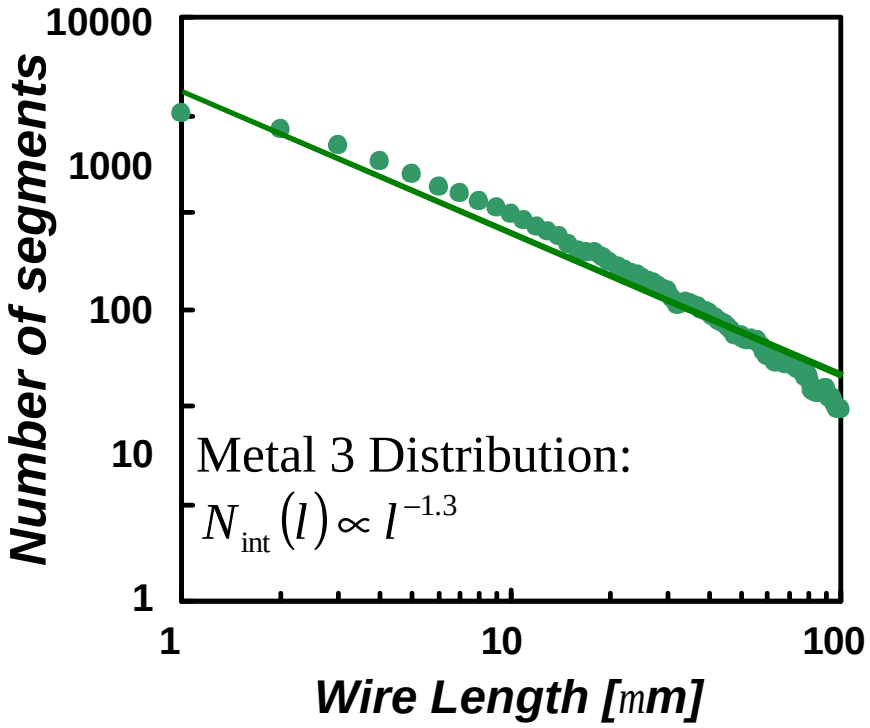
M2 Segment Length Distribution

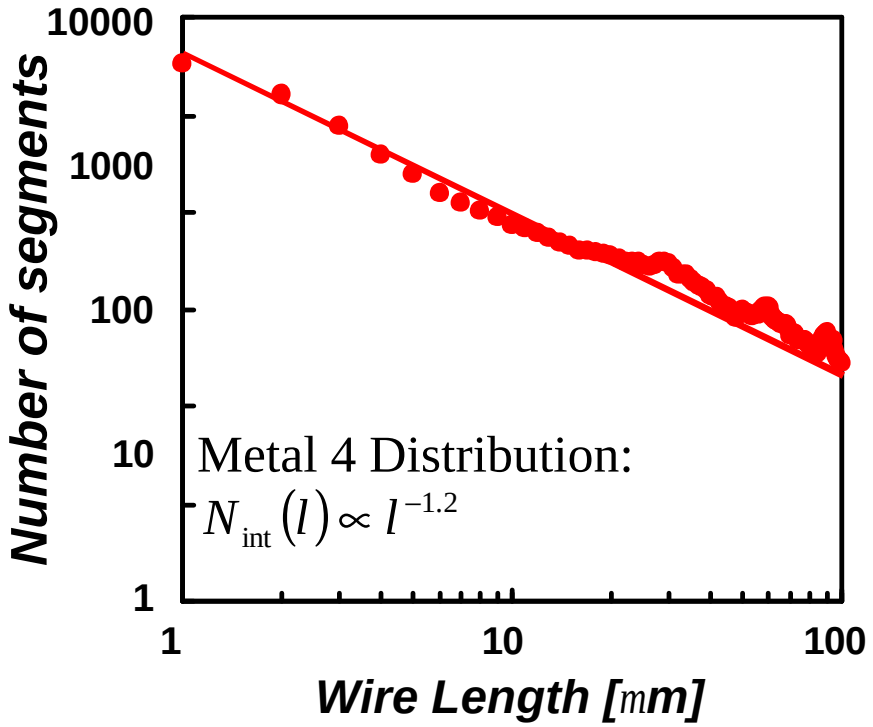




Technology = 130nm
Metal layer = M2
Min wire length = 1.0 mm
Max wire length = 100 mm

Other Segment Length Distribution





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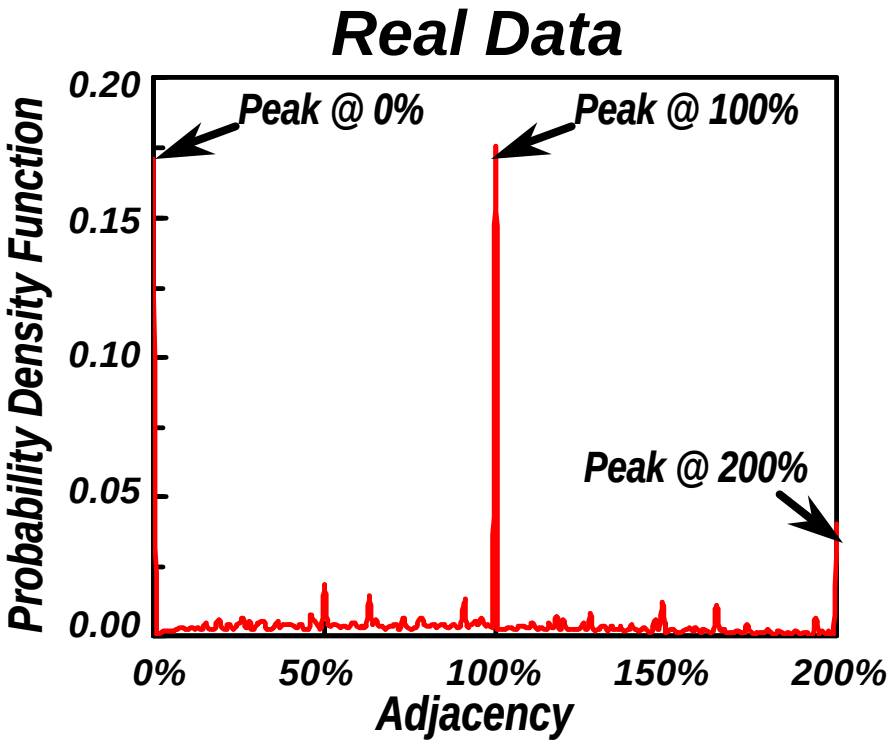
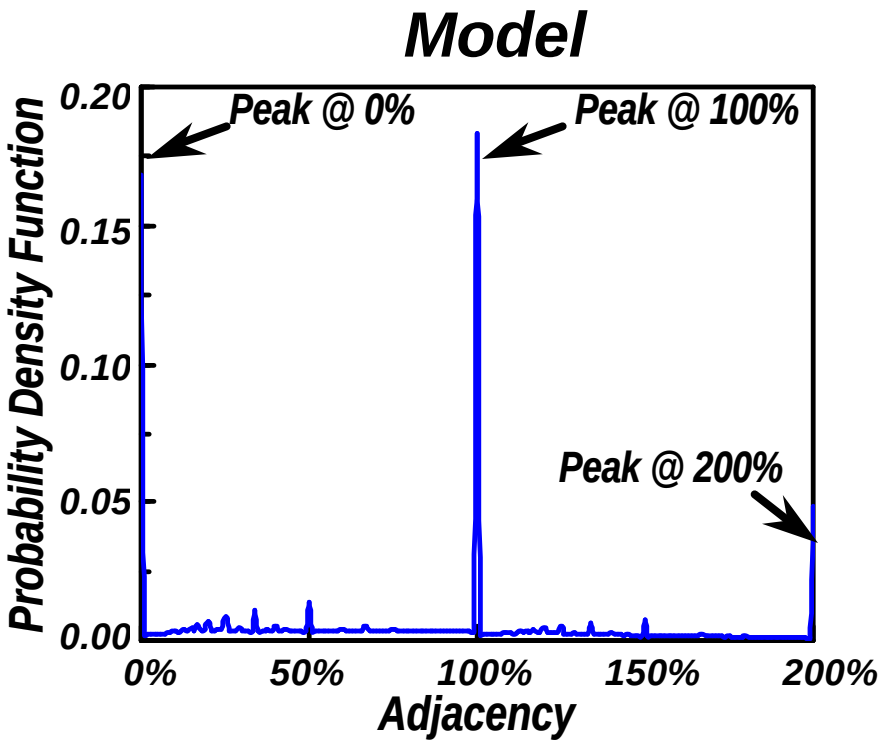
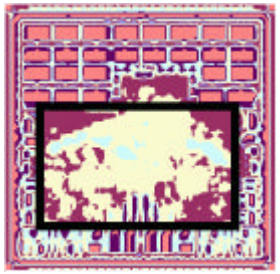
Comparison with Actual Data PDF



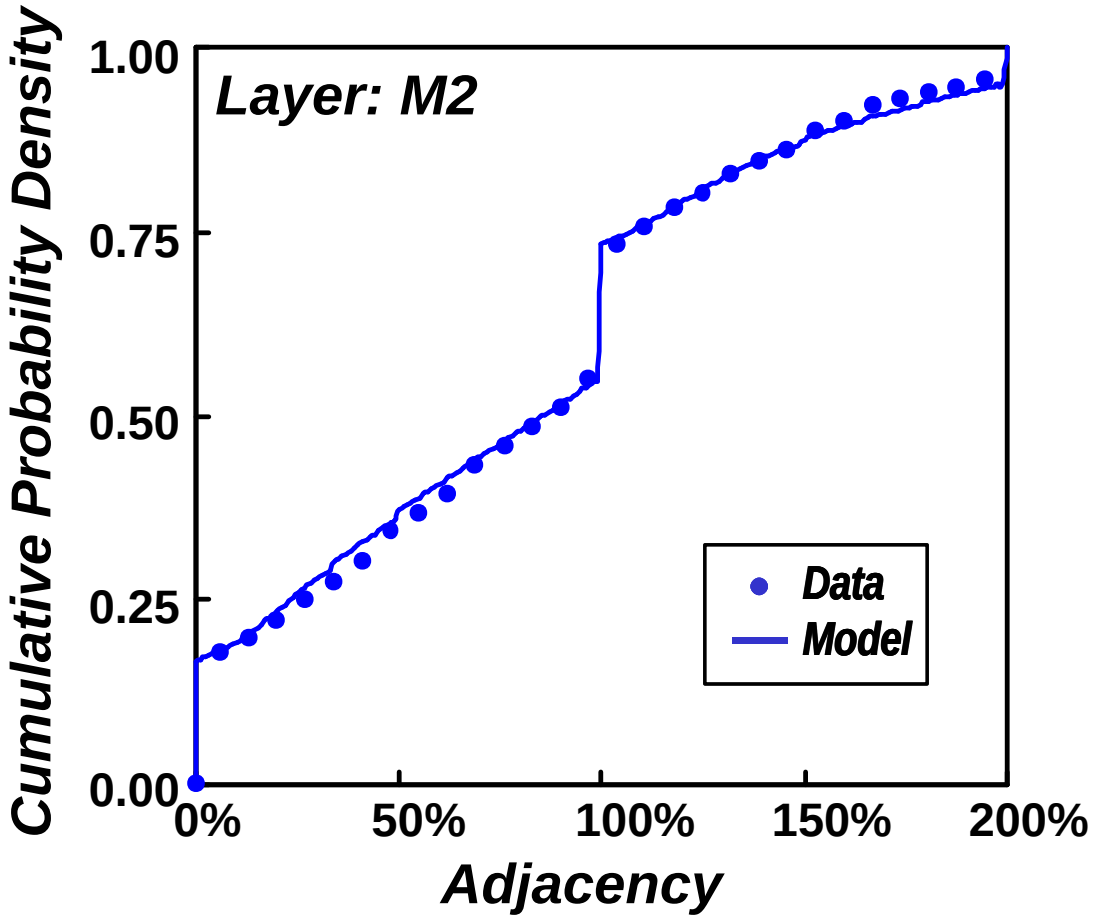




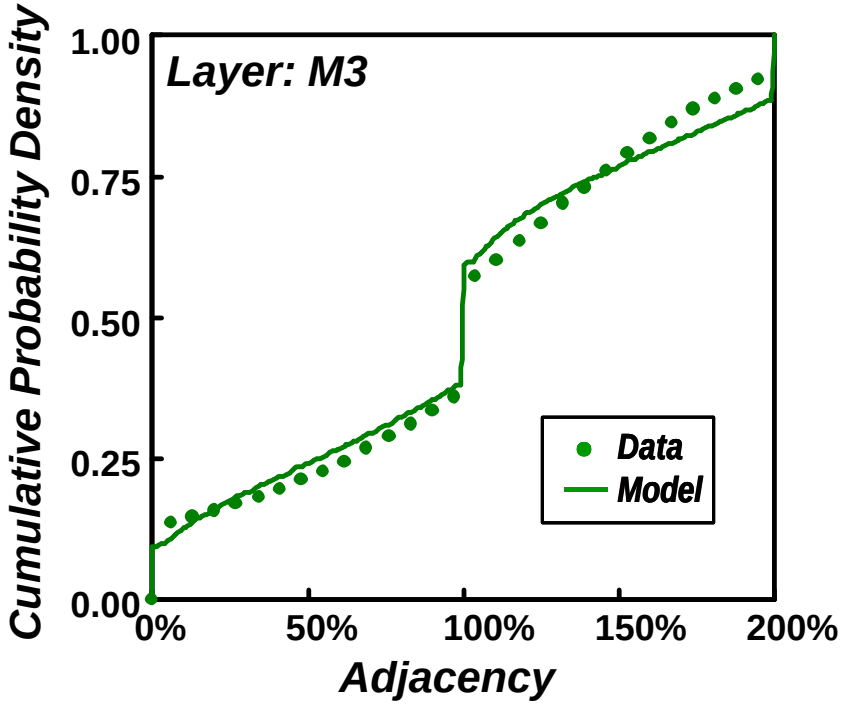
Metal layer = M2
Technology = 130 nm

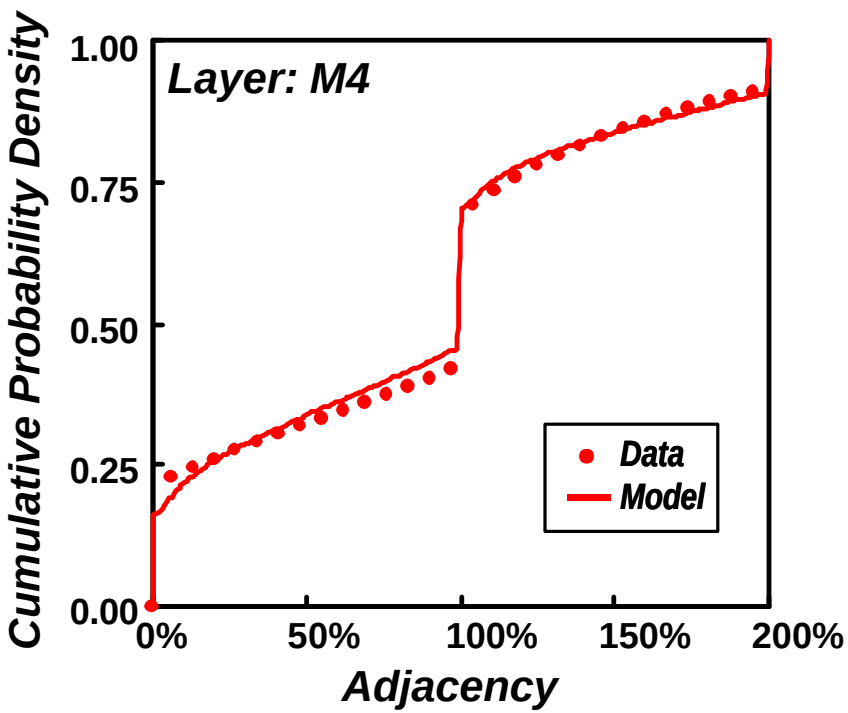
Channel utilization = 40%
Min wire length = 1.0 mm
Max wire length = 100 mm
Grid size = 0.01 mm

Comparison with Actual Data CDF



Comparison with Actual Data CDF



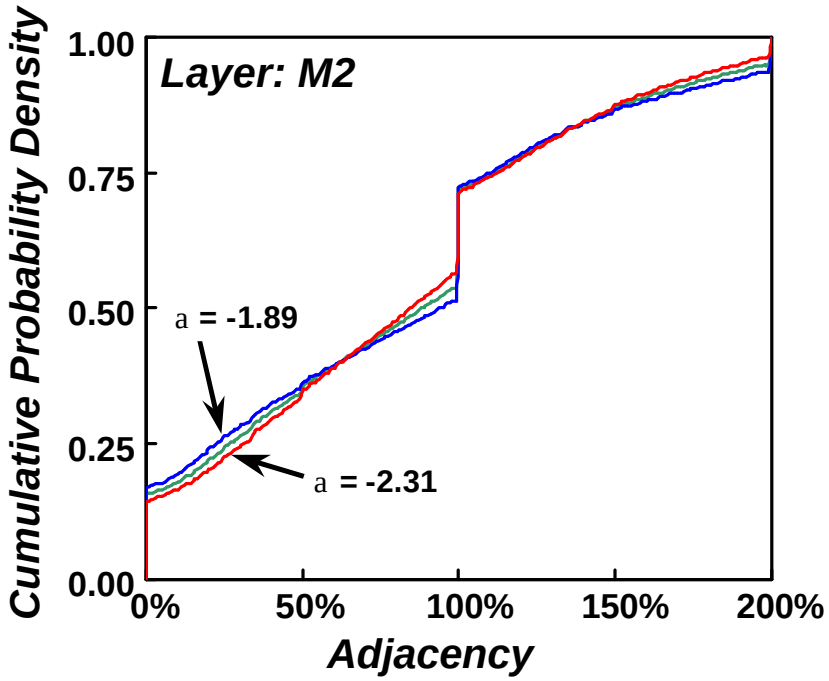


Metal layer = M3
Channel utilization = 50%
Gate pitch = 1.0 μm
Max wire length = 150 μm
Grid size = 0.01 μm

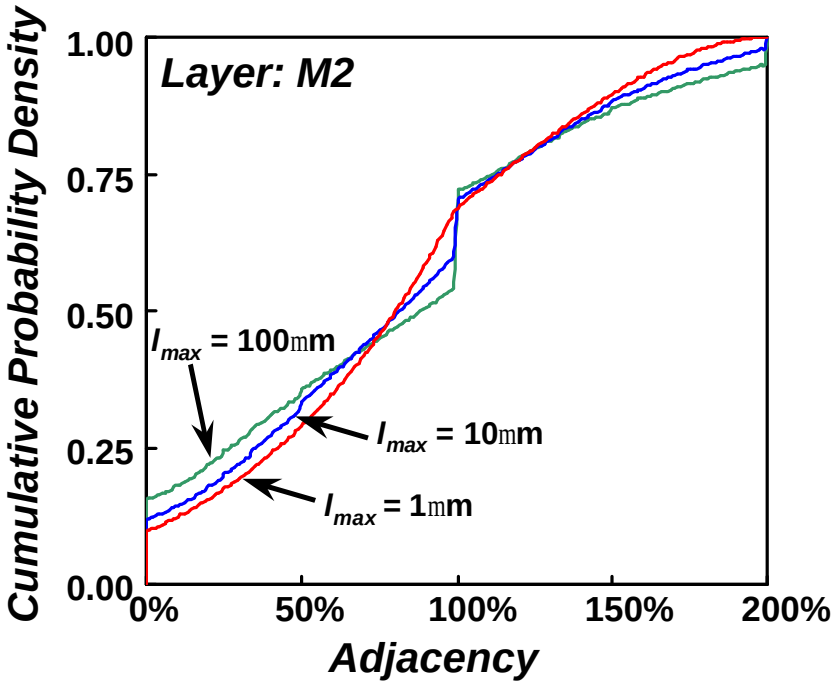
Metal layer = M4
Channel utilization = 42%
Gate pitch = 1.0 μm
Max wire length = 150 μm
Grid size = 0.01 μm

Sensitivity to Length Distribution

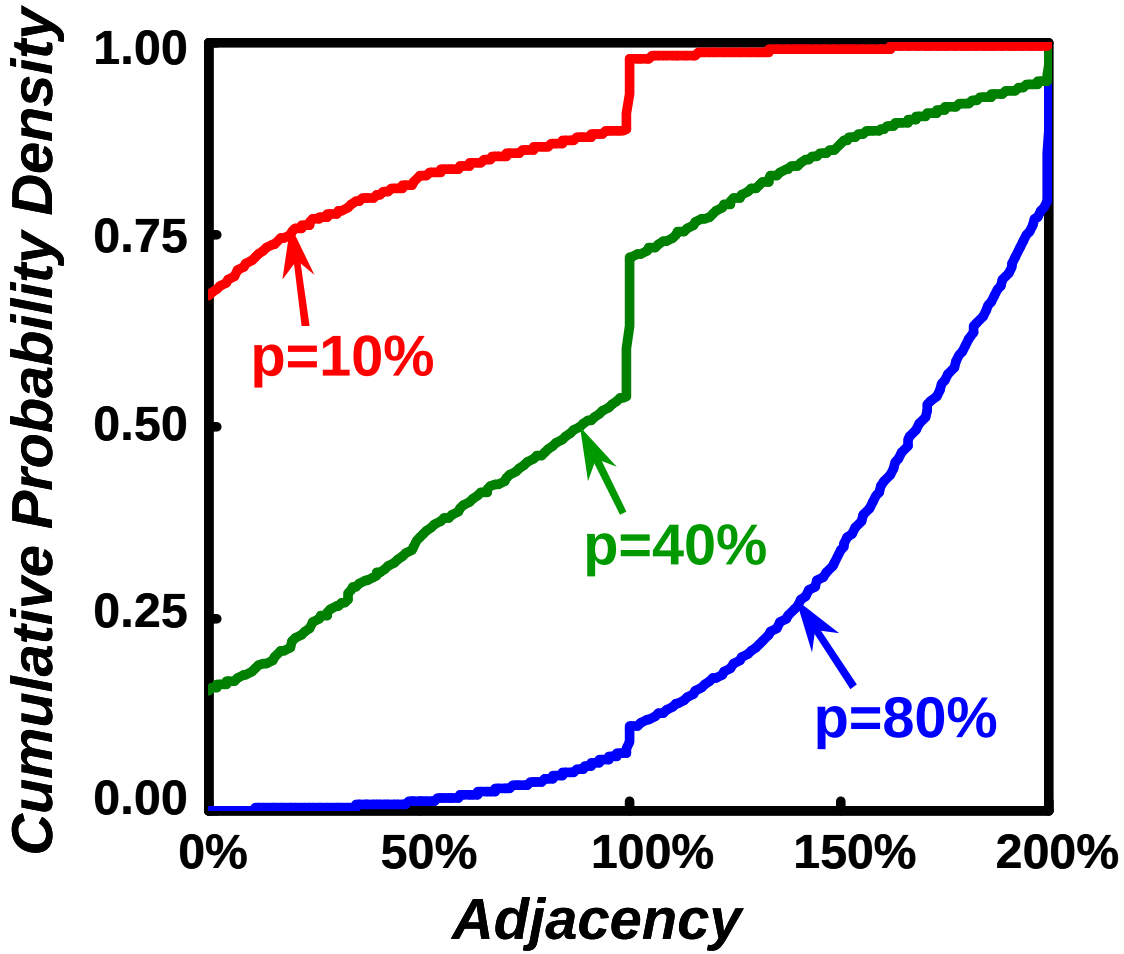
Change in a



Change in l_{max}



Adjacency Distribution Change with p



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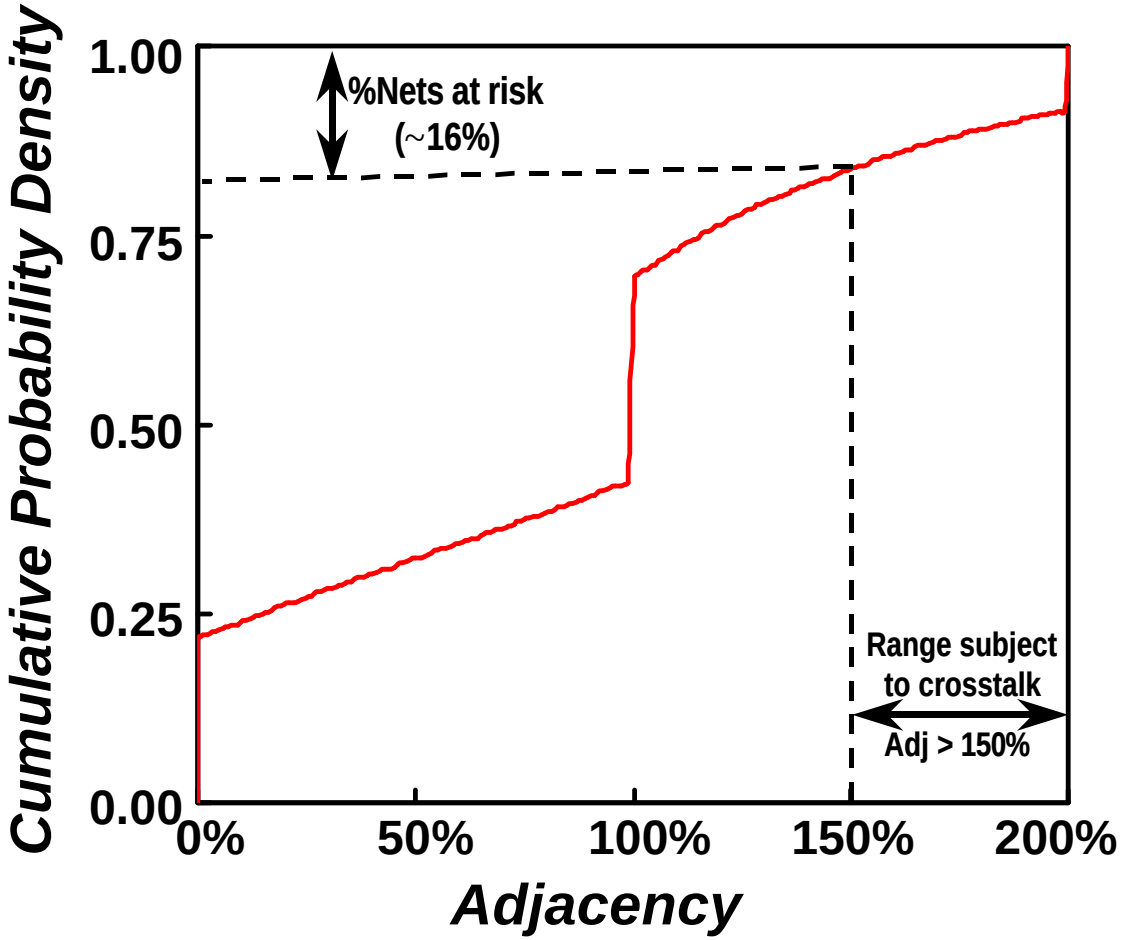
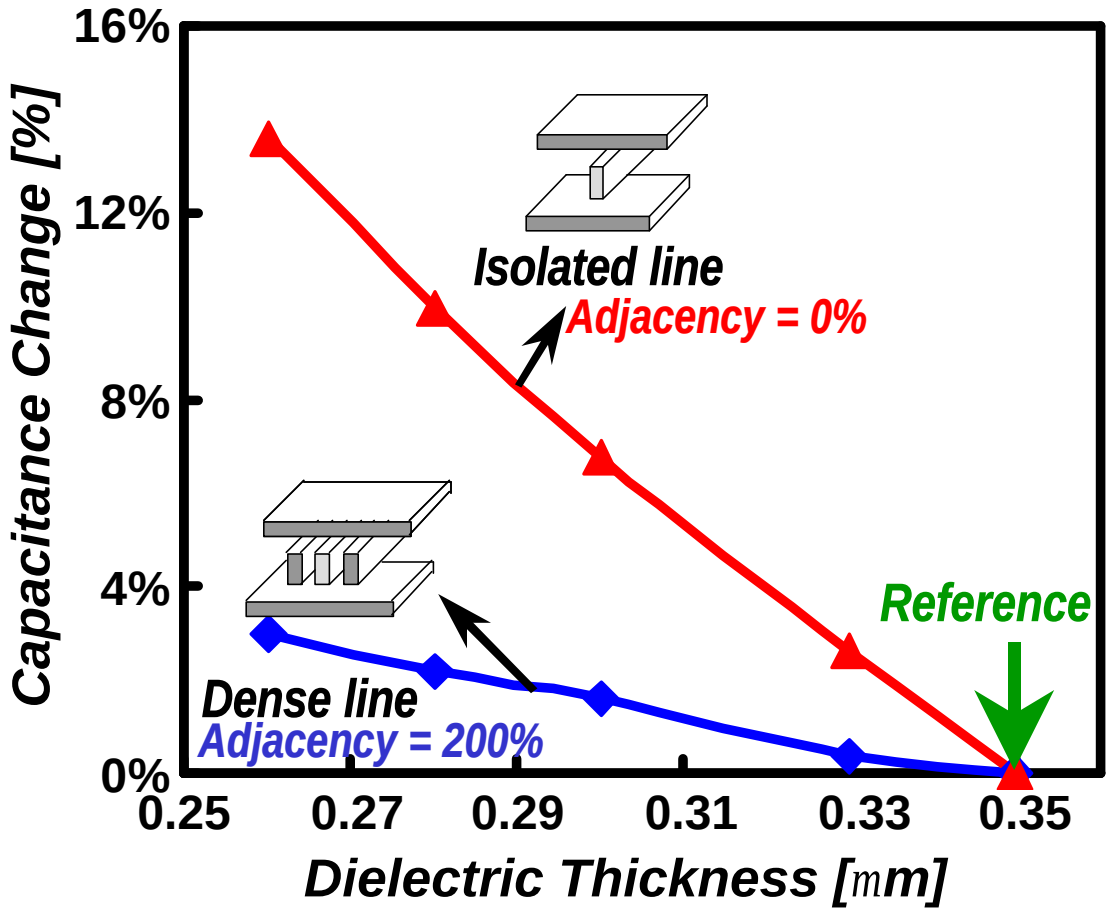
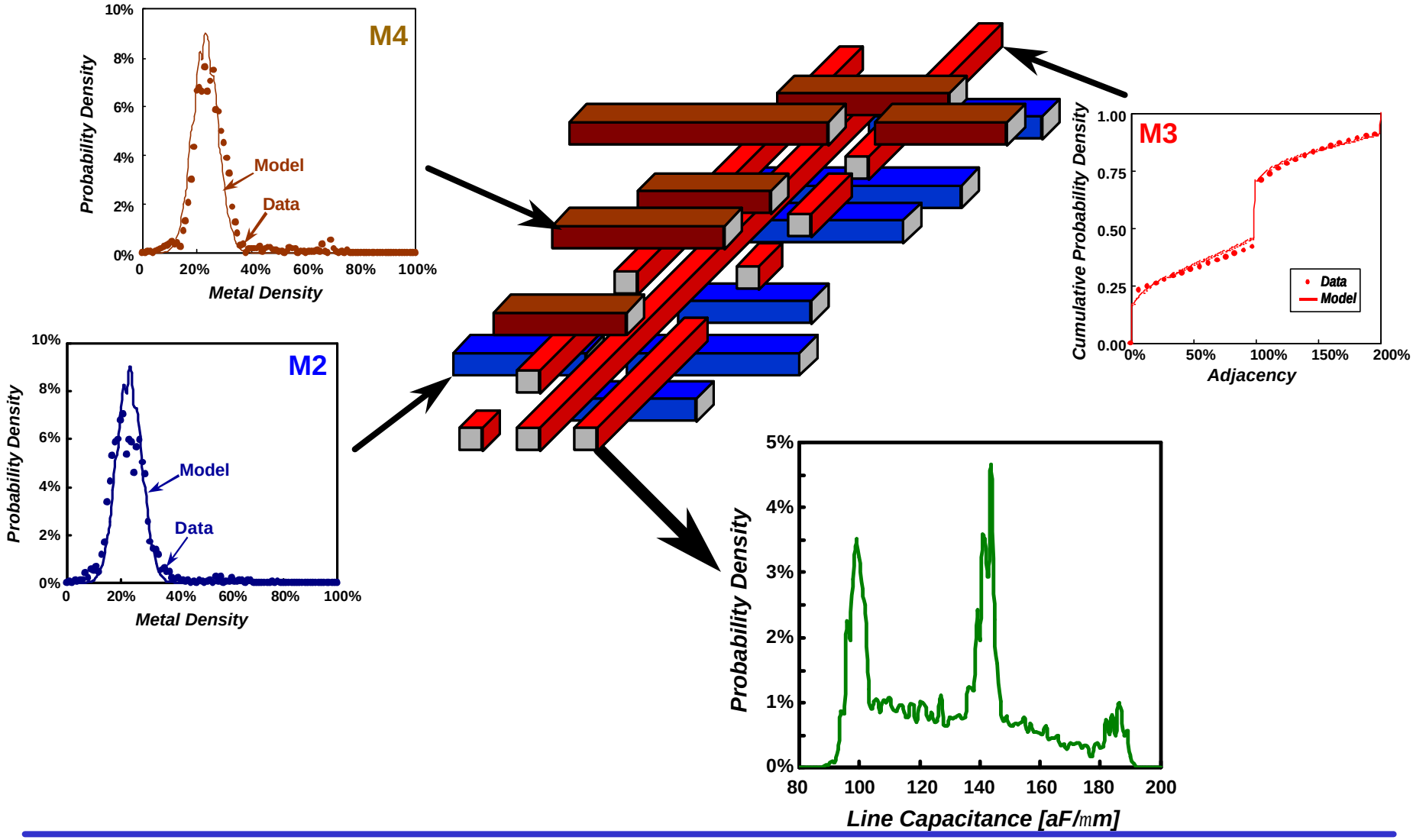
Statistical Crosstalk Analysis



Sensitivity Analysis



Interconnect Statistical Reference



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Conclusions

- Compact model for Interconnect Adjacency Distribution for random logic networks is derived.
- The model uses only system level generic parameters such as segment length distribution and channel utilization. This enables us to predict future system level performance.
- Comparison to product data confirms the accuracy of the model.
- Some possible applications of the adjacency are proposed.

Acknowledgement

We acknowledge Ralph Iverson from Magma Design Automation for his generous support in the extraction of the real data.