Prediction of Delay Time for Future LSI Using On-Chip Transmission Line Interconnects

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Outline

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(2) Derivation of Delay Distribution

(3) Replacement Method with Transmission Lines

(4) Simulation Conditions

(5) Experimental Results

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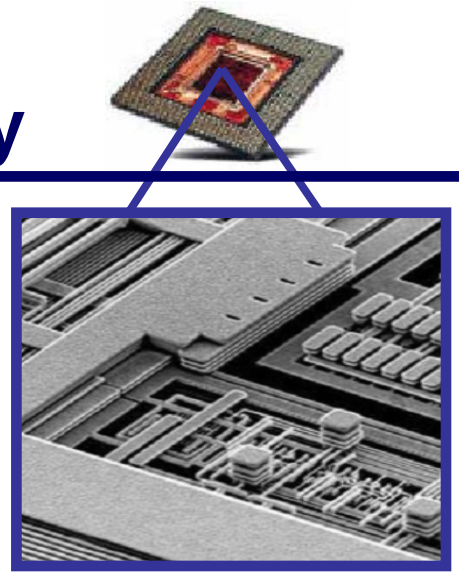
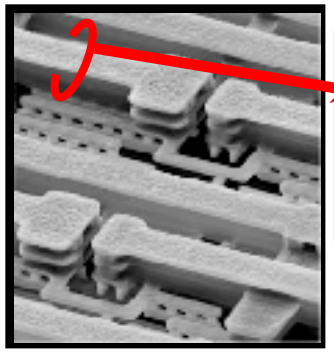
1. Background

Large Scaling of LSI
& Increasing of Clock Frequency



- Delay time of global interconnect ≫ Gate delay
- Signal wavelength ≒ Global interconnect length
- ωL : can not be neglected
  in analysis of signal propagation

⟶ Global interconnect ≠ RC lumped constant circuit



Transmission line can be realized in Si ULSI using the inductance of interconnect.

2. Purpose

Main purpose

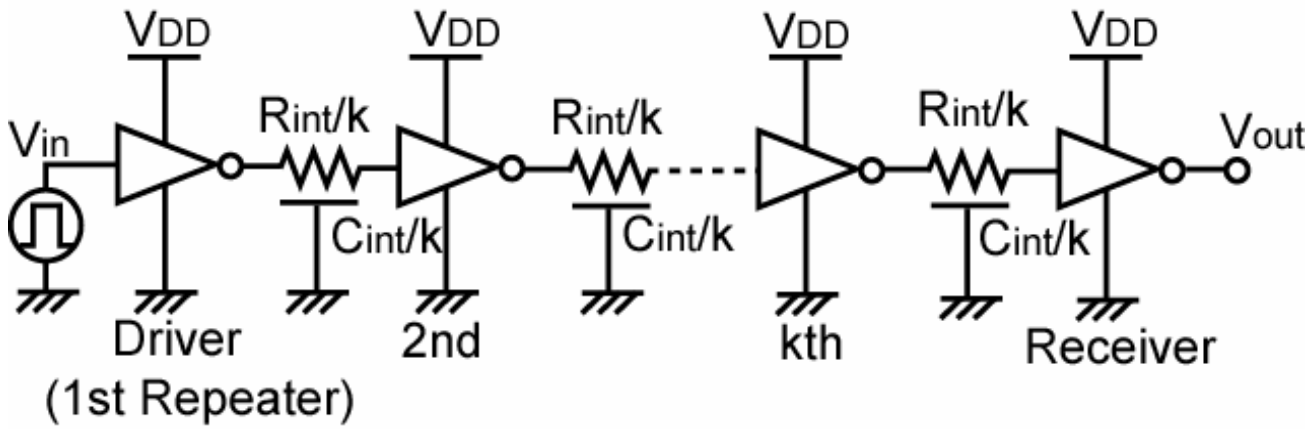
Estimation of future advantages of on-chip transmission line interconnects

advantage of transmission line → operating frequency of circuit designed with on-chip transmission line interconnects

The on-chip transmission line has smaller delay and smaller power consumption than RC interconnect at the long wire length.

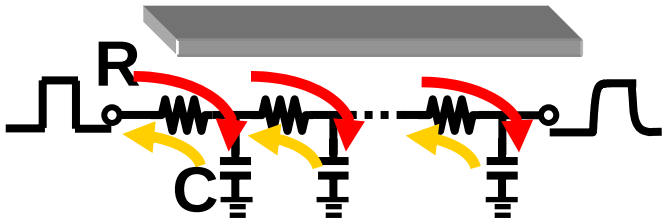
Replacement with the on-chip transmission lines can improve critical-path delay.

3. RC Line



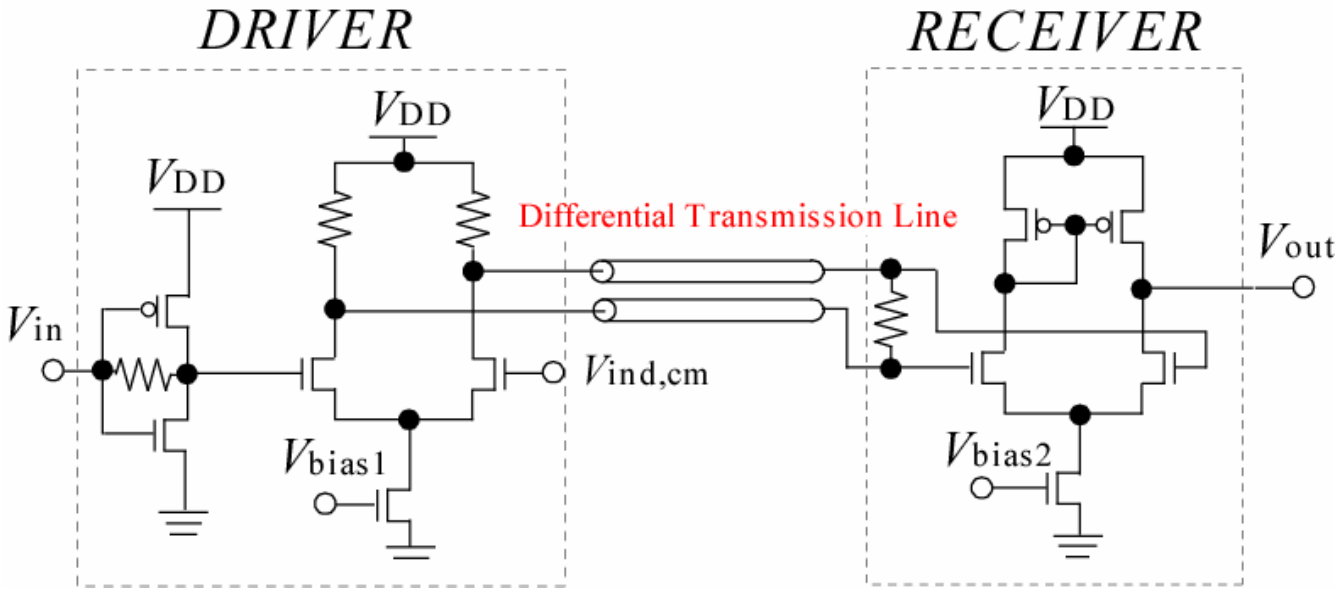
As RC line becomes longer,

- Delay time increases.
  More repeaters are required.
- Power consumption increases.

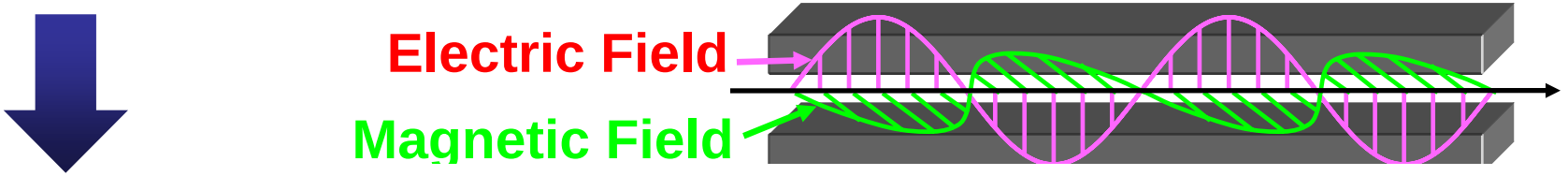


Trade-off between high-speed and power consumption

4. Transmission Line

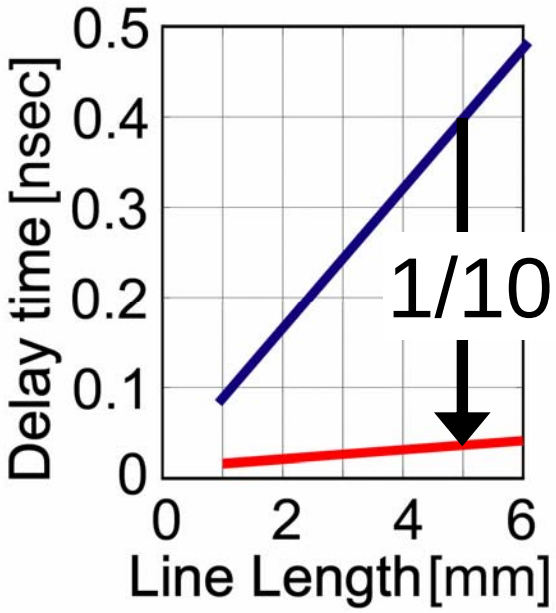


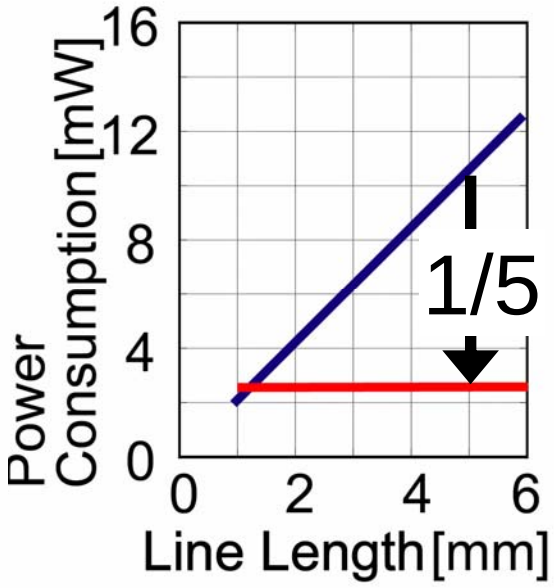
- Transmission lines can propagate signals at electromagnetic wave speed.
  - ⟶ High-speed signal propagation.
- Transmission line does not require repeaters.
  - ⟶ Low power consumption is expected for global interconnect.



High-speed signal propagation & Low power consumption

5. Comparison in Delay Time





45nm technology node

Delay time is proportional to the wire length.

RC line

➡ resistance and capacitance in interconnects

Transmission line

➡ electromagnetic wave

At 45nm technology node, delay time of transmission line is a tenth part of RC line delay, and transmission line can save power of 80% at 5mm length.

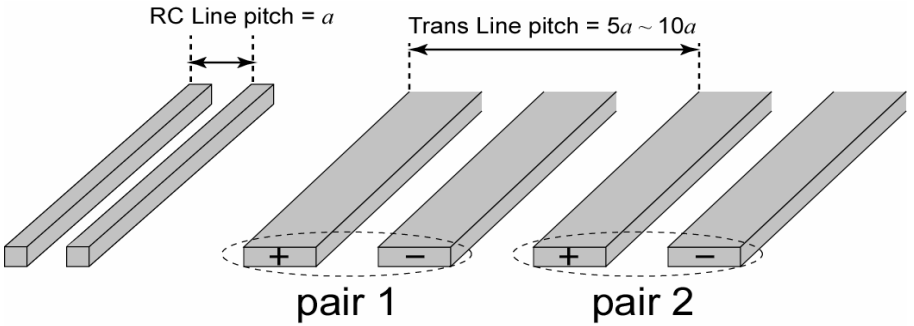
Delay time and power consumption are improved.

[1] H. Ito, *et al*., IEDM, pp.677-680 (2004).

6. Issue of Using Transmission Line

Problem area

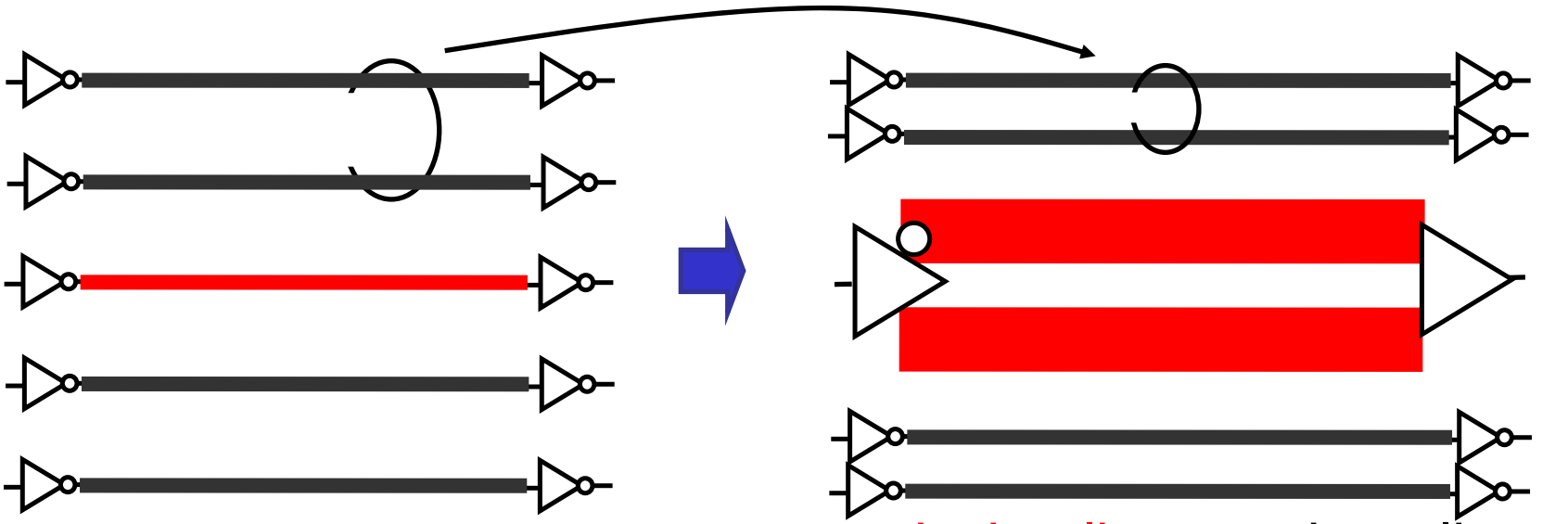
Transmission line requires large wiring area.



RC line Transmission line(Co-planar)

Replacement with Tr. lines

Wiring density becomes high.



RC lines Transmission lines and RC lines

Schematic of replacement with transmission line

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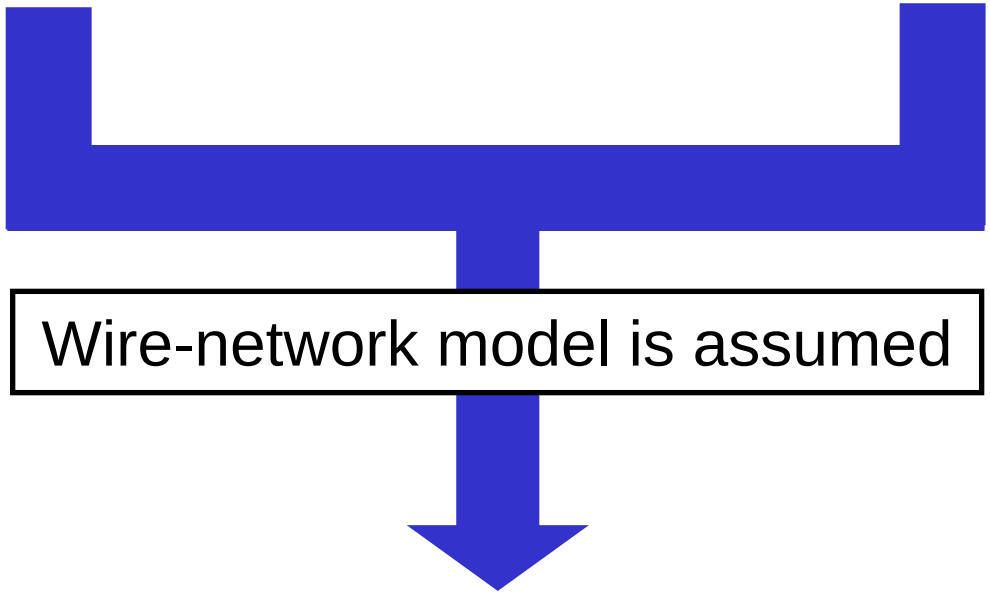
7. Derivation Flow of Delay Distribution

Delay distribution is used in the proposed method.

Wire Length Distribution

It is used to estimate the circuit performance.

Target delay distribution

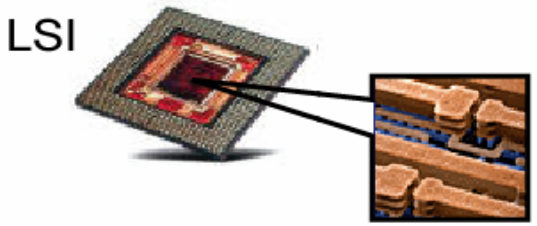


Each wire length is allocated from a wire-length set determined by wire length distribution statistically.

8. Wire Length Distribution (WLD)

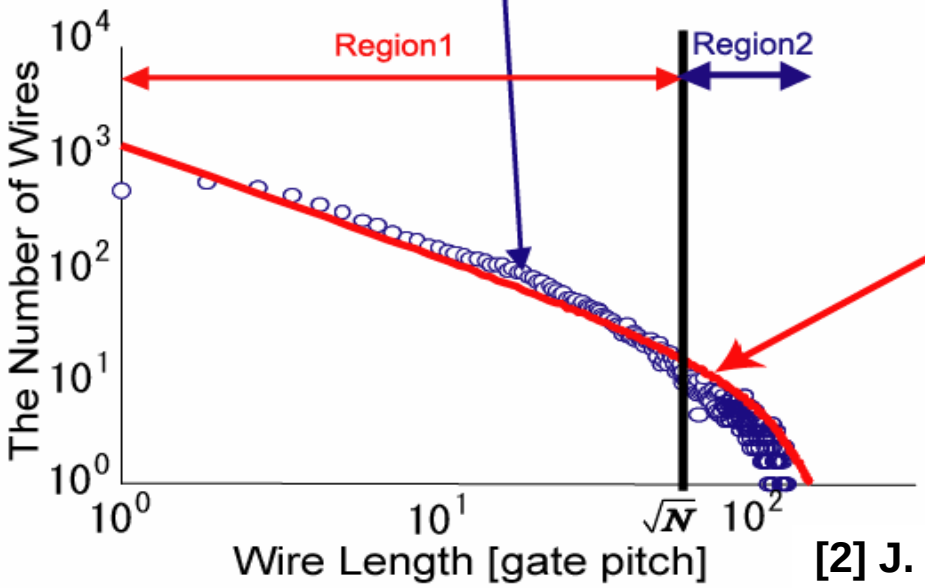
Wire Length Distribution : a relationship between wire length and the number of wires

- N: Number of gates
- p: Rent's exponent
- k: Rent's constant
- f_{out}: fan-out



Extraction

Wire Data



Derivation

Model Equations

Region1: $1 \le l < \sqrt{N}$

$$i(l) = \frac{\alpha k}{2}\Gamma\left(\frac{l^3}{3} - \sqrt{2}Nl^2 + 2Nl\right)l^{2p-4} \quad (1)$$

Region2: $\sqrt{N} \le l < \sqrt{N}$

$$i(l) = \frac{\alpha k}{6}\Gamma\left(2\sqrt{N} - l\right)^3 l^{2p-4} \quad (2)$$

$$\Gamma = \frac{2N(1-N^{p-1})}{-N^p \frac{1+2p-2^{2p-1}}{p(2p-1)(p-1)(2p-3)} - \frac{1}{6p}\frac{2\sqrt{N}}{2p-1} - \frac{N}{p-1}} \qquad \alpha = \frac{f.o.}{f.o.+1}$$

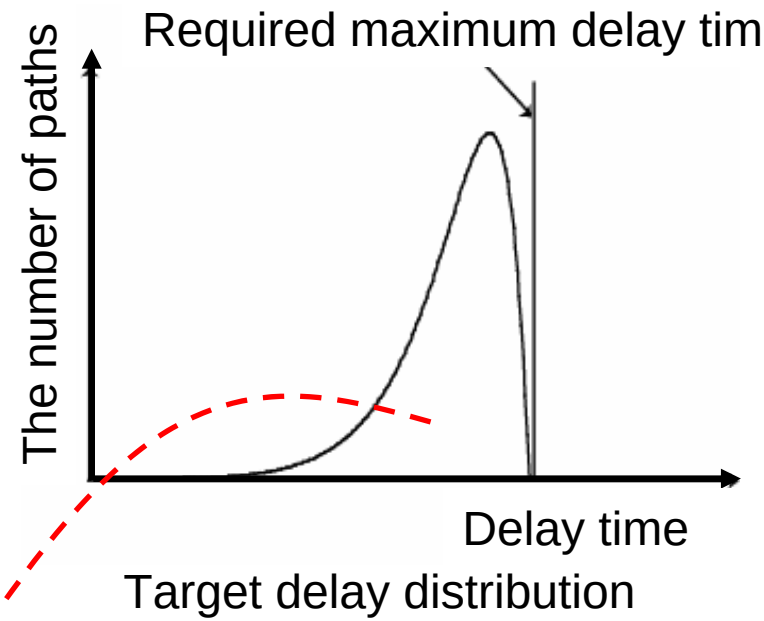
[2] J. Davis, *et al.*, IEEE ED, vol 45, pp.580-589 (1998).

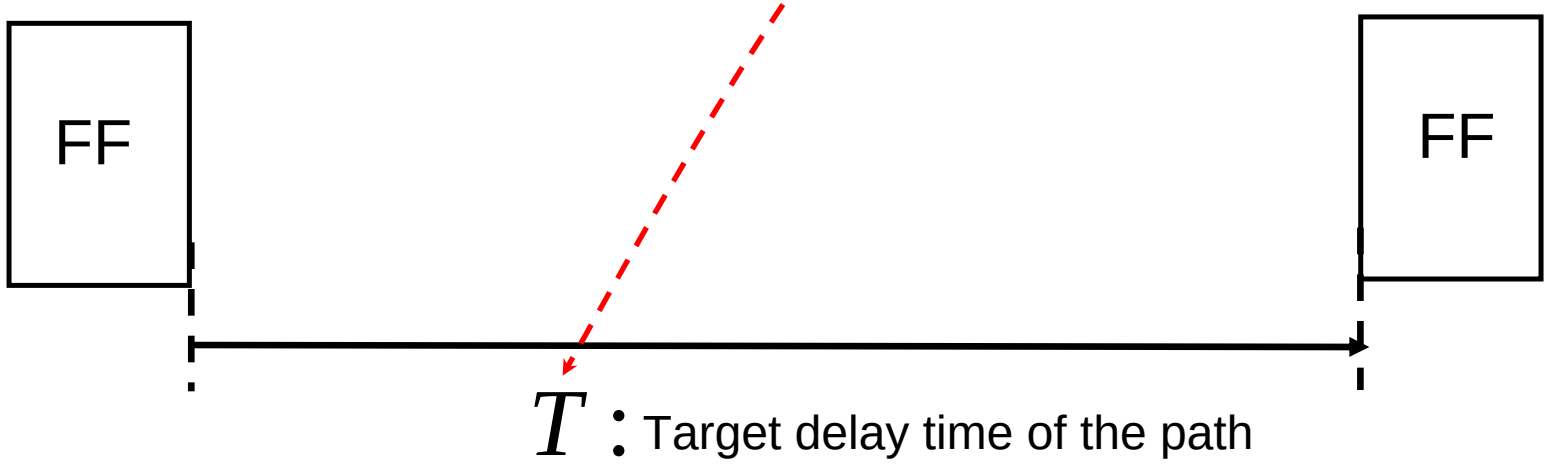
9. Derivation of Delay Distribution 1

In the proposed algorithm, paths in the circuit is reconstructed so that the circuit has target delay distribution.

Derivation Step

1. Target delay of the path is determined by the probability of target delay distribution.



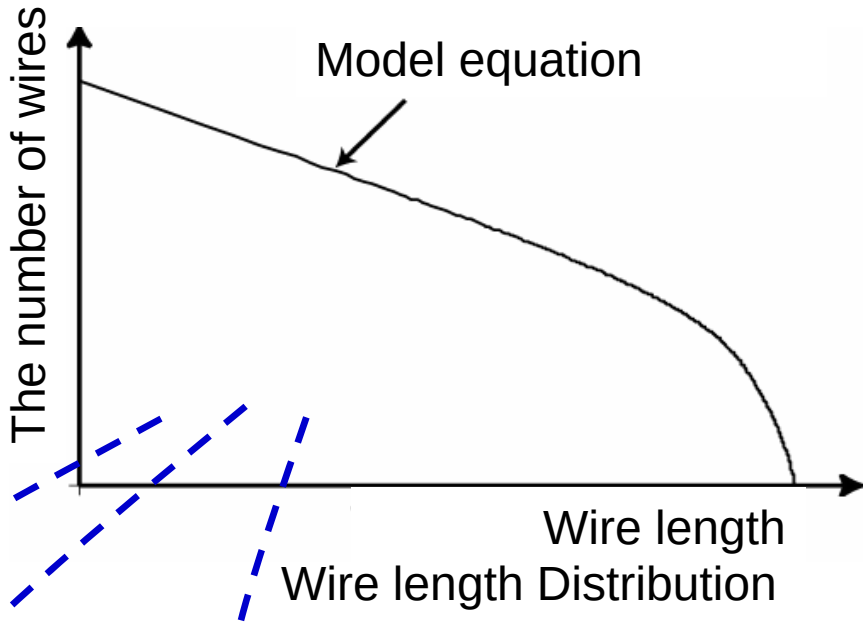


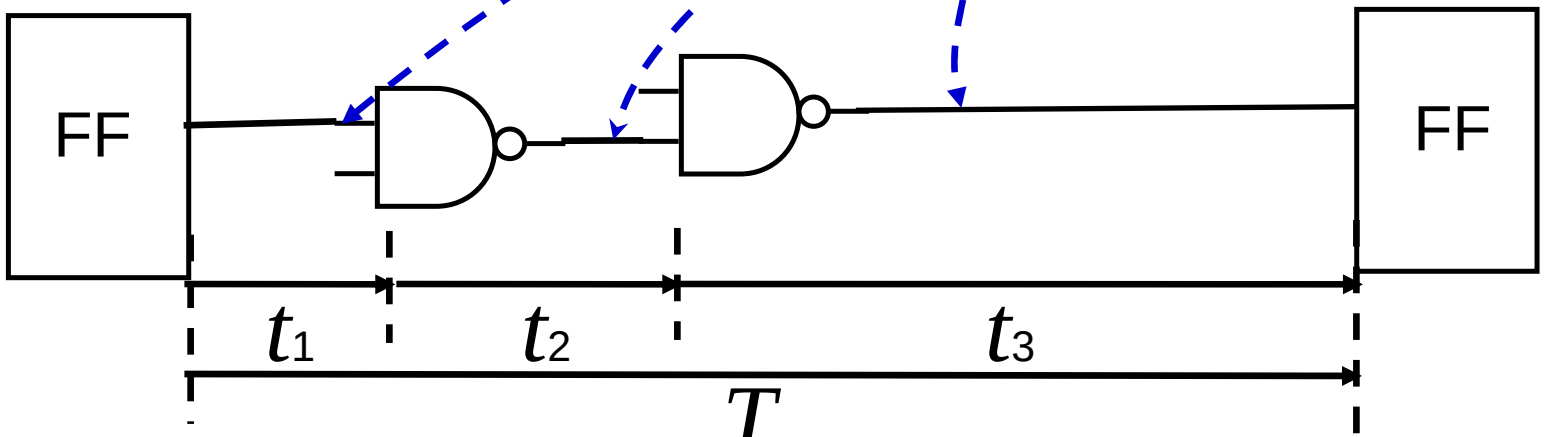
10. Derivation of Delay Distribution 2

Derivation Step

2. The number of gates is incremented and wire length is determined by the probability of the wire length distribution.

3. Step 2 is repeated while path delay is less than target path-delay.





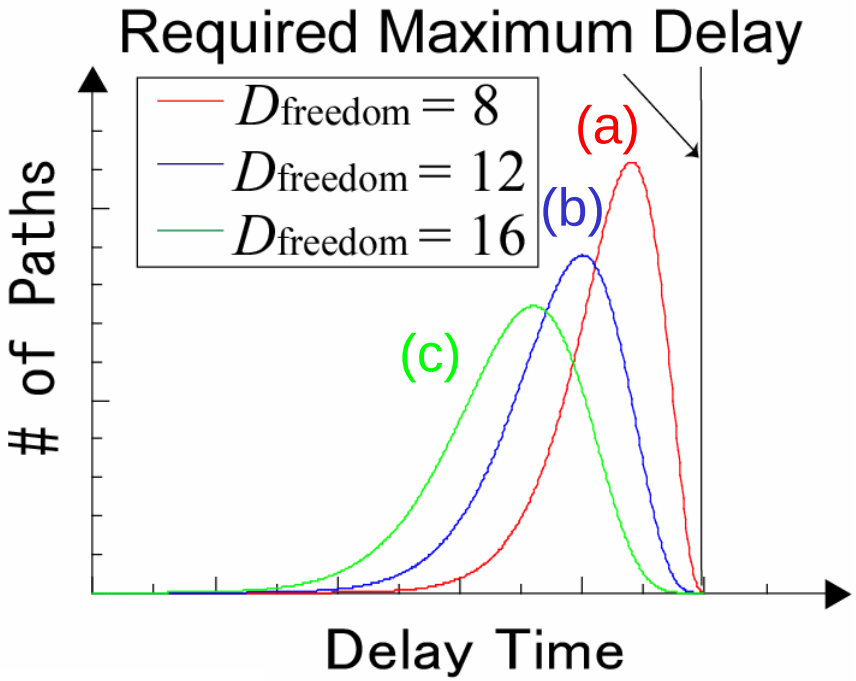
$$t_1 + t_2 + t_3 < T$$

11. Target Delay Distribution

We assume the chi-square distribution as the target delay distribution.

Chi-square distribution is characterized by one parameter, degree of freedom.

Degree of freedom D_{freedom} ⟷ How optimized the circuit is



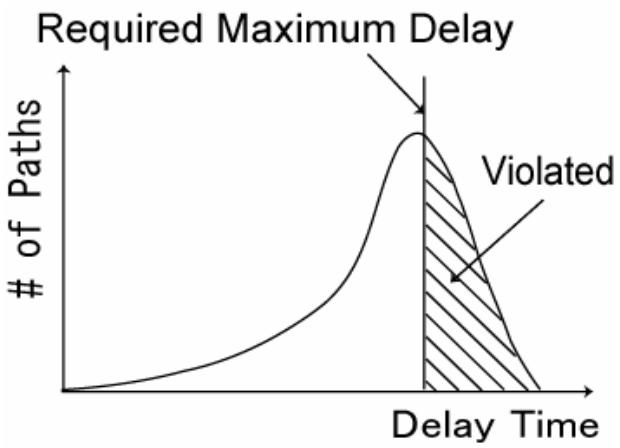
The distribution (a), (b) and (c) have the same function and the same netlist, and different wire topology and gate sizes.

All distributions satisfy the required delay.

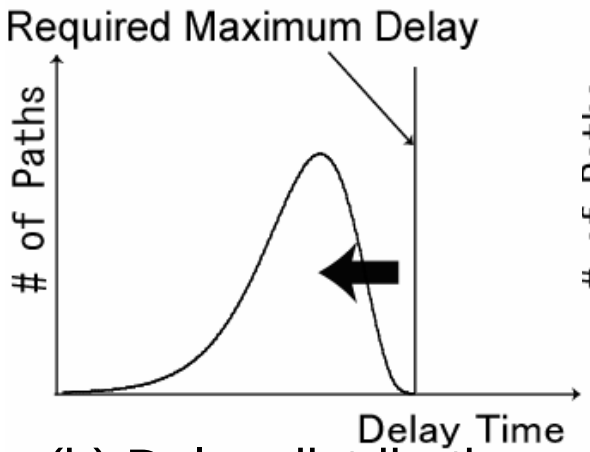
The distribution (a) requires the smaller power consumption.

The circuit having the distribution (a) can be regarded as a more optimized circuit.

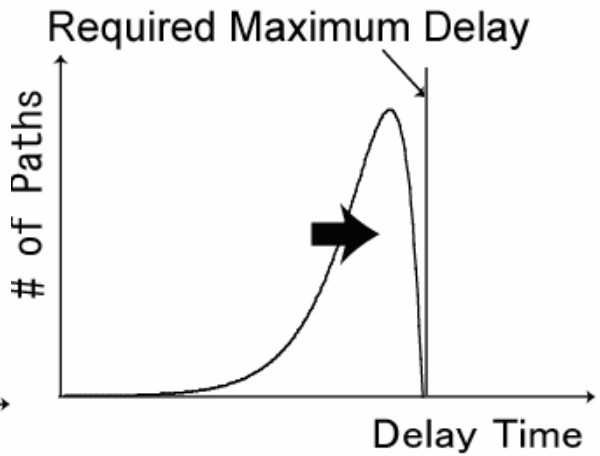
12. Delay Distribution of Actual Circuit



(a) Delay distribution before optimization



(b) Delay distribution optimized for delay



(c) Delay distribution optimized for power

Optimization for delay

- The violated paths are divided by several repeaters
- The gate sizes on the paths are increased.

operated simultaneously

Optimization for power consumption

- Repeaters in the fast paths are removed.
- The gate size in the fast paths is decreased.

➡ A lot of paths don't have too fast nor too slow delay.

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13. Replacement with Transmission Lines

• Operating frequency of the circuit depends on the critical-path delay.
• Critical-path delay depends on long wire in the path.
• The on-chip transmission line has smaller delay than RC line at the long wire length.

The longest RC lines in critical paths are replaced with transmission lines.

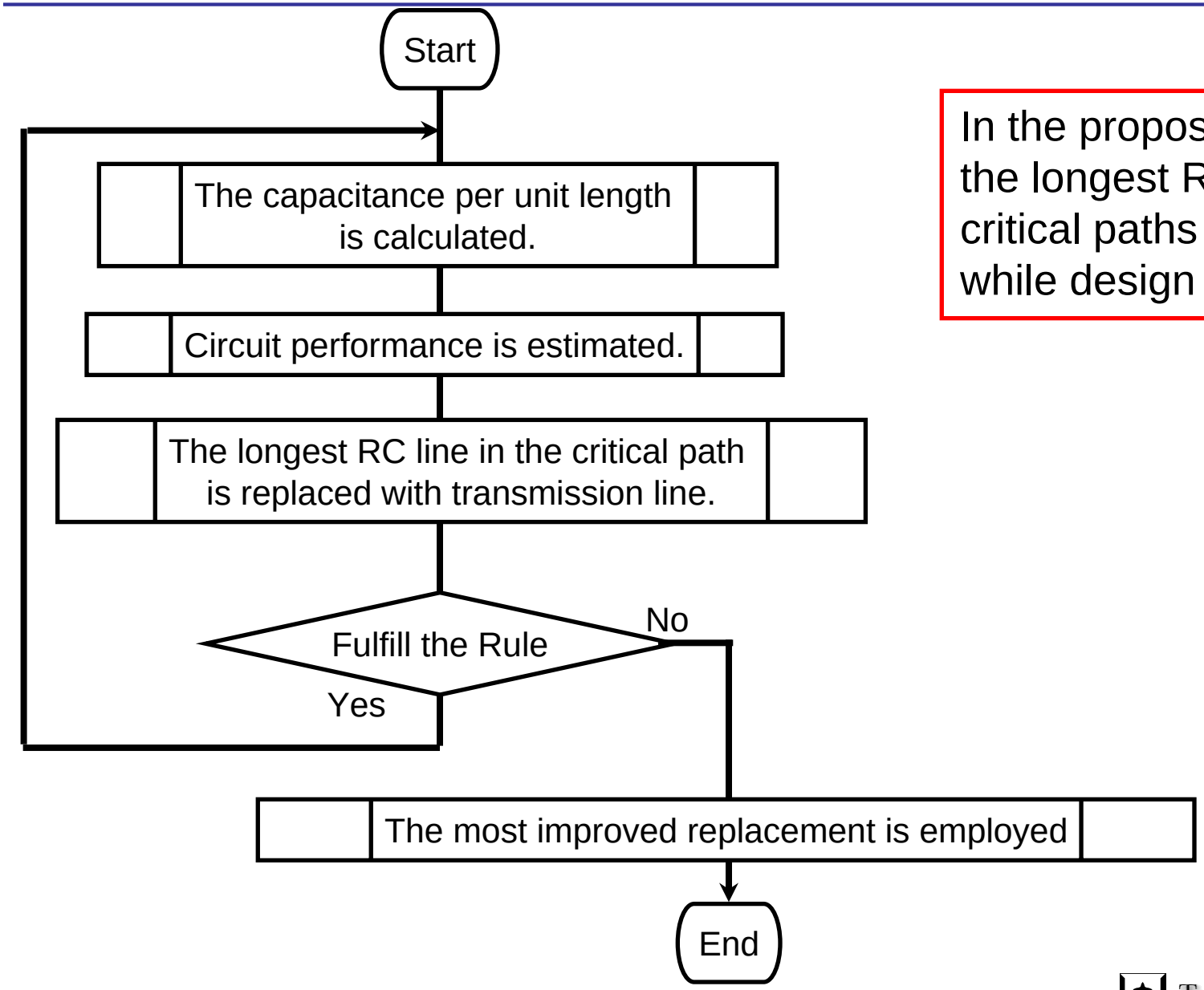
Problem

Transmission line requires large wiring area.

{ replaced line → Line delay is improved.
{ other RC line → Line delay is a little degraded.

replacement too many RC lines → Degradation becomes larger than improvement.

14. Replacement Algorithm



In the proposed algorithm, the longest RC lines in the critical paths are replaced while design rule is fulfilled

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15. Benchmark Circuits and Assumptions

Technology node	180nm	90nm	45nm
Number of gates	15.5M gates	60M gates	240M gates
Chip size	$3.1cm^2$		
Number of average pins (k)	2.5		
Average fan-out (f_{out})	1.5		
Rent's constant (p)	0.4		
Operating frequency	1.25GHz	2.5GHz	5GHz
Number of metal layers	8	10	12
Gate output resistance	$6.3k\Omega$		
Gate input capacitance	1.7fF	0.87fF	0.43fF
Degree of freedom (D_{freedom})	8, 12, 16		

16. Estimation Equations

Optimal delay time

$$T = 2.5\sqrt{R_0 R_{\text{int}} C_0 C_{\text{int}}}$$

The optimal number of repeaters

$$k = \sqrt{\frac{0.4 R_{\text{int}} C_{\text{int}}}{0.7 R_0 C_0}}$$

Proportion of optimal W/L

$$h = \sqrt{\frac{R_0 C_{\text{int}}}{R_{\text{int}} C_0}}$$

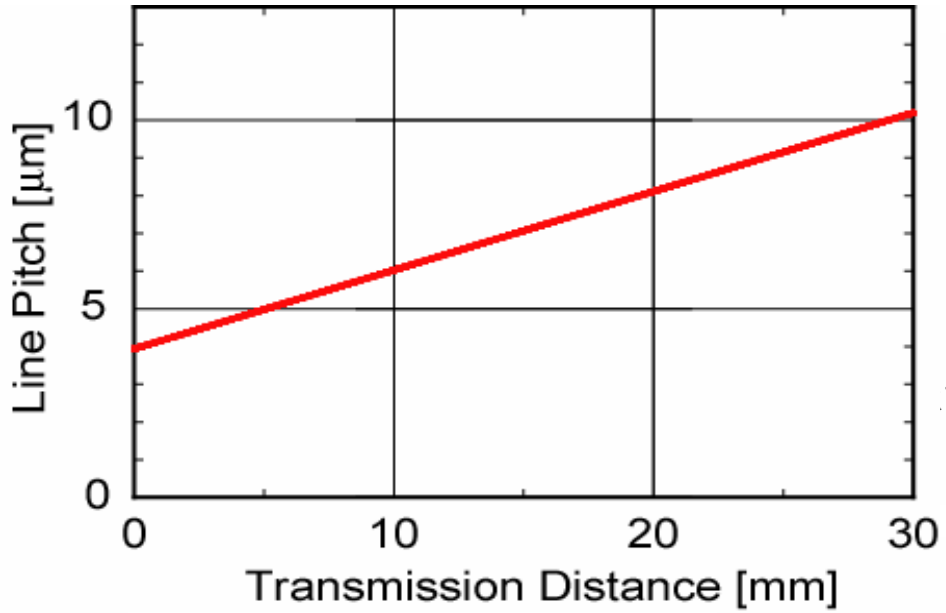
R_0: gate output resistance
C_0: gate input capacitance
R_{int}: wire resistance
C_{int}: wire capacitance

Delay time without any repeaters

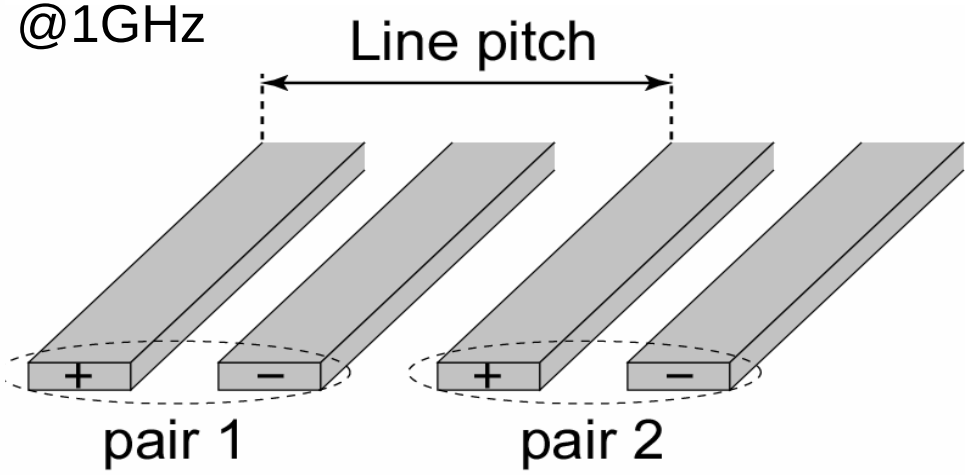
$$T = 0.4 R_{\text{int}} C_{\text{int}} + 0.7(R_0 C_{\text{int}} + R_0 C_0 + R_{\text{int}} C_0)$$

[3]H. B. Bakoglu, “Circuits, Interconnections, and Packaging for VLSI,” Chapters 5-7 (1995).

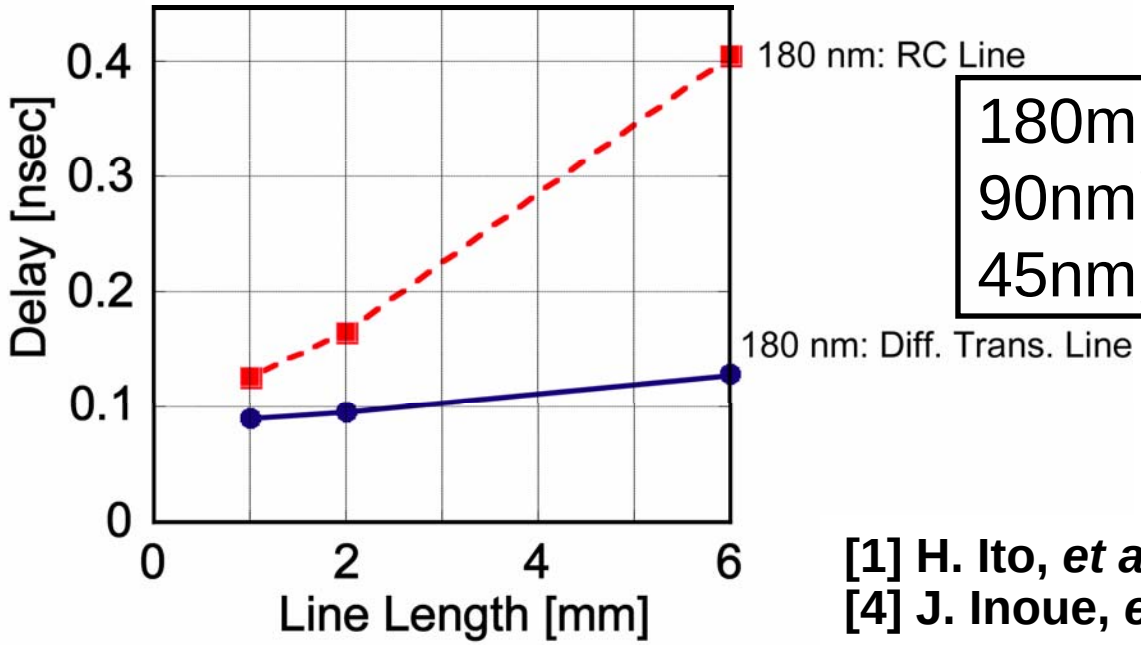
17. Transmission Line Conditions



@1GHz



Co-planar structure



180mn → measured
90nm, 45nm → derived from 180nm with ITRS

[1] H. Ito, *et al*., IEDM, pp.677-680 (2004).
[4] J. Inoue, *et al*., ASP-DAC, pp.133-138(2005)

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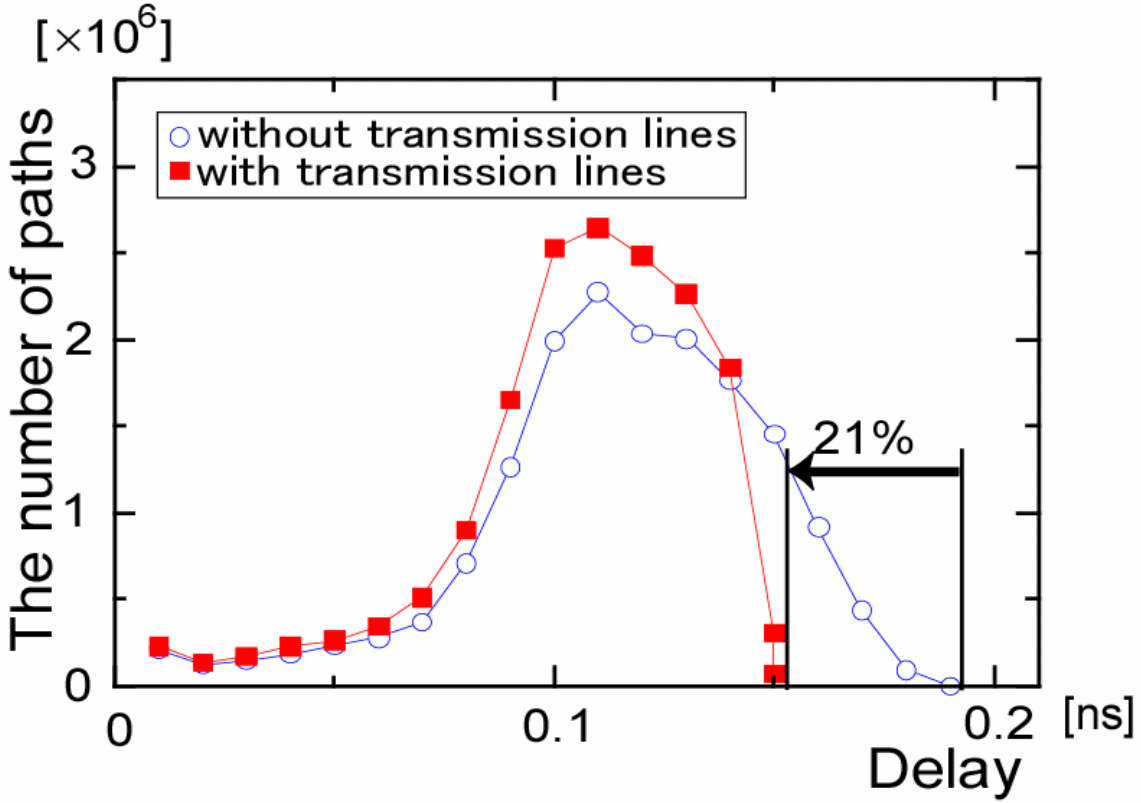
18. Experimental Results

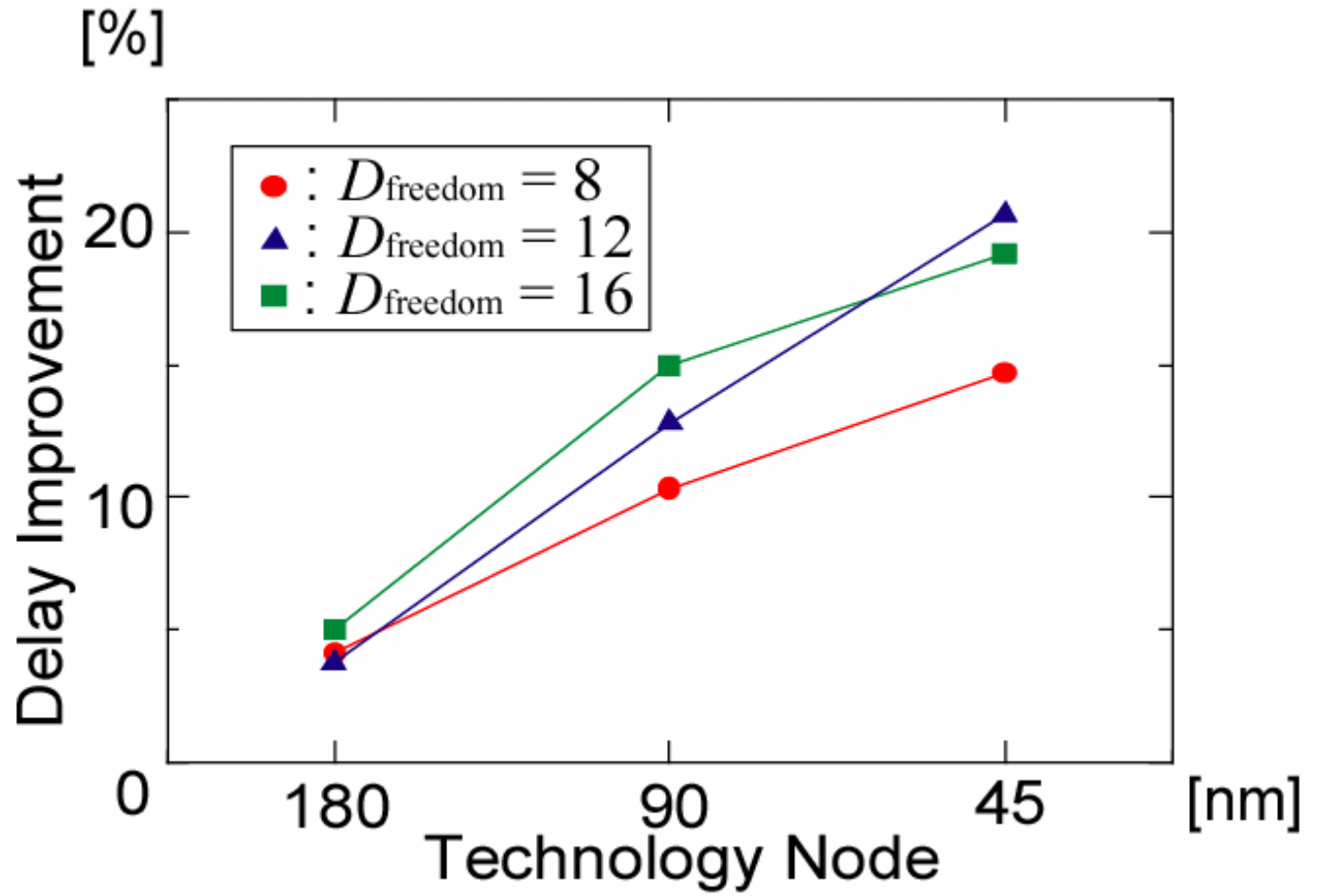


Delay distributions

(45nm technology node, D_{freedom} = 12)

- At 45nm technology node, the replacement with transmission lines improved critical-path delay by 21%.

19. Experimental Results



In spite of the target delay distributions, the replacement with transmission lines has more advantage as technology node advances.

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20. Summary and Conclusion

We estimated operating frequency of LSI with on-chip transmission line interconnects.

The longest RC lines in the critical paths are replaced with on-chip transmission lines.

In spite of the target delay distributions, the replacement with transmission lines has more advantage as technology node advances.

Replacement with the transmission line interconnects becomes an indispensable method at the future technology node.