# Multilevel Full-Chip Routing with Testability and Yield Enhancement


***Katherine Shu-Min Li, Chung-Len Lee, Yao-Wen Chang*, Chauchin Su and J. E Chen****

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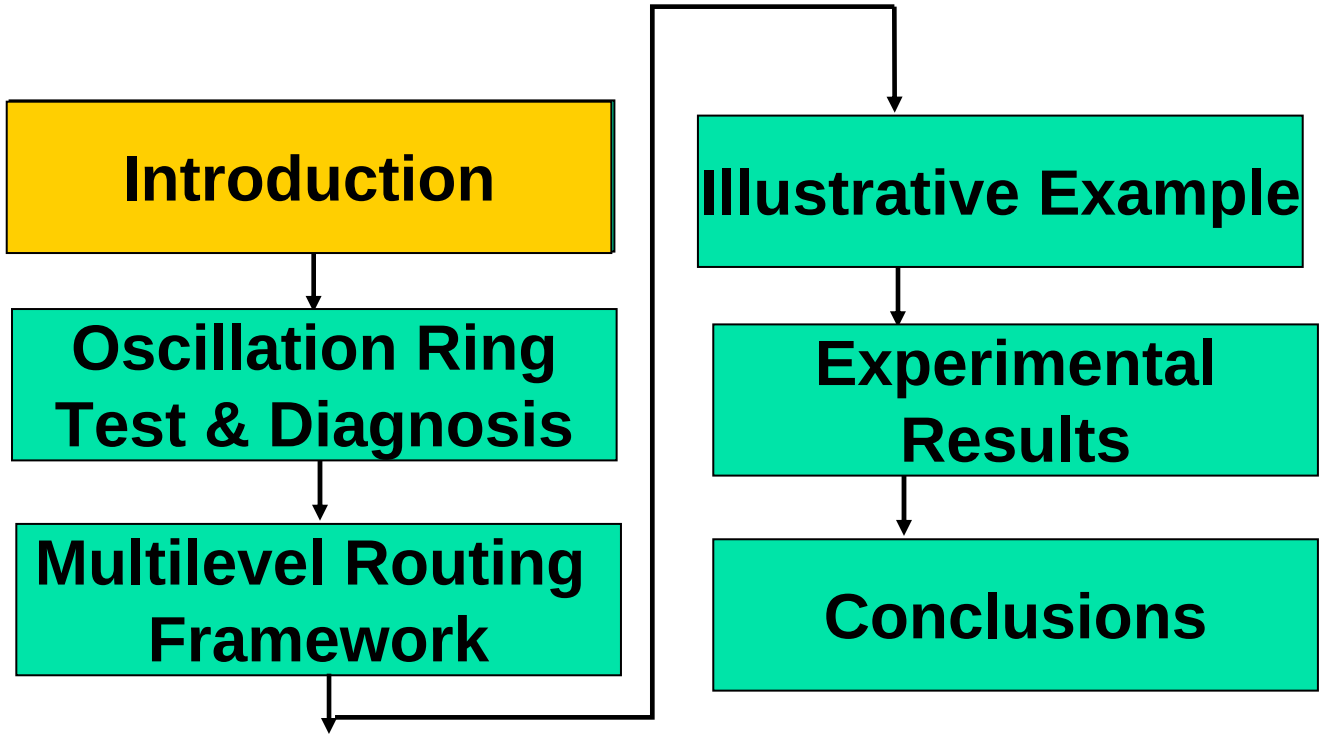
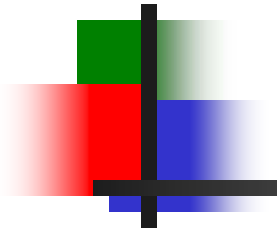
# Outline


Introduction
Oscillation Ring Test & Diagnosis
Multilevel Routing Framework
Illustrative Example
Experimental Results
Conclusions

# Introduction

- Interconnect plays a dominant role in deep submicron era
  - determines circuit performance and signal integrity
    - Delay Fault
    - Crosstalk Glitch Fault
- Interconnect Test
  - Board-level
  - System-level





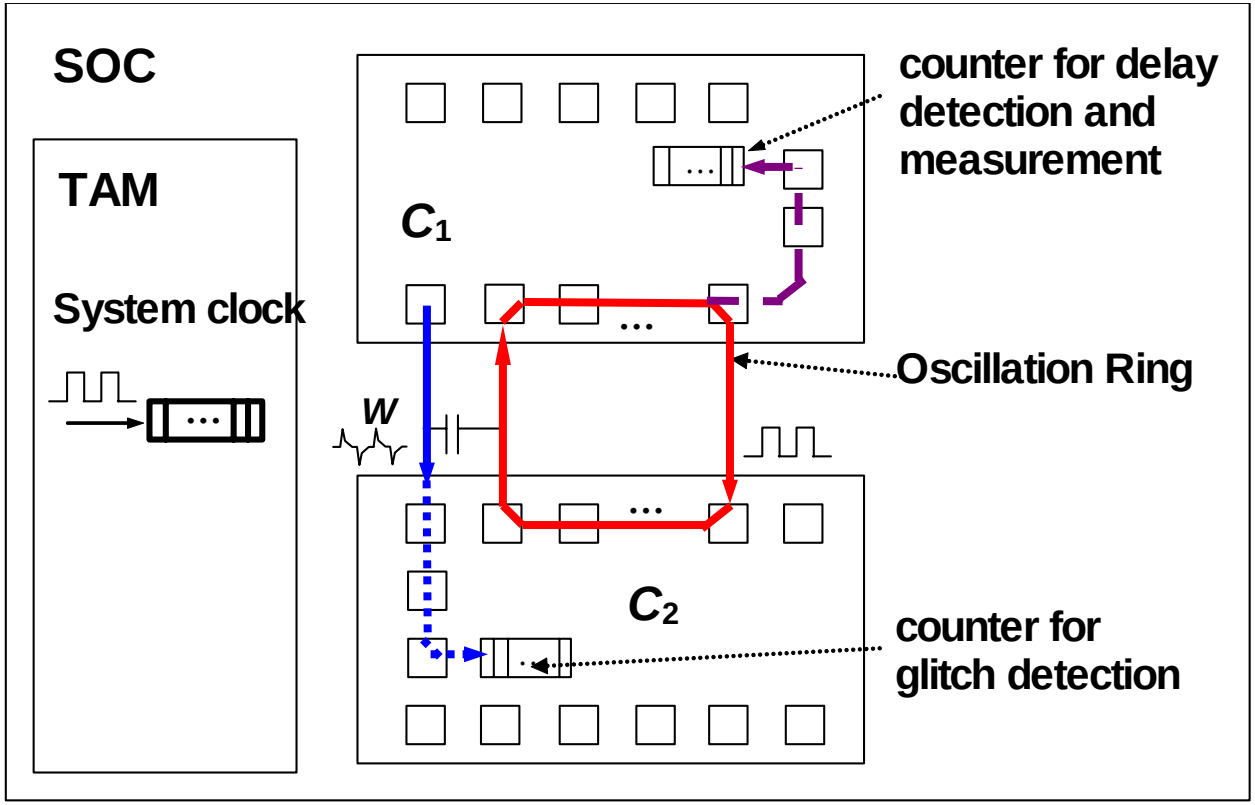
# Introduction (Cont'd)

- **IEEE P1500 standards**
  - **provide structural support for core testing and interconnect testing in SoC**
- **Our Proposed Oscillation Ring (OR) Test Architecture**
  - **detects stuck-at and open, also delay and crosstalk glitch**
  - **measures delay period**

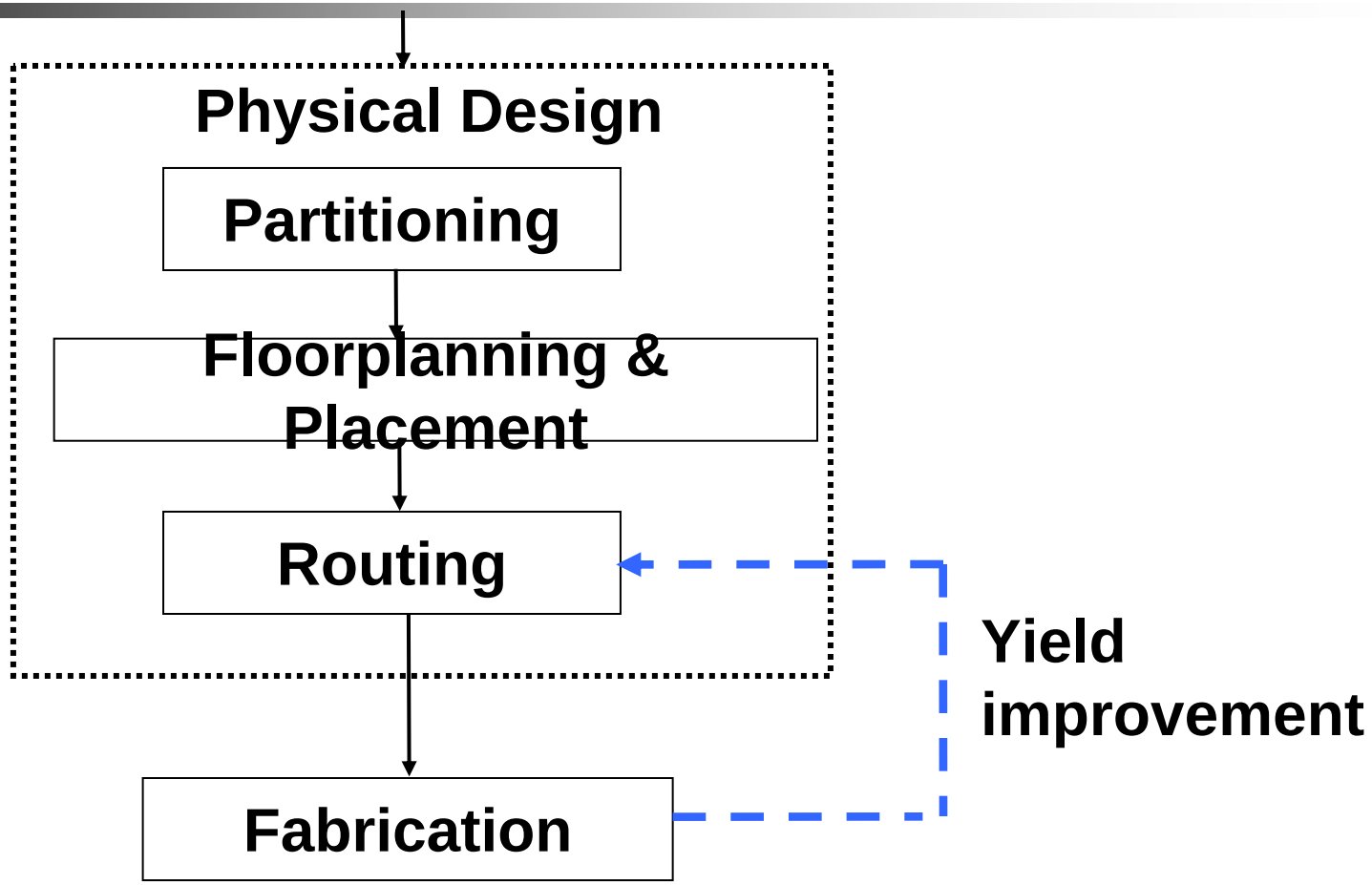
# Two Motivations

- **Testability Enhancement:**
  - **Propose integrated multilevel routing framework with embedded oscillation ring (OR) test architecture**
    - to detect stuck-at and open, also delay and crosstalk glitch
    - to measure delay period
- **Yield Enhancement:**
  - **Propose Congestion-Control guided routing**

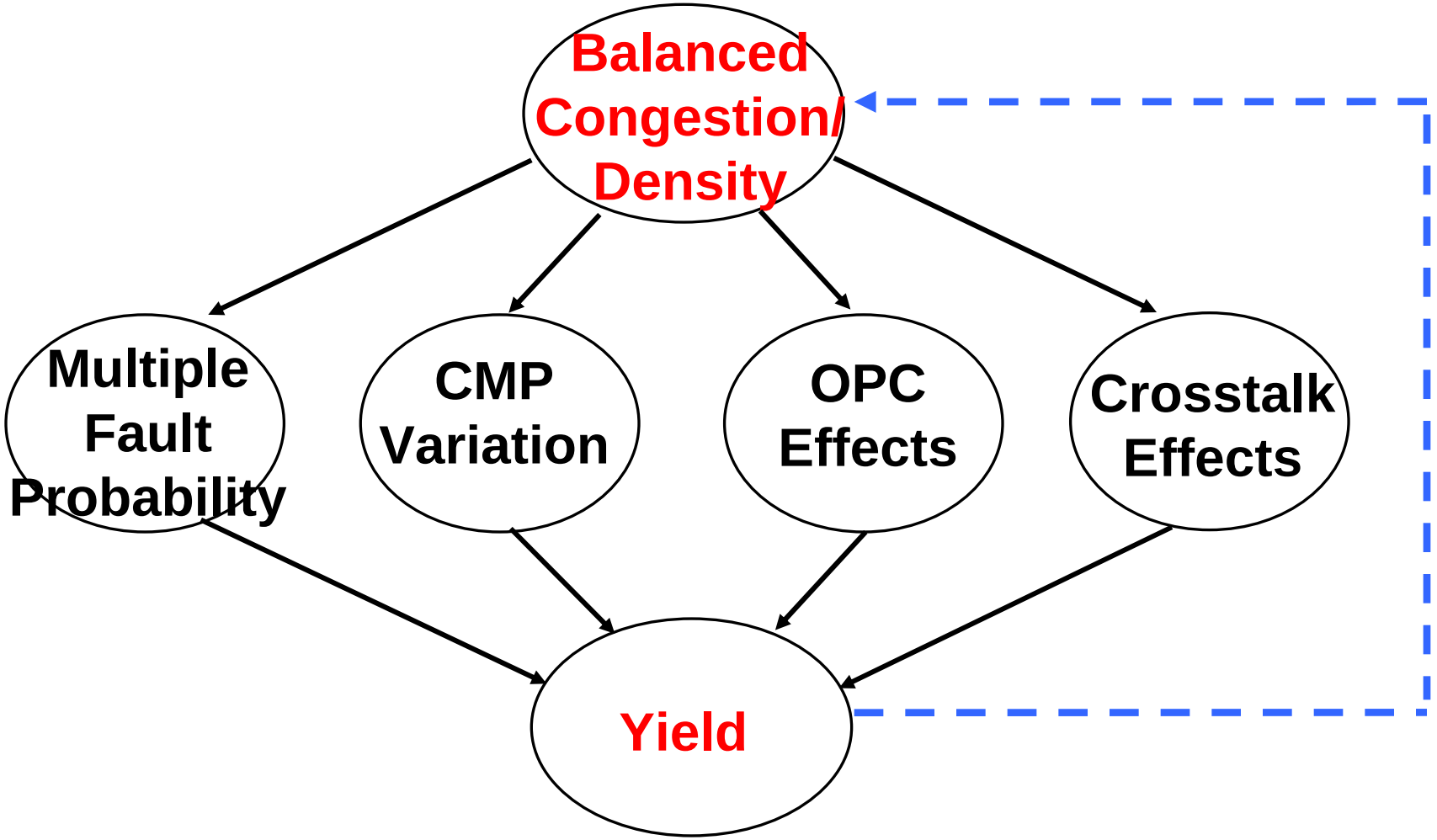
# Motivation for Testability Enhancement: OR Test Architecture for Interconnect (1/2)

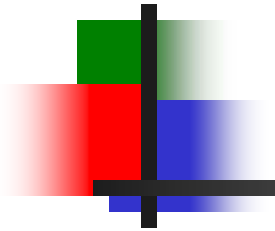


# Motivation for Yield Improvement (2/2)



# Motivation for Yield Improvement (Cont'd)



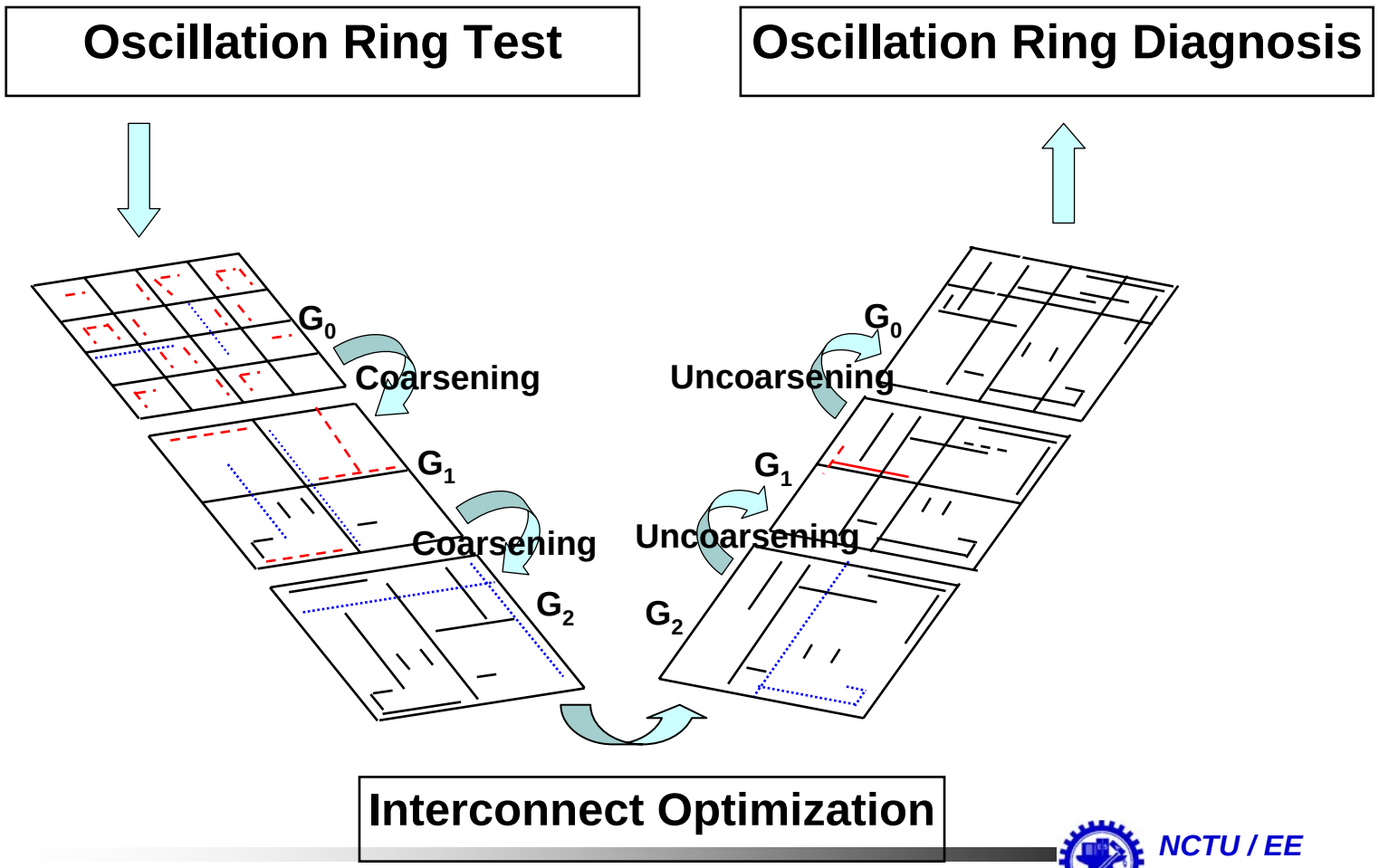


# Our Work

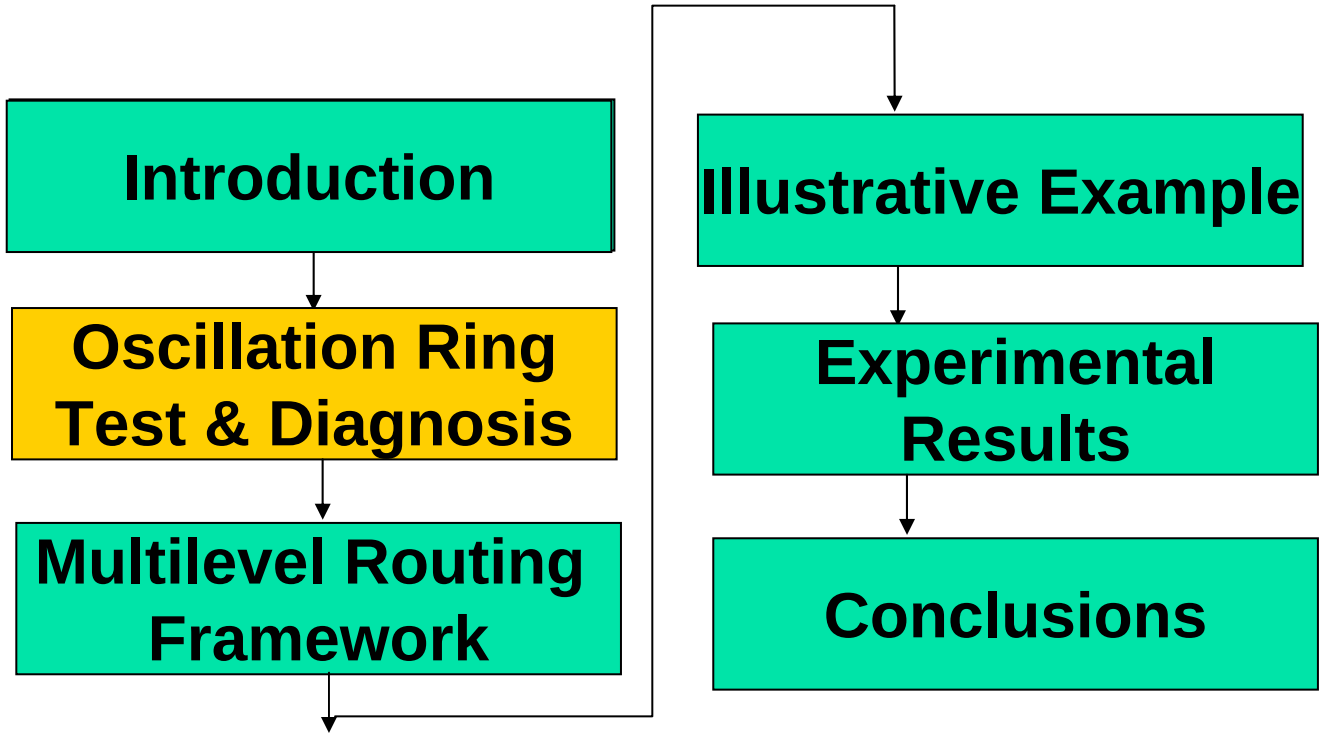
- **Consider testability and diagnosability, manufacturability, and signal integrity simultaneously in the multilevel routing framework.**
- **Provide testability and yield enhancement solutions in the routing stage to both diagnose interconnects and improve density flexibility**
- **Present heuristics to balance and reduce congestion in routing for yield improvement**

# Our Work (Cont'd)

- **Propose a new testability-driven multilevel routing framework:**



# Outline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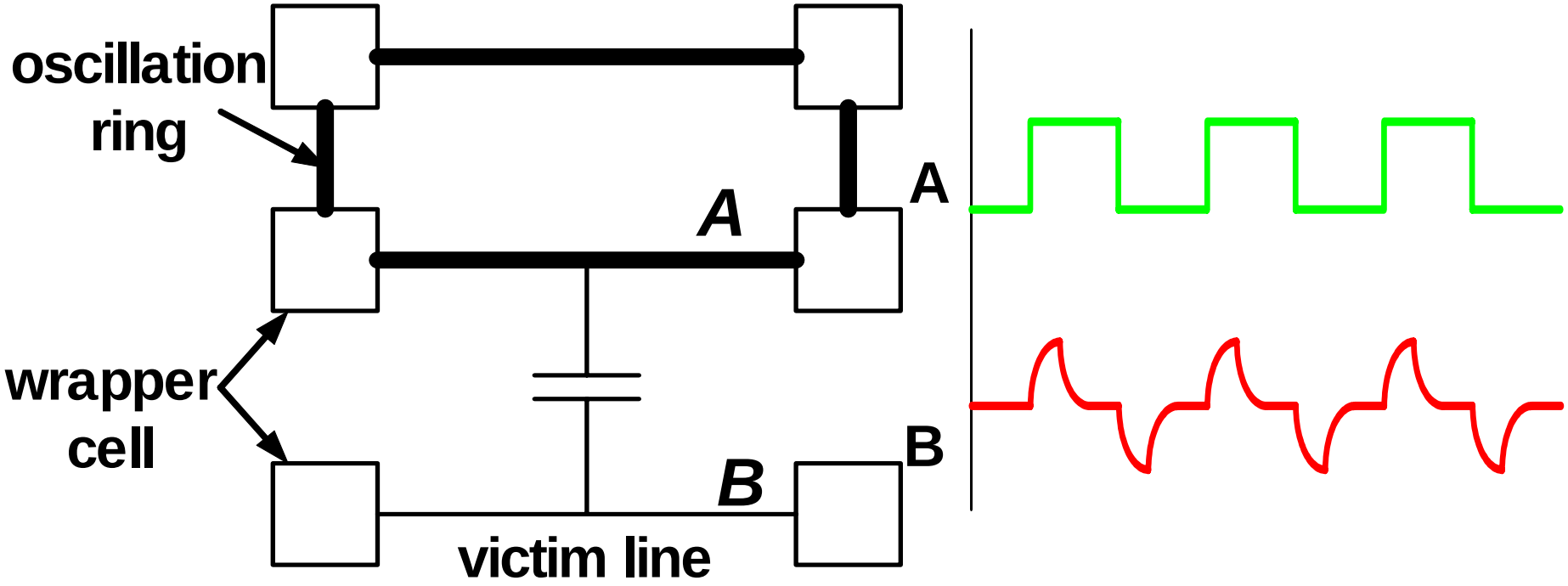
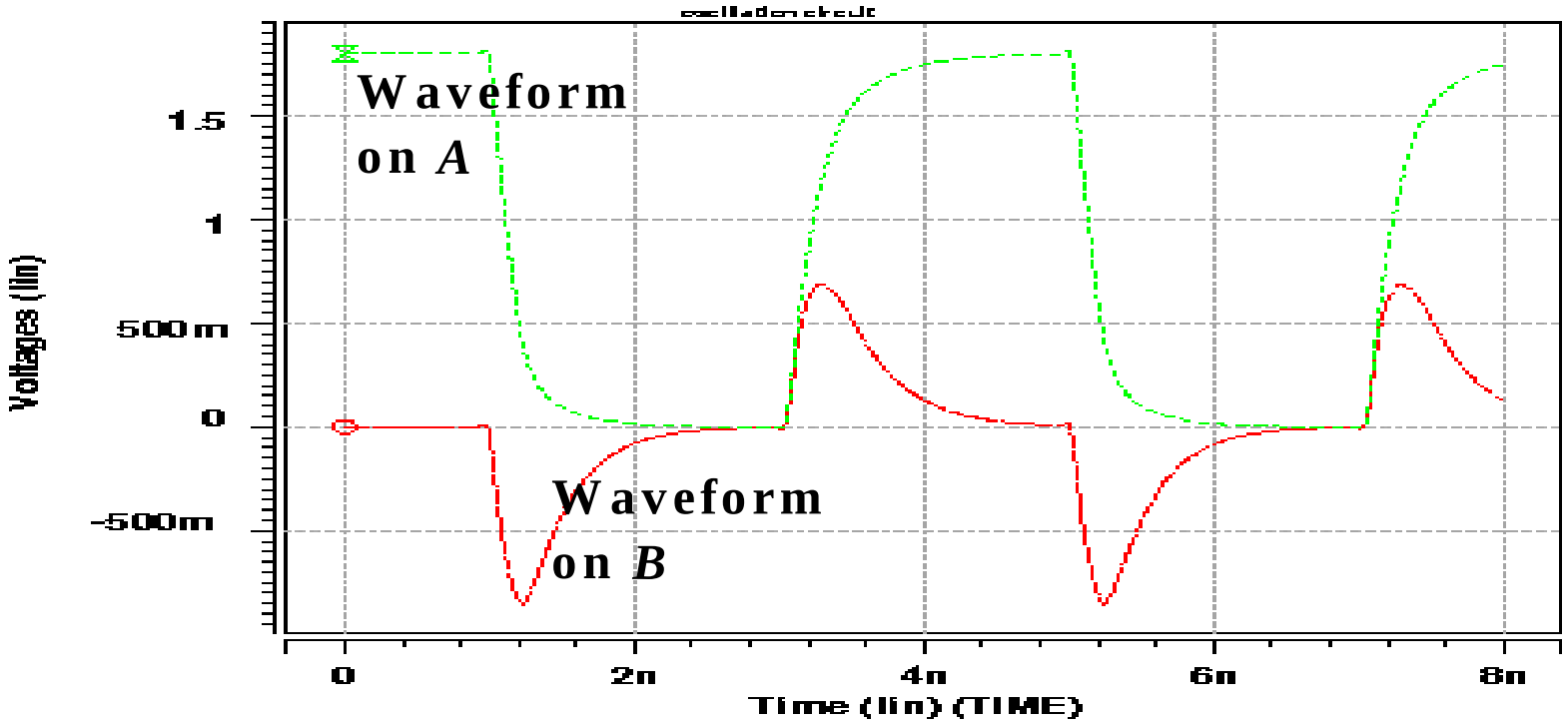
# Oscillation Ring for Interconnect Test (ORT)

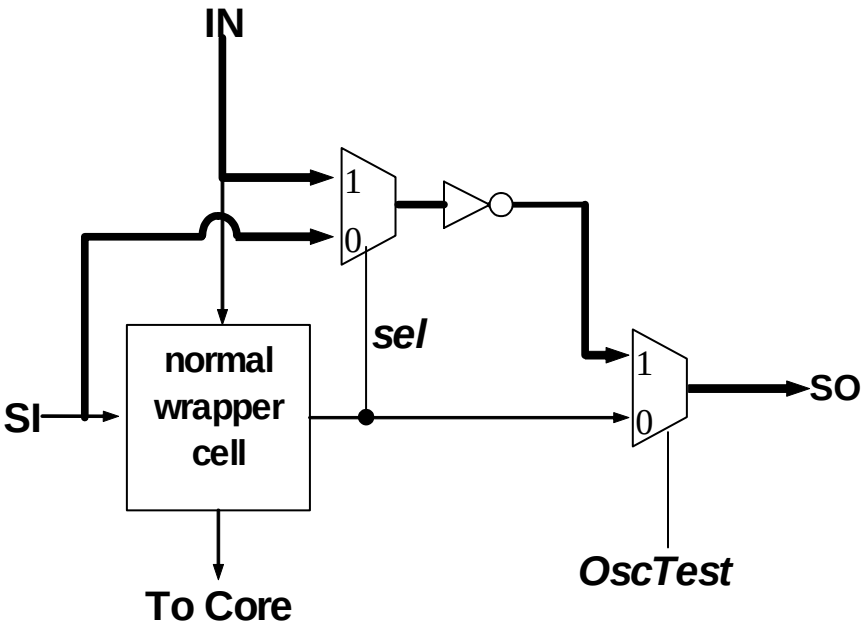


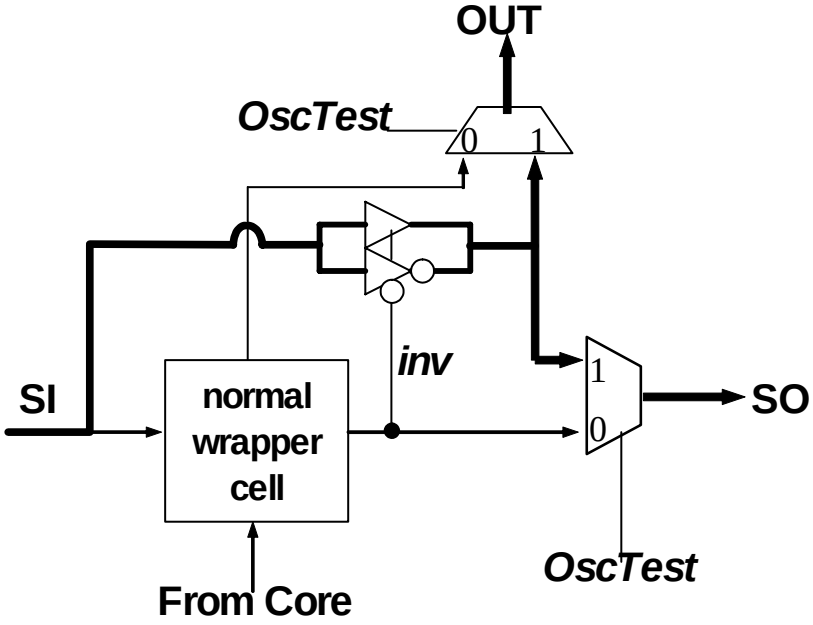

(a) (b)

# SPICE Simulation Waveforms



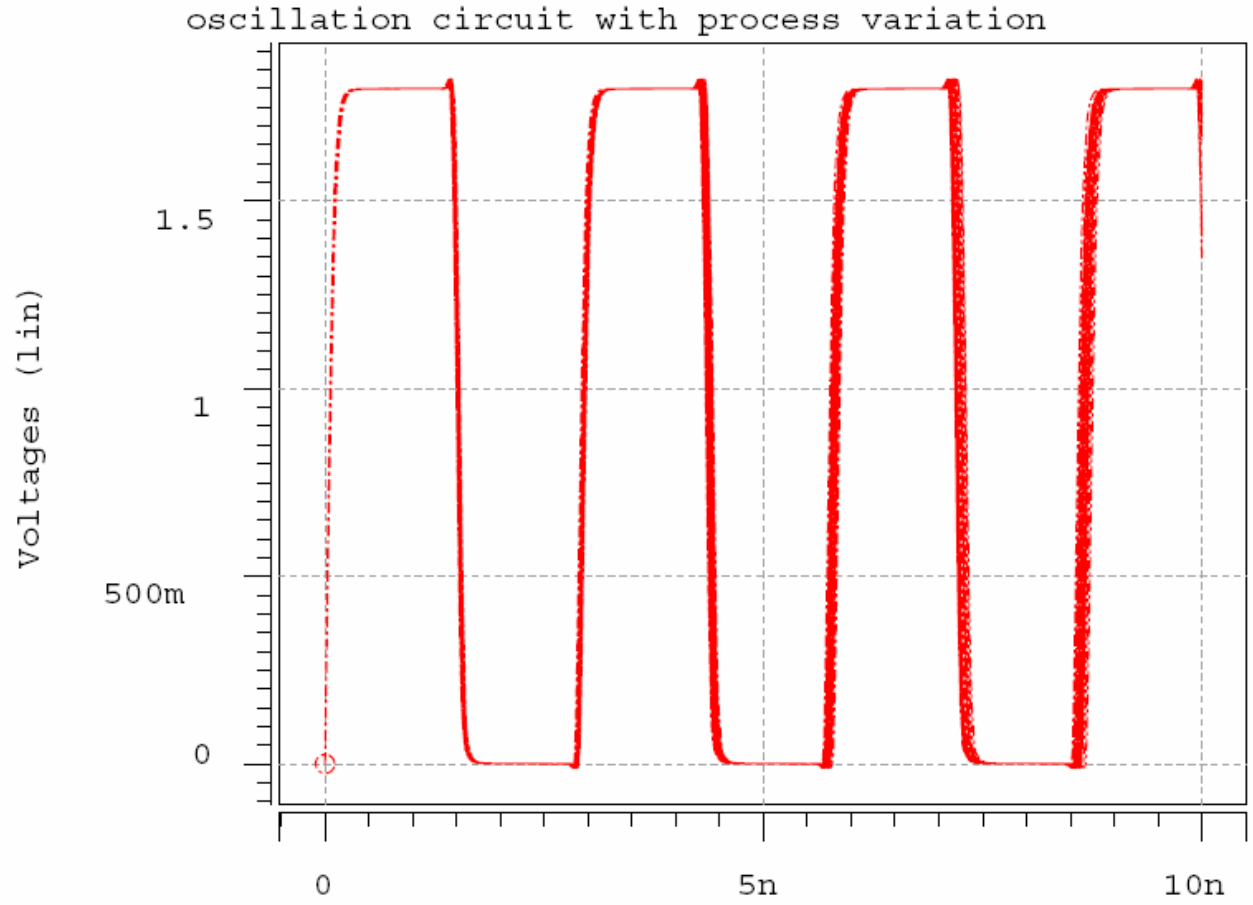
# P1500 Modified Wrapper Cells for SOC




**(a) Input Cell** **(b) Output Cell**

# Process Variation Effects on Oscillation Signals in Nanotechnology



# Interconnect Modeling

- **Interconnect Detection Model**
  - **Interconnect Model for Oscillation Ring Test (ORT)**
  - **2-pin nets**
- **Interconnect Diagnosis Model**
  - **Interconnect Model for Oscillation Ring Diagnosis (ORD)**
  - **Net segments**

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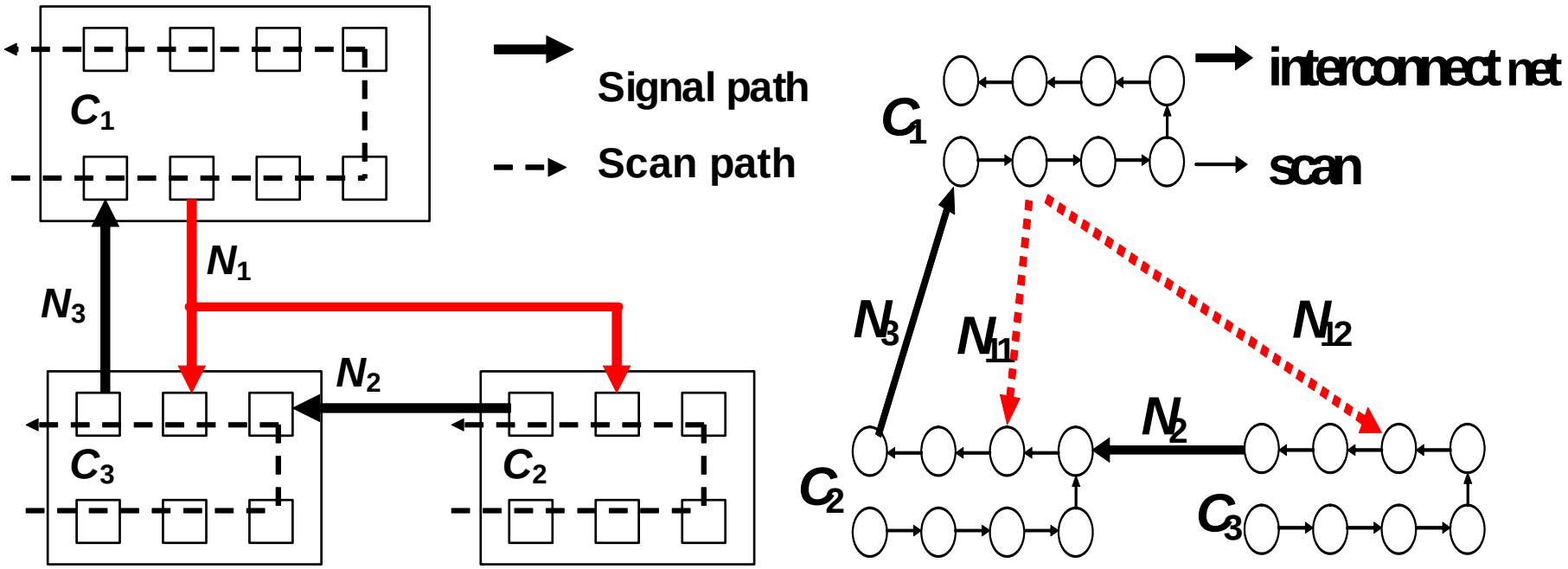
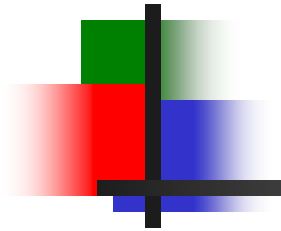
# Graph Model for Oscillation Ring Test




(a) Hypernets

(b) 2-pin nets



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  - **2-pin nets**
- **Interconnect Diagnosis Model**
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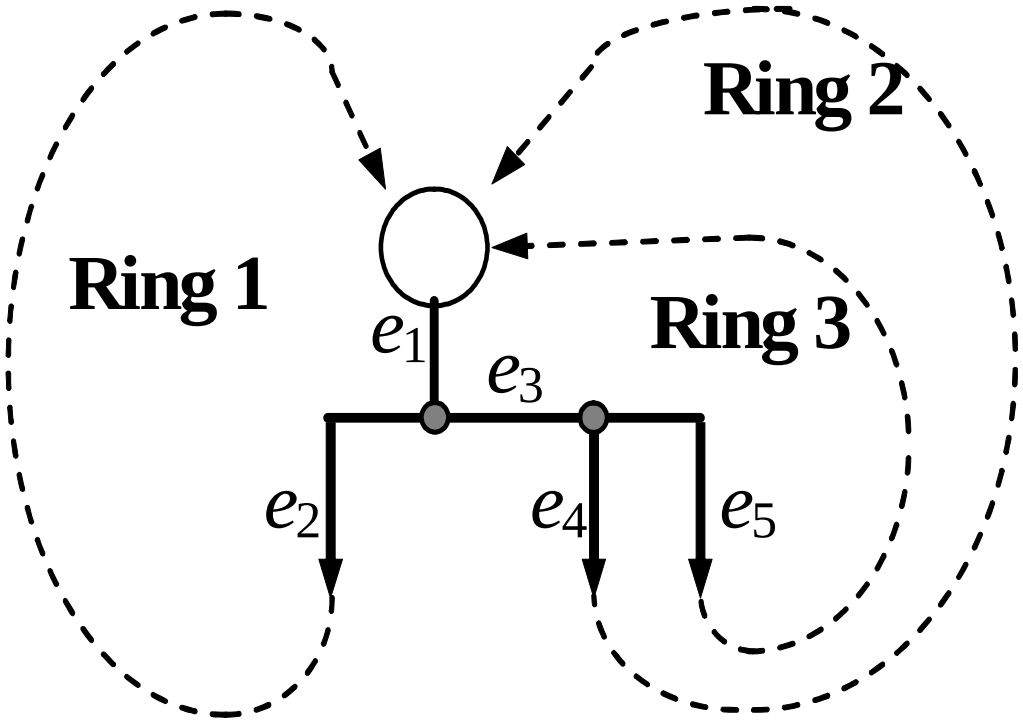
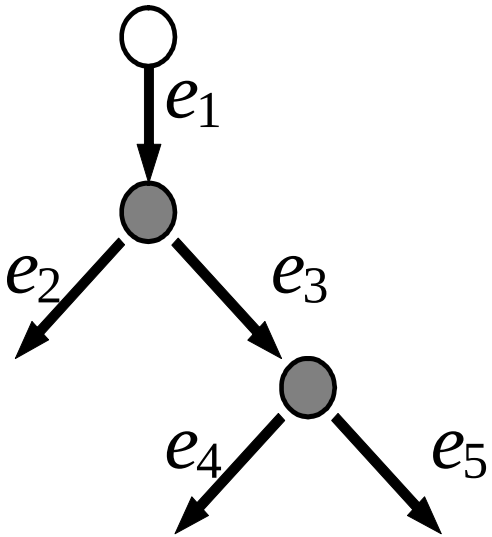
# Interconnect Diagnosis Model (ORD)

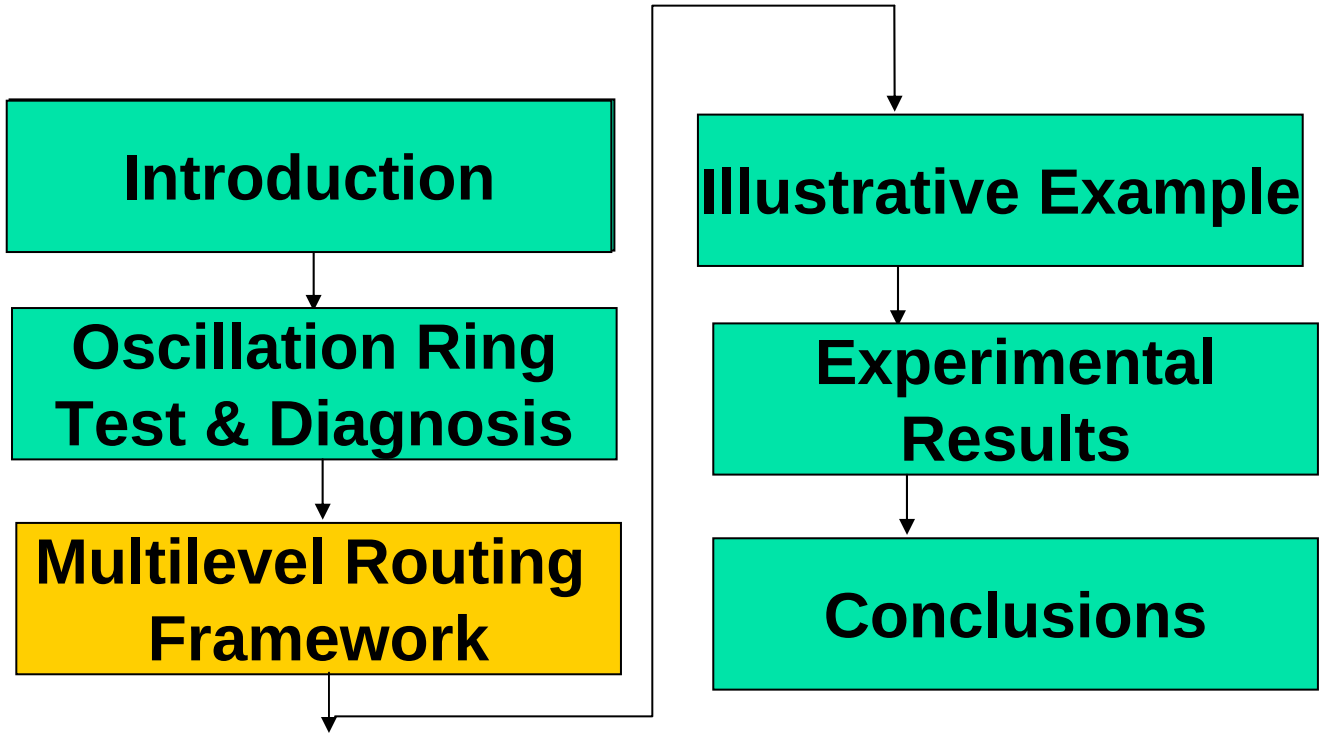



(a) Hypernets




(b) Interconnect Net Segments

# Outline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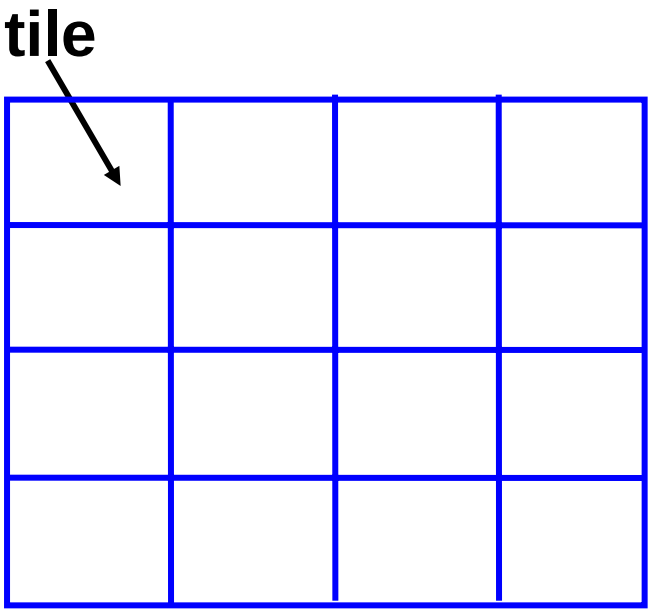
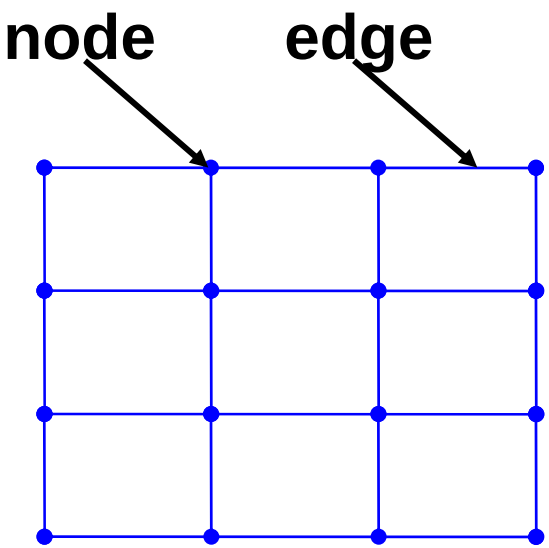
# Routing Model

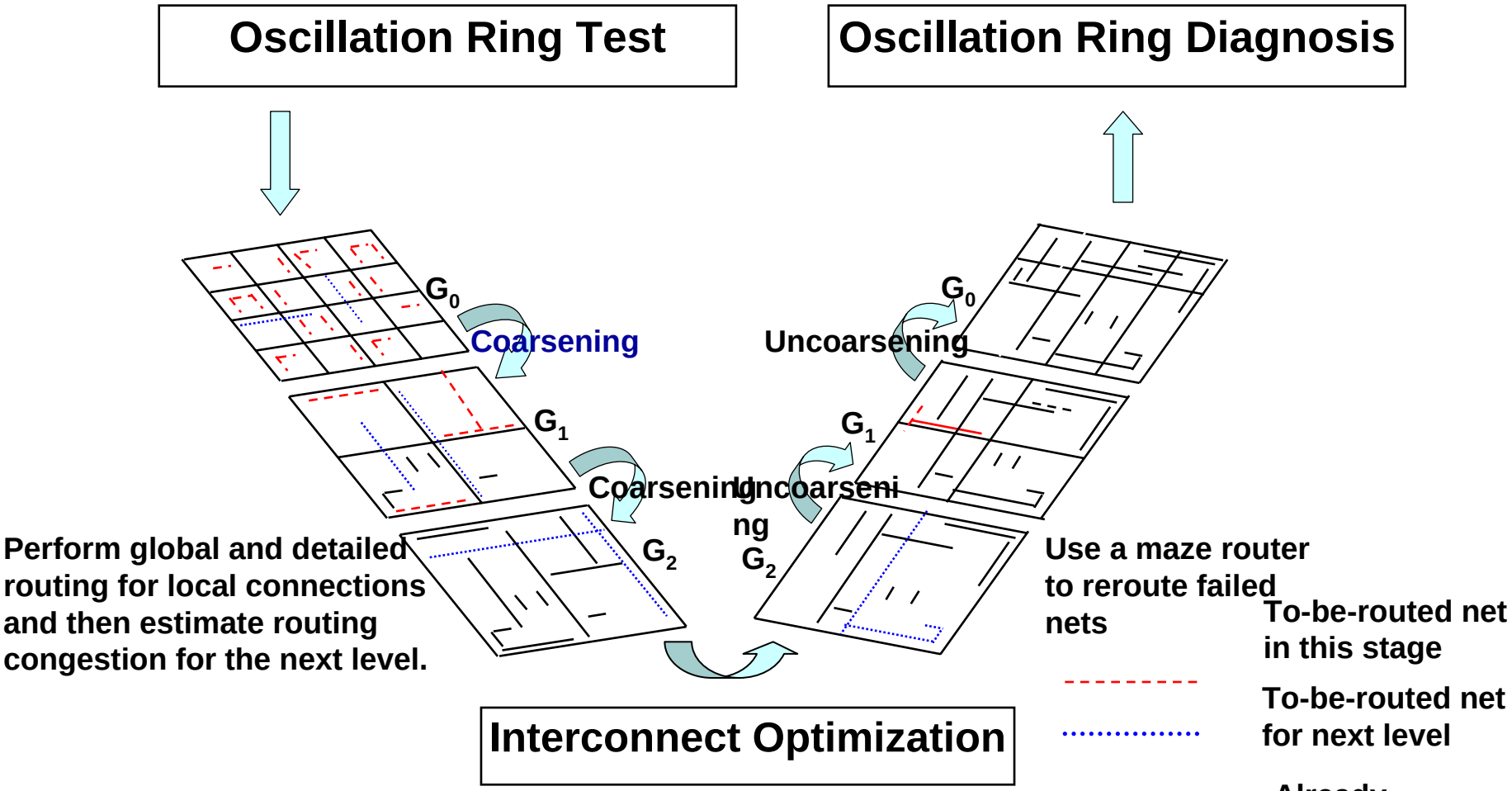



(a) Routing Plane

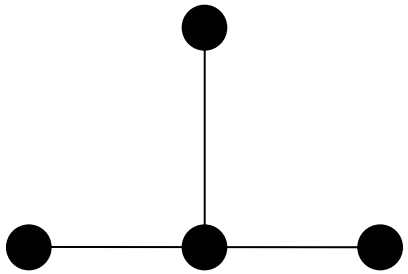



(b) Routing Graph Model

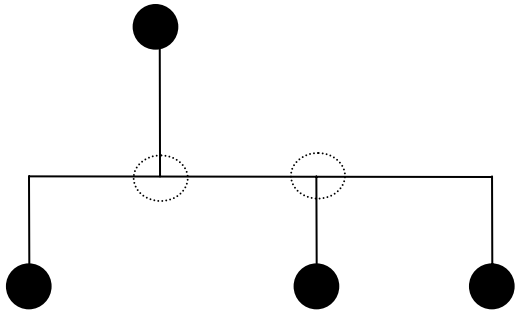
# Testability-Aware Integrated Multilevel Framework



# Diagnosability-Aware Routing Structure



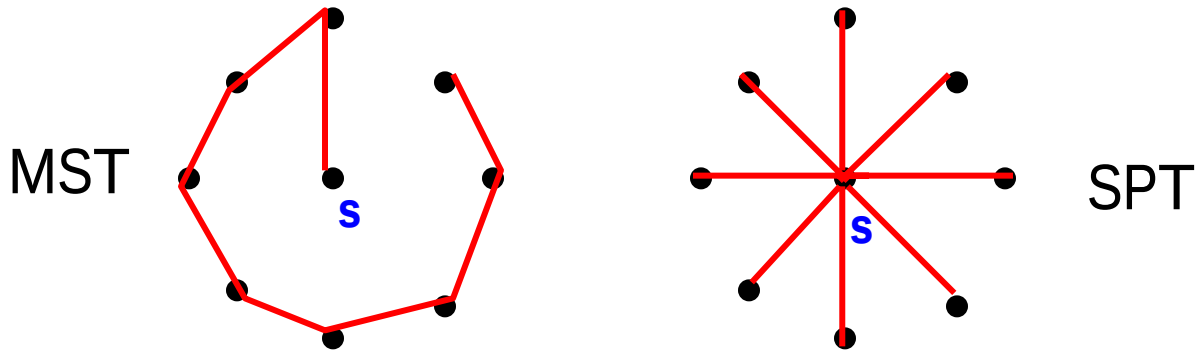
(a) Router Diagnosis Model: 3 nets



(b) Router Diagnosis Model based on Steiner Tree: 5 nets

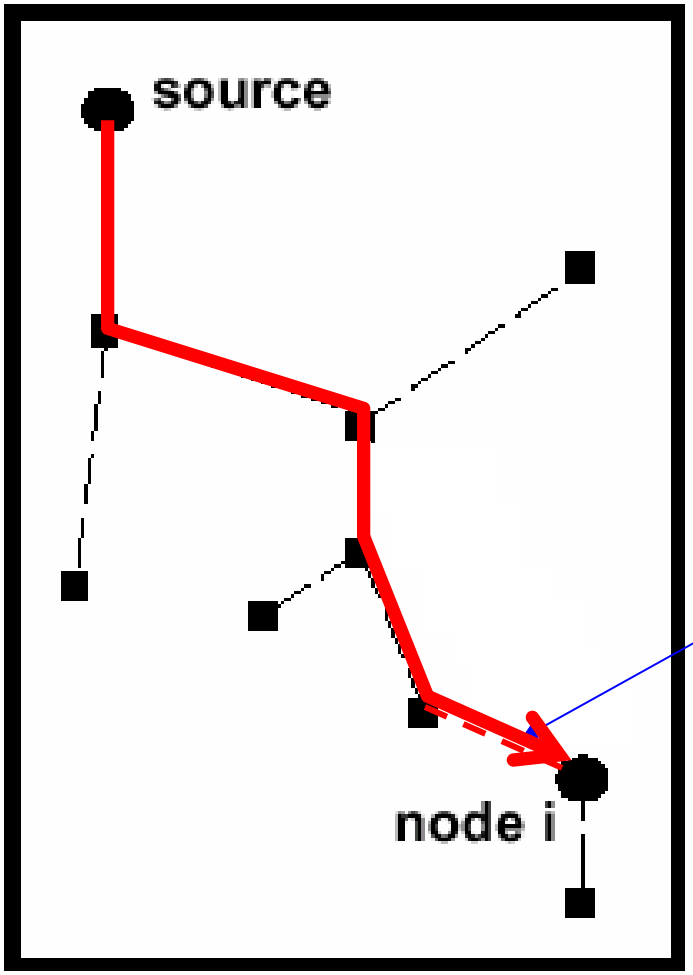
# MST vs. Shortest Path Tree

- **MST**
  - **Has the smallest** total wire length
  - **May incur longer** path length
- **Shortest path tree (SPT)**
  - **May incur larger** total wire length
  - **Has the shortest** path length
- **Simultaneously minimizing** total wire length **and** path length **reduces the Elmore delay of a tree.**



# Recalling Modification

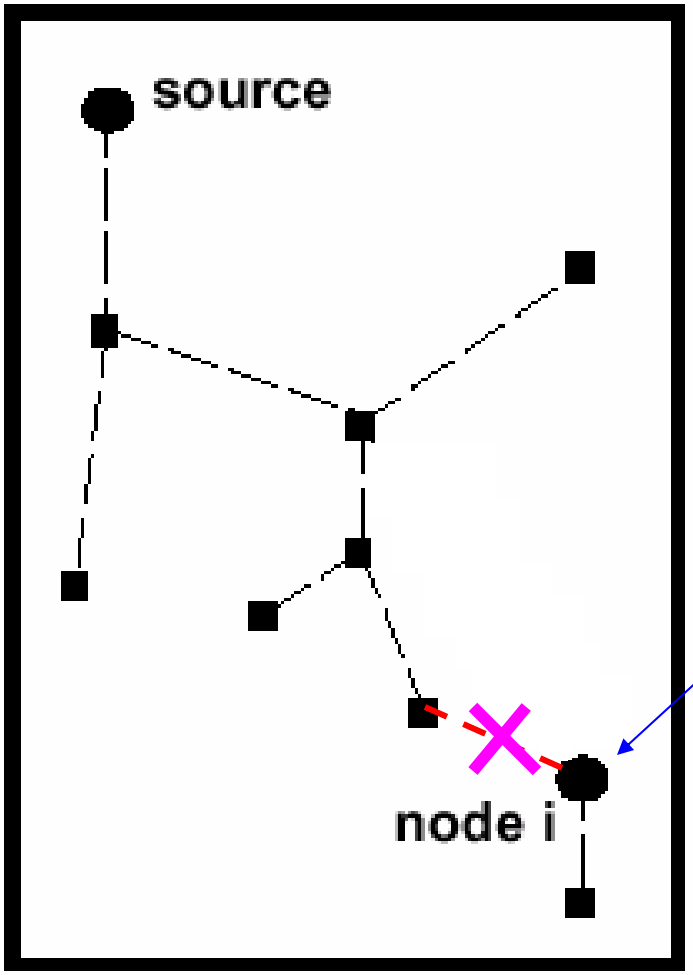
timing analysis




target connection

# Recalling Modification

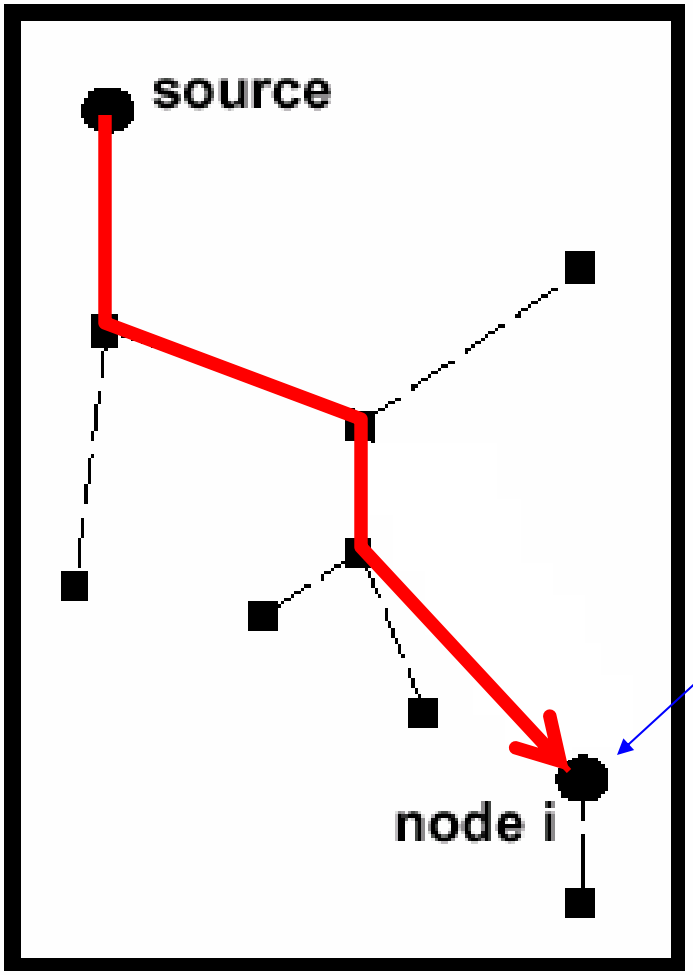
delete the connection




timing violation

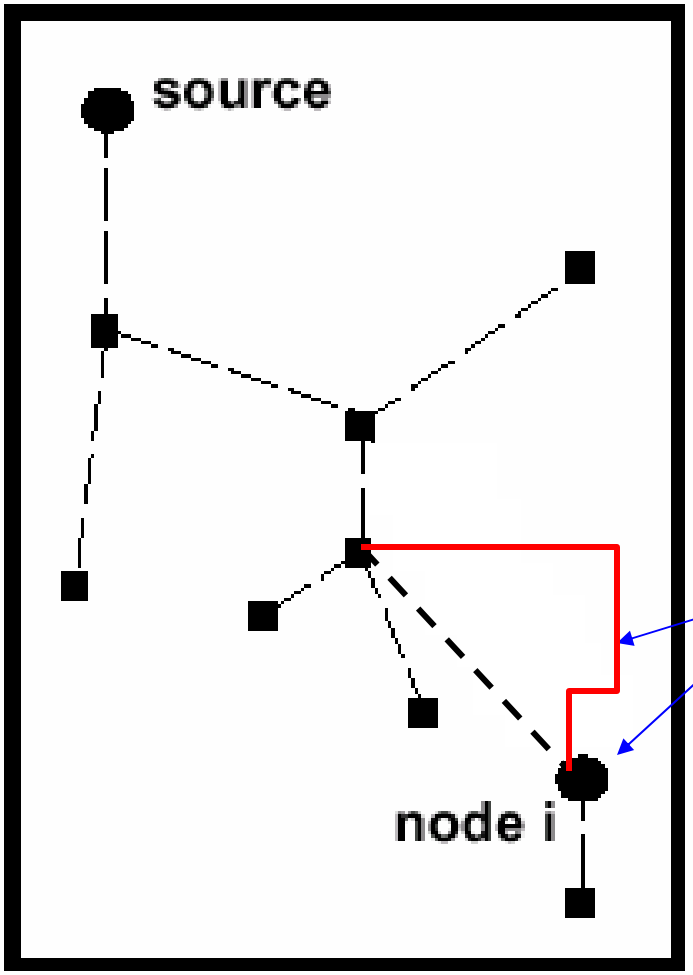
# Recalling Modification

timing analysis again




connect to a new parent

# Recalling Modification




perform routing

# MINCOUNT_Shortest Path Algorithm with $n(v)$ computation

```
MINCOUNT_SPA(G, dist, s)
1. Intialize_Source(G, s);
2. S ← ∅;
3. Q ← V[G];
4. while Q ≠ ∅
5.    u ← Extract_Min(Q);
6.    S ← S ∪ {u};
7.    for each v ∈ Adj[u]
8.       Count_Nodes(u, v, dist);
```

```
Count_Nodes(u, v, dist)
1. if d(v) ≥ d(u) + dist(u, v)
2.    d(v) ← d(v) + dist(u, v);
3.    if n(v) ≥ n(u) + node(u, v)
4.       n(v) ← n(u) + node(u, v);
5.       record u as the predecessor
routing region of v.
```



# Cost Metric for Routing Density Control

Cost Function in Uncoarsing Stage

$$\alpha(R_e) = \sum_{e \in R_e} c_e$$

$$c_e = \begin{cases} \dfrac{1}{2^{[(p_e/t)-d_e]}} & d_e < (p_e/t) \\ 1 & d_e \geq (p_e/t) \end{cases}$$

- $\alpha$: $E_i \rightarrow R$
- $R_e$
- $c_e$: congestion of edge
- $p_e$: capacity of nets
- $d_e$: number of nets

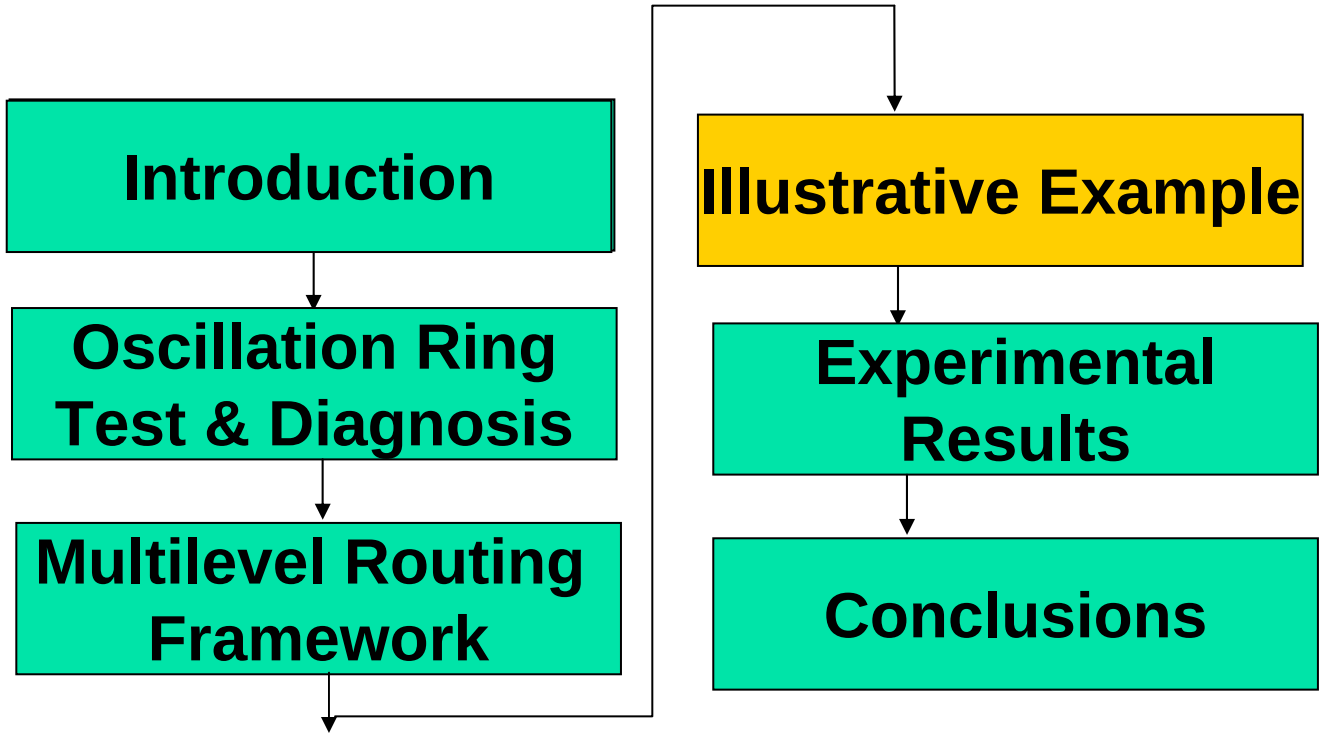
Cost Function in Coarsing Stage

$$\beta(R_e) = \sum_{e \in R_e} (a \cdot c_e + b \cdot o_e)$$

- $a$, $b$: user-defined parameters
- $o_e \in \{0,1\}$



# Outline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# An Illustrated Example

$$f_i = f \times \frac{n_i}{n}$$

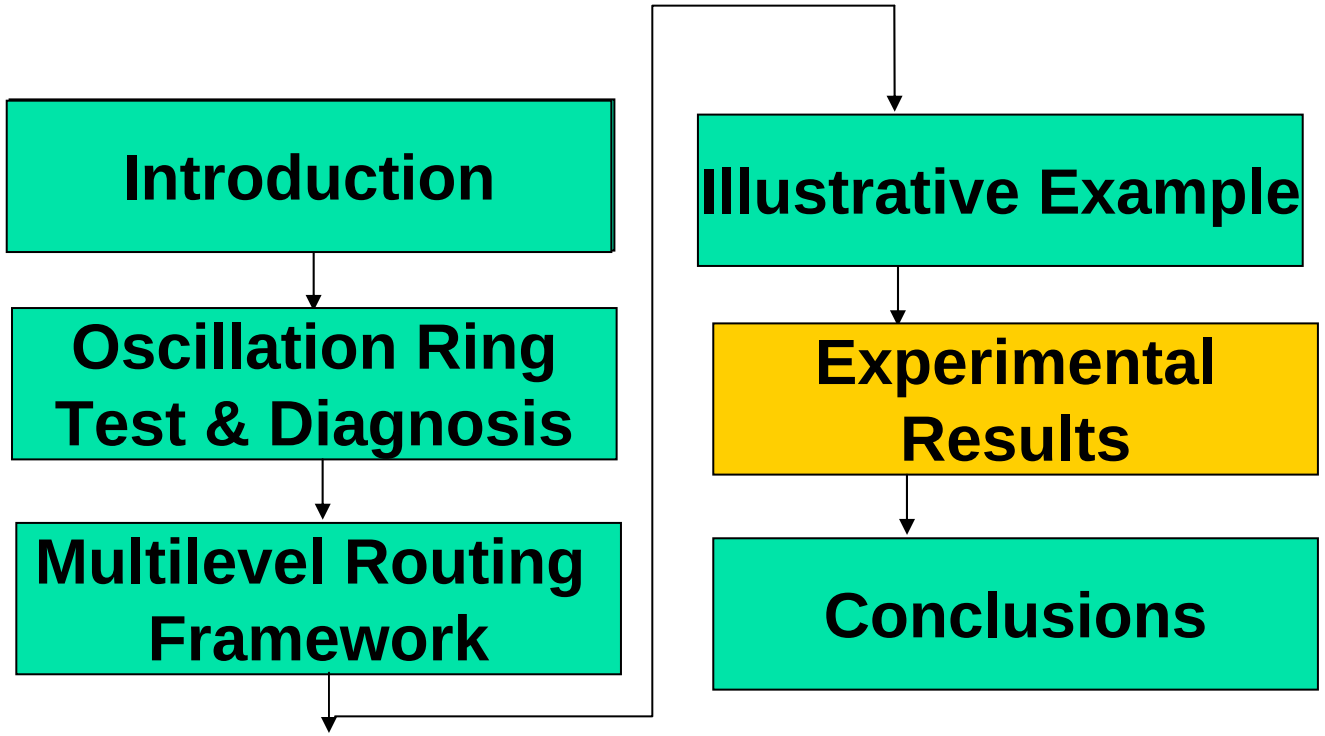
$$\varepsilon = \frac{1}{f_{\min} \times T_0} \leq \zeta$$

- $f_i$: frequency of the ith oscilaltion ring
- $n_i$: counter's content of the ith oscilaltion ring
- $\varepsilon$: counter's maximum measurement error
- $\xi$: delay measurement resolution

- Let 4 MHz$\leq f_i \leq$400 MHz, $f_{min}$= 4 MHz, $\xi$=0.001, thus, $n_i = 1/\xi$=1,000, we have $T_0$=250$\mu$s.



# Outline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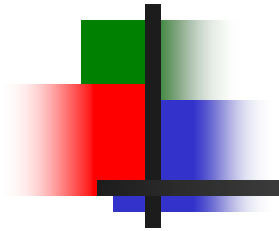


# Experimental Results

- **Testability enhancement of interconnect detection and diagnosis**
- **Congestion control for multi-objective optimization**



# Experimental Results for Testability Enhancement of Interconnect Detection and Diagnosis

by Katherine Shu-Min Li

| Circuit | Statistics | | | | #rings constructed for testability $\|R_t\|$ & diagnosis $\|R_d\|$ | |
|---|---|---|---|---|---|---|
| | #core | #pad | #hyp | #2-pin | $\|R_t\|$ | $\|R_d\|$ |
| ac3 | 27 | 75 | 211 | 416 | 133(33.3ms) | 374(93.5ms) |
| ami33 | 33 | 42 | 117 | 343 | 242(60.5ms) | 303(75.8ms) |
| ami49 | 49 | 22 | 361 | 475 | 156(39ms) | 386(96.5ms) |
| apte | 9 | 73 | 92 | 136 | 73(18.3ms) | 122(30.5ms) |
| hp | 11 | 45 | 72 | 195 | 81(20.3ms) | 164(41ms) |
| xerox | 10 | 2 | 161 | 356 | 218(54.5ms) | 342(85.5ms) |

# Experimental Results

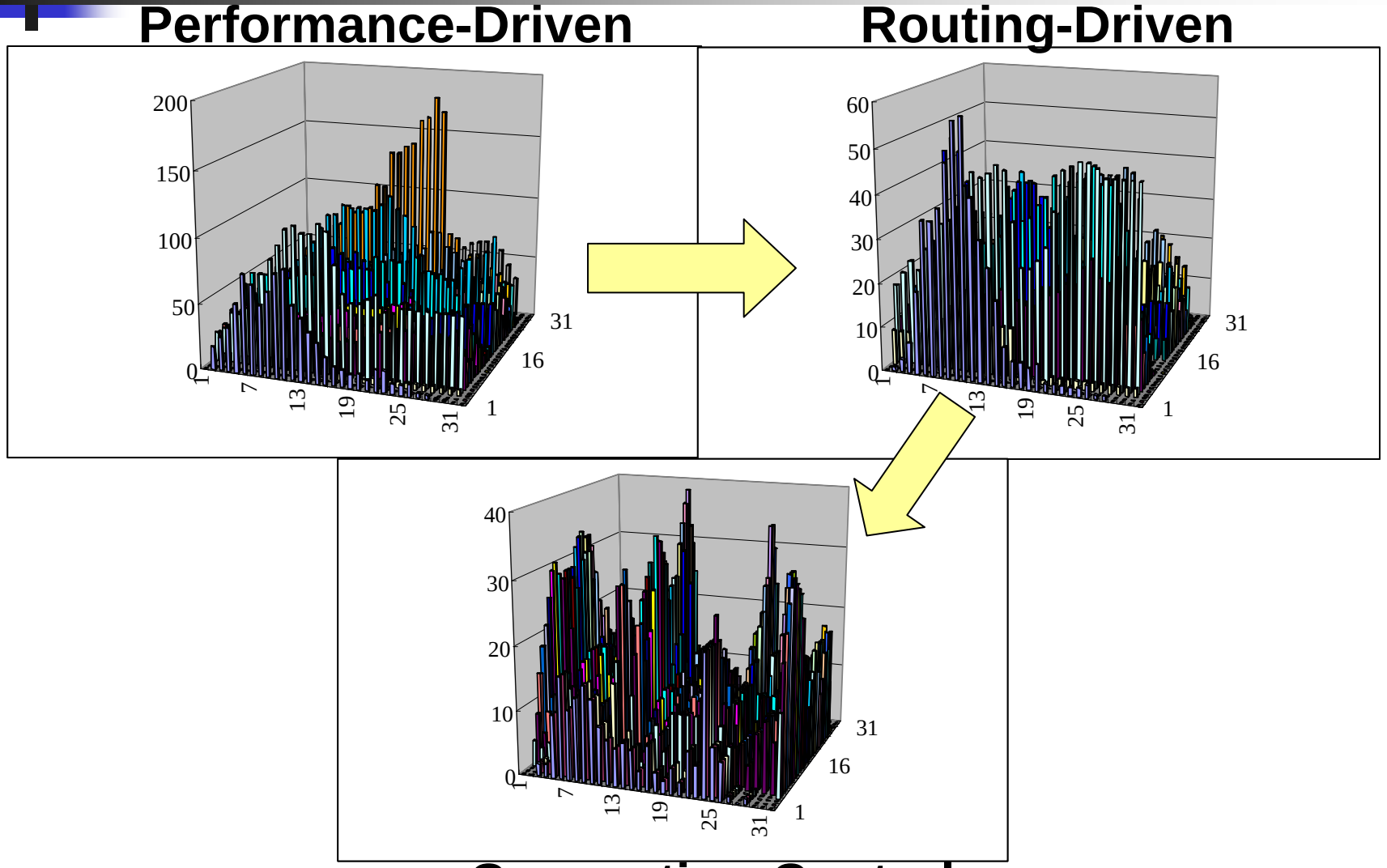
- Testability enhancement of interconnect detection and diagnosis
- Congestion control for multi-objective optimization

# Routing Benchmark Circuits

| Circuit | Size (mm) | #Layers | #Nets | #Pins |
|---|---|---|---|---|
| Mcc1 | 39000×45000 | 4 | 1694 | 3101 |
| Mcc2 | 152400×152400 | 4 | 7541 | 25024 |
| Struct | 4903x4904 | 3 | 3551 | 5717 |
| Primary1 | 7552x4988 | 3 | 2037 | 2941 |
| Primary2 | 10438x6468 | 3 | 8197 | 11226 |
| S5378 | 4330x2370 | 3 | 3124 | 4734 |
| S9234 | 4020x2230 | 3 | 2774 | 4185 |
| S13207 | 6590x3640 | 3 | 6995 | 10562 |
| S15850 | 7040x3880 | 3 | 8321 | 12566 |
| S38417 | 111430x6180 | 3 | 21035 | 32210 |
| S38584 | 12940x6710 | 3 | 28177 | 42589 |

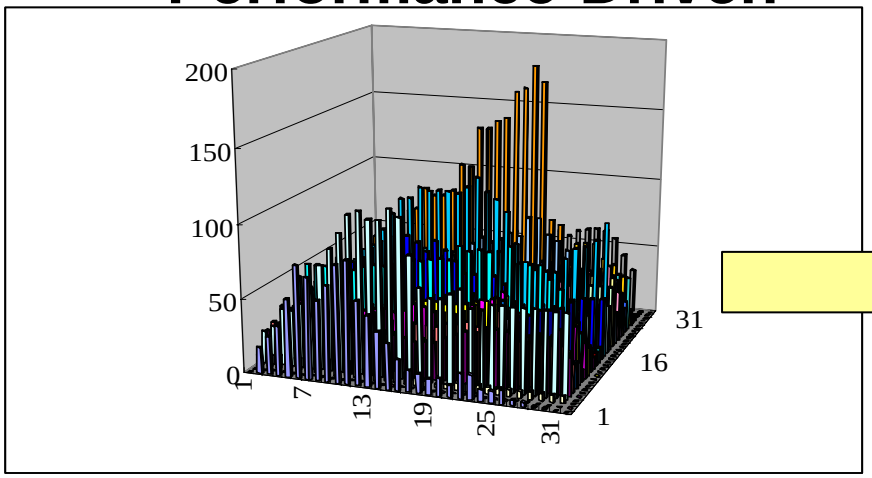


# Routing Density Distribution for MCC1 with Absolute Net Counts

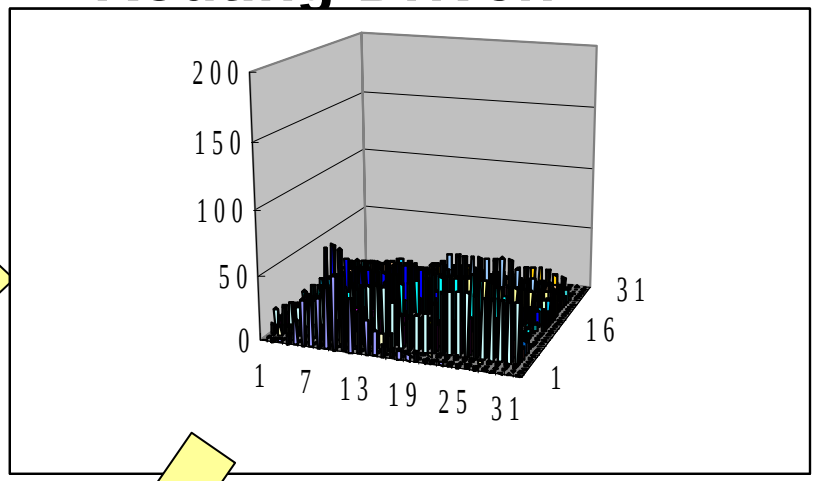


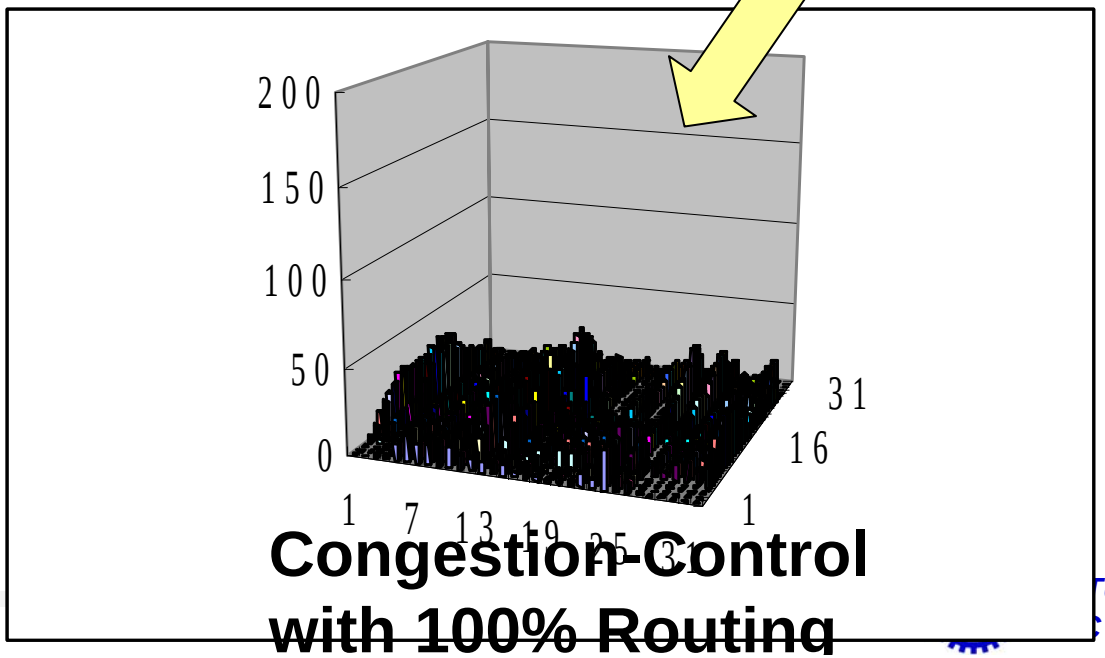
# Routing Density Distribution for MCC1 with Normalized Net Counts

**Performance-Driven**




**Routing-Driven**




**Congestion-Control with 100% Routing**

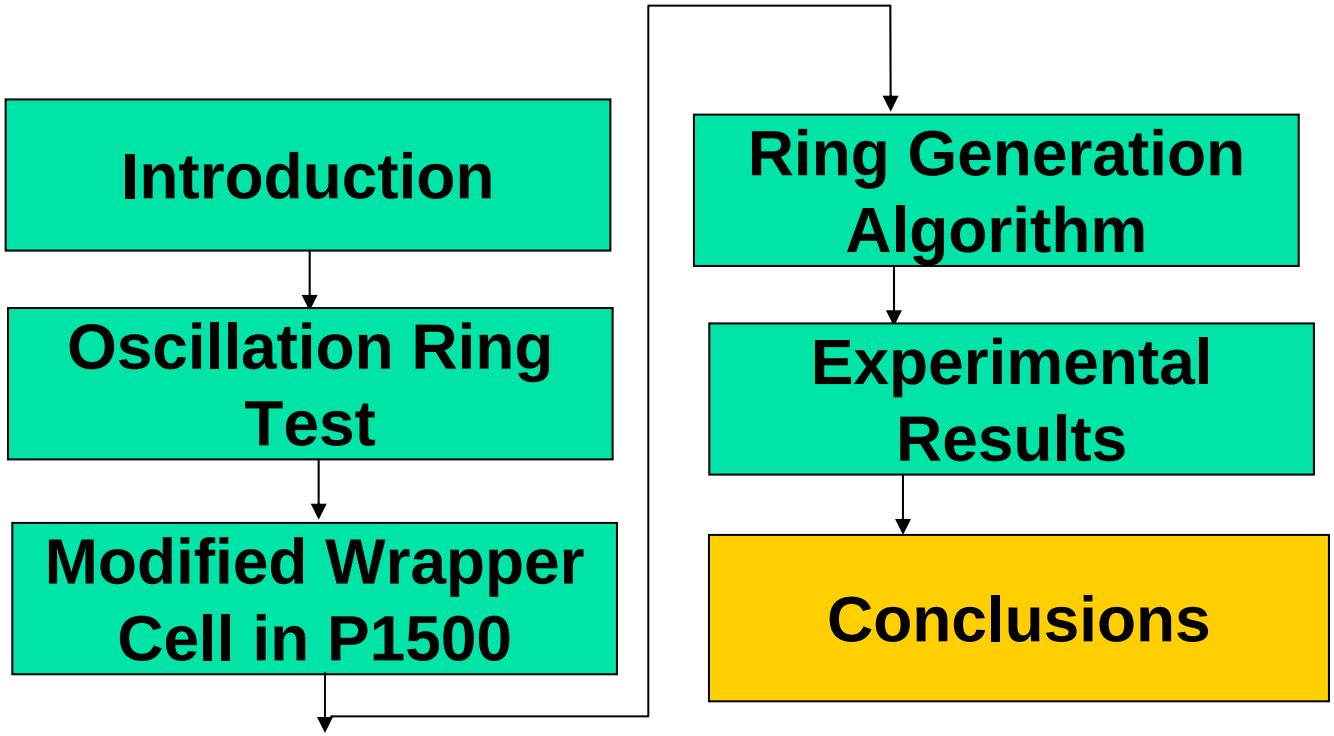
# Comparison of Maximum Density with both Maximum Delay and Average

| Circuit | (A) Performance-Driven [LIN] | | | | (B) Routability-Driven [LIN] | | | | (C) Proposed Balanced Density with 100% routability | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $d_{max}$ | $d_{avg}$ | #PEAK_Nets | CPU | $d_{max}$ | $d_{avg}$ | #PEAK_Nets | CPU | $d_{max}$ | $d_{avg}$ | #PEAK_Nets | CPU |
| Mcc1 | 5.E+07 | 1.E+07 | 181 | 223.68 | 2.03E+08 | 3.32E+07 | 61 | 77.11 | 2.03E+08 | 3.33E+07 | 45 | 72.63 |
| Mcc2 | 7.E+07 | 5.E+06 | 274 | 5964.2 | 8.46E+07 | 5.12E+06 | 135 | 2855.5 | 8.51E+07 | 5.11E+06 | 96 | 2592.34 |
| Struct | 1.E+06 | 7.E+04 | 32 | 307.91 | 1.52E+06 | 7.13E+04 | 9 | 56.33 | 1.52E+06 | 7.13E+04 | 7 | 56.53 |
| Primary 1 | 3.E+05 | 3.E+04 | 51 | 241.96 | 7.00E+05 | 5.51E+04 | 17 | 63.9 | 6.99E+05 | 5.50E+04 | 15 | 64.36 |
| Primary 2 | 4.E+06 | 2.E+05 | 91 | 1808.56 | 3.92E+06 | 2.09E+05 | 28 | 298.17 | 3.91E+06 | 2.09E+05 | 25 | 295.32 |
| S5378 | 9.E+04 | 6.E+03 | 49 | 23.28 | 8.91E+04 | 6.39E+03 | 17 | 4.13 | 8.94E+04 | 6.41E+03 | 15 | 4.29 |
| S9234 | 1.E+05 | 9.E+03 | 61 | 16.78 | 2.53E+05 | 1.19E+04 | 15 | 2.91 | 2.53E+05 | 1.19E+04 | 14 | 2.9 |
| S13207 | 4.E+05 | 2.E+04 | 114 | 65.45 | 4.64E+05 | 2.04E+04 | 30 | 14.44 | 4.64E+05 | 2.03E+04 | 27 | 14.57 |
| S15850 | 6.E+05 | 3.E+04 | 140 | 181.82 | 2.66E+06 | 6.68E+04 | 30 | 22.04 | 2.66E+06 | 6.67E+04 | 26 | 21.77 |
| S38417 | 5.E+05 | 3.E+04 | 272 | 741.53 | 8.52E+06 | 3.94E+05 | 27 | 50.02 | 8.52E+06 | 3.94E+05 | 23 | 50.08 |
| S38584 | 2.E+06 | 6.E+04 | 295 | 1453.8 | 1.76E+08 | 1.25E+07 | 31 | 127.8 | 1.76E+08 | 1.25E+07 | 29 | 122.5 |
| Comparison | 0.27 | 0.32 | 4.84 | 3.34 | 1.00 | 1.00 | 1.24 | 1.08 | 1 | 1 | 1 | 1 |

# Comparison of Routing Statistical Density

| Circuit | (A) Performance-Driven [LIN] | | | | (B) Routability-Driven [LIN] | | | | (C) Proposed Balanced Density with 100% routability | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | *#AvgNets_v* | *#AvgNets_h* | $\sigma_v$ | $\sigma_h$ | *#AvgNets_v* | *#AvgNets_h* | $\sigma_v$ | $\sigma_h$ | *#AvgNets_v* | *#AvgNets_h* | $\sigma_v$ | $\sigma_h$ |
| Mcc1 | 28.19 | 31.78 | 20.59 | 24.35 | 10.03 | 11.5 | 10.45 | 10.82 | 9.91 | 11.33 | 7.58 | 7.33 |
| Mcc2 | 39.35 | 44.05 | 37.26 | 46.98 | 19.39 | 21.65 | 23.53 | 25.8 | 18.74 | 20.88 | 17.3 | 18.54 |
| Struct | 4.97 | 4.86 | 4.62 | 5.03 | 1.42 | 1.41 | 1.24 | 1.67 | 1.42 | 1.41 | 1.07 | 1.59 |
| Primary1 | 2.29 | 1.74 | 3 | 5.67 | 0.7 | 0.6 | 1.05 | 1.95 | 0.7 | 0.6 | 1.2 | 1.8 |
| Primary2 | 7.22 | 7.49 | 5.56 | 18.23 | 2.05 | 1.85 | 1.59 | 4.57 | 2.05 | 1.85 | 1.56 | 4.45 |
| S5378 | 12.53 | 13.46 | 9.16 | 8.4 | 4.38 | 3.44 | 3.45 | 2.13 | 4.4 | 3.46 | 3.44 | 2.1 |
| S9234 | 14.16 | 9.99 | 12.91 | 7.04 | 3.95 | 2.56 | 3.25 | 1.62 | 3.95 | 2.56 | 3.24 | 1.6 |
| S13207 | 28.43 | 20.49 | 18.4 | 11.08 | 9.3 | 5.93 | 5.77 | 2.76 | 9.29 | 5.92 | 5.23 | 2.81 |
| S15850 | 36.61 | 34.48 | 23.89 | 20.42 | 10.29 | 7.41 | 5.63 | 2.92 | 10.31 | 7.41 | 5.39 | 2.91 |
| S38417 | 44.58 | 27.38 | 37.36 | 27.94 | 7.31 | 4.27 | 4.75 | 2.17 | 7.3 | 4.27 | 4.44 | 2.18 |
| S38584 | 43.99 | 30.53 | 35.93 | 20.12 | 9.06 | 5.8 | 5.74 | 2.86 | 9.05 | 5.79 | 5.43 | 2.88 |
| Comparison | 3.40 | 3.46 | 3.73 | 4.05 | 1.01 | 1.01 | 1.19 | 1.23 | 1 | 1 | 1 | 1 |

# Outline


Introduction
Oscillation Ring Test
Modified Wrapper Cell in P1500
Ring Generation Algorithm
Experimental Results
Conclusions

# Conclusion

- **Present an effective multilevel routing framework**
  - **Embedded OR Scheme to form prerouting and postrouting stage**
    - Show that the embedded oscillation ring test and diagnosis scheme is feasible based on the simulation results with TSMC .18 μm process technology
    - OR scheme achieves 100% fault detection coverage and maximal diagnosability for testing interconnects in SoC
  - **Congestion Control in bottom-up and top-down two stages**
    - Apply a congestion-driven routing algorithm to reduce the multiple-fault probability, CMP and OPC induced effects, and crosstalk effects for yield enhancement



# Thank you!