



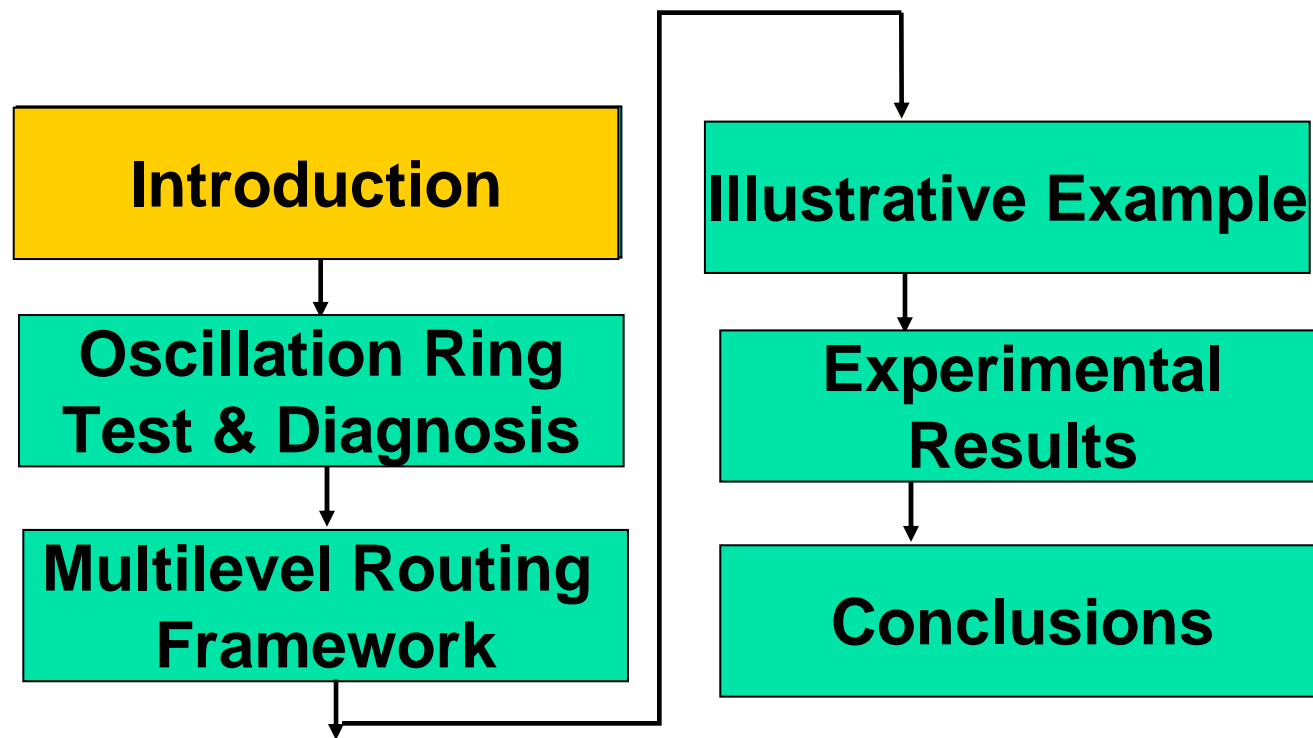
# **Multilevel Full-Chip Routing with Testability and Yield Enhancement**

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***Katherine Shu-Min Li, Chung-Len Lee, Yao-Wen Chang\*,  
Chauchin Su and J. E Chen\*\****

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University\*, National Central University\*\****

# Outline



# Introduction

- **Interconnect plays a dominant role in deep submicron era**
  - **determines circuit performance and signal integrity**
    - **Delay Fault**
    - **Crosstalk Glitch Fault**
- **Interconnect Test**
  - **Board-level**
  - **System-level**

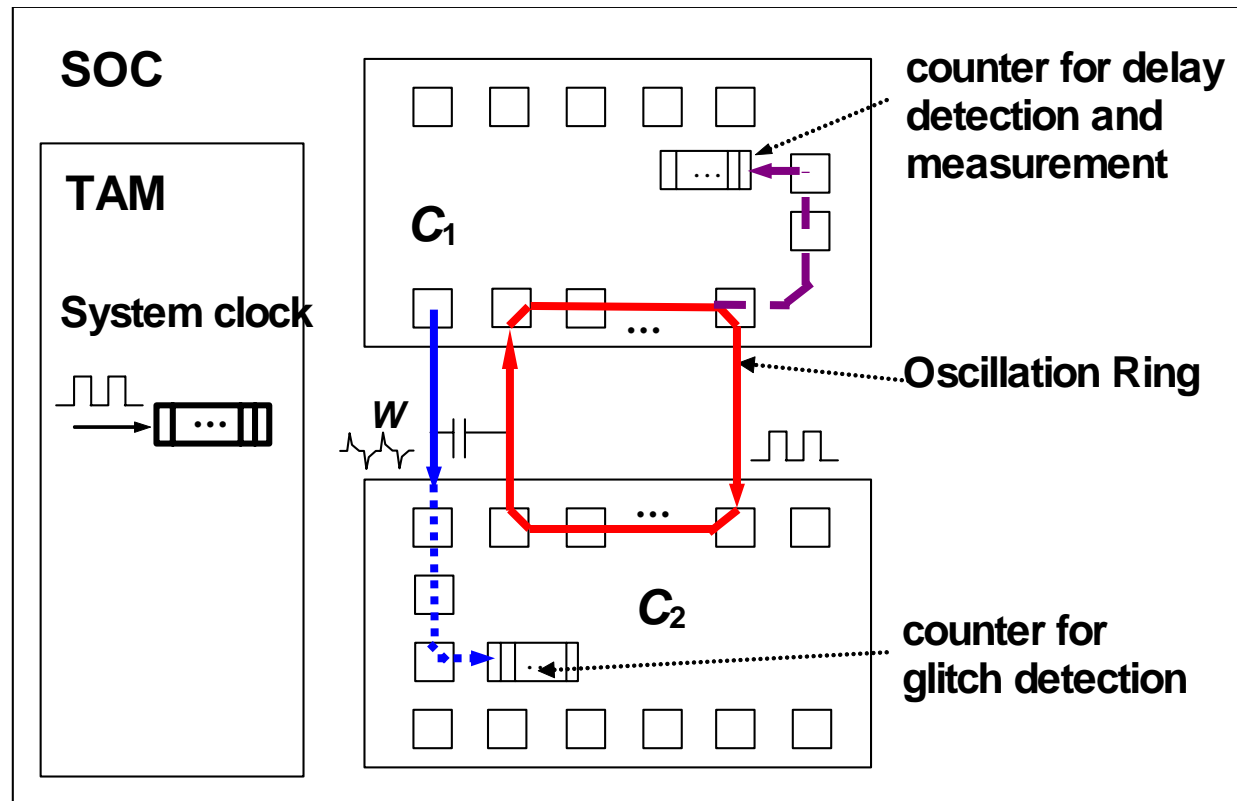
# Introduction (Cont'd)

- **IEEE P1500 standards**
  - provide structural support for core testing and interconnect testing in SoC
- **Our Proposed Oscillation Ring (OR) Test Architecture**
  - detects stuck-at and open, also delay and crosstalk glitch
  - measures delay period

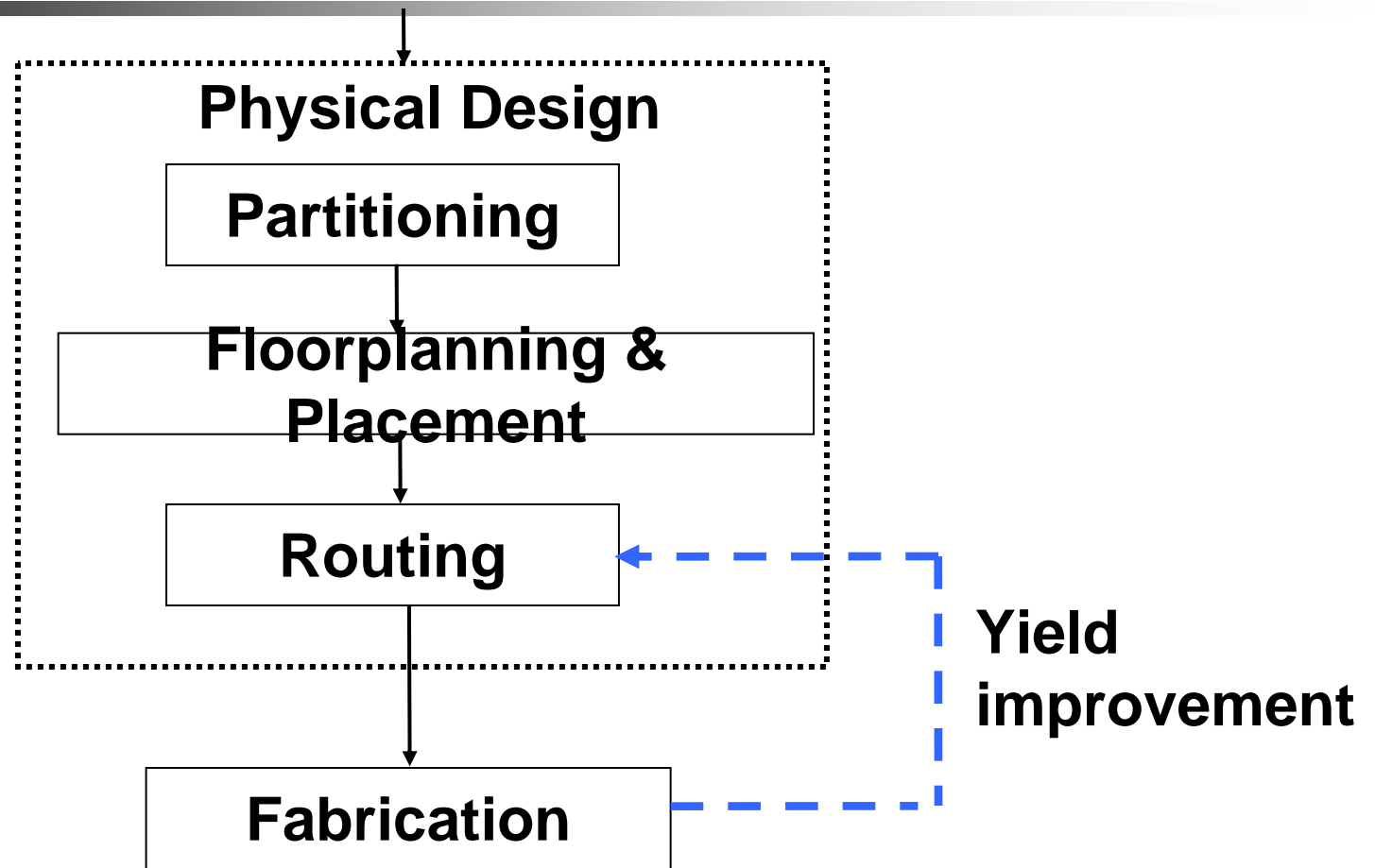
# Two Motivations

- **Testability Enhancement:**
  - **Propose integrated multilevel routing framework with embedded oscillation ring (OR) test architecture**
    - to detect stuck-at and open, also delay and crosstalk glitch
    - to measure delay period
- **Yield Enhancement:**
  - **Propose Congestion-Control guided routing**

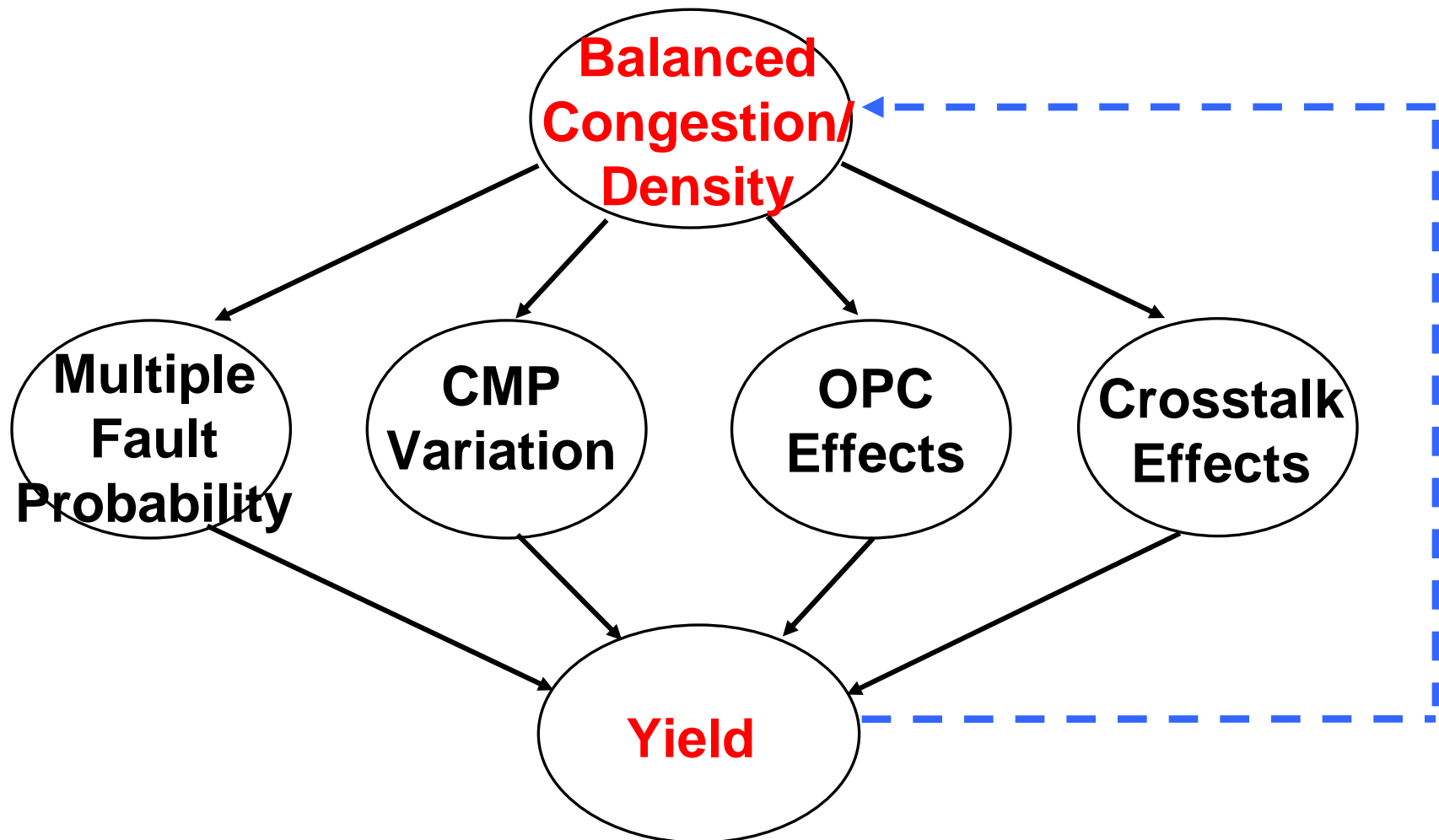
# Motivation for Testability Enhancement: OR Test Architecture for Interconnect (1/2)



# Motivation for Yield Improvement (2/2)



# Motivation for Yield Improvement (Cont'd)



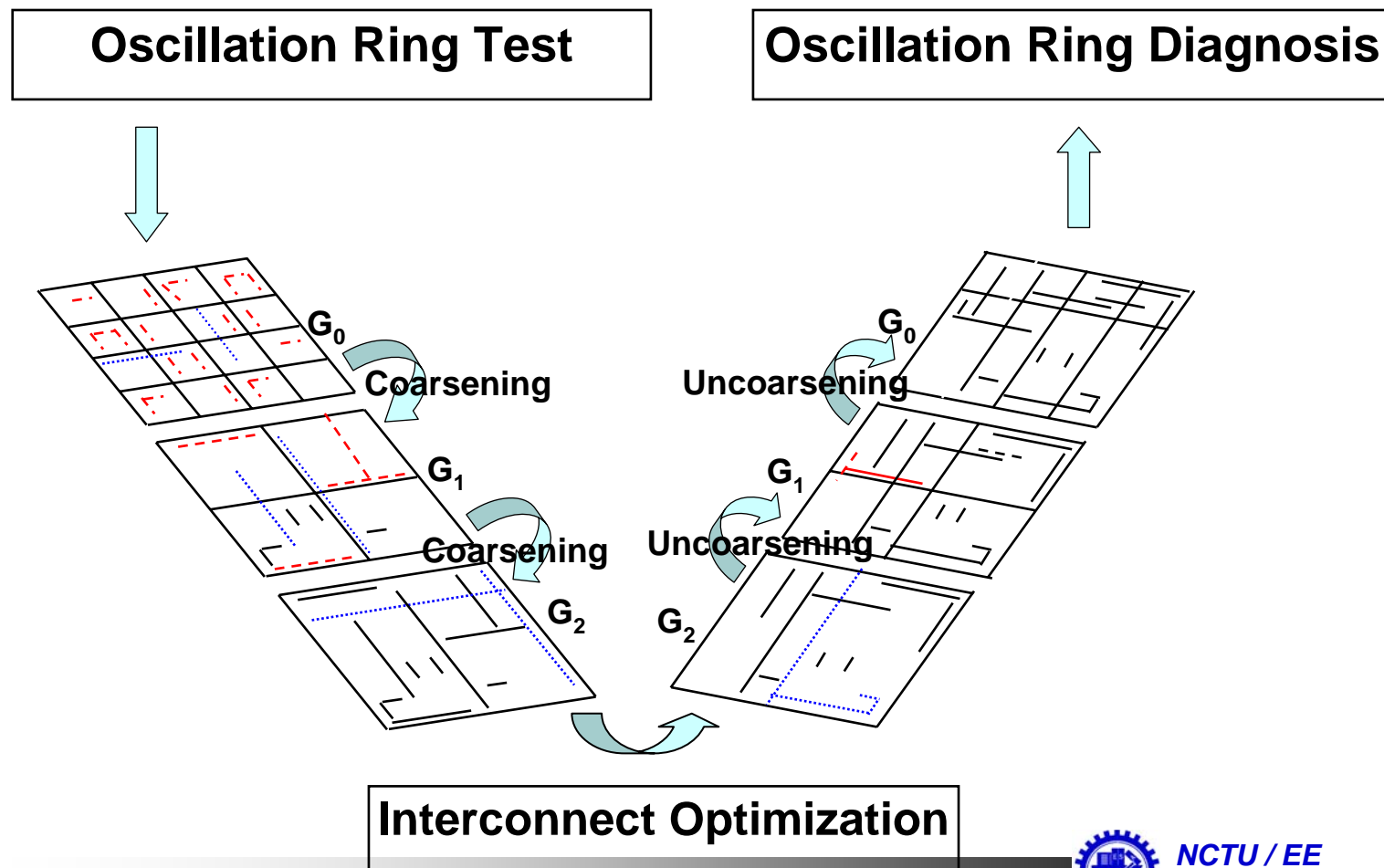
# Our Work

- **Consider testability and diagnosability, manufacturability, and signal integrity simultaneously in the multilevel routing framework.**
- **Provide testability and yield enhancement solutions in the routing stage to both diagnose interconnects and improve density flexibility**
- **Present heuristics to balance and reduce congestion in routing for yield improvement**

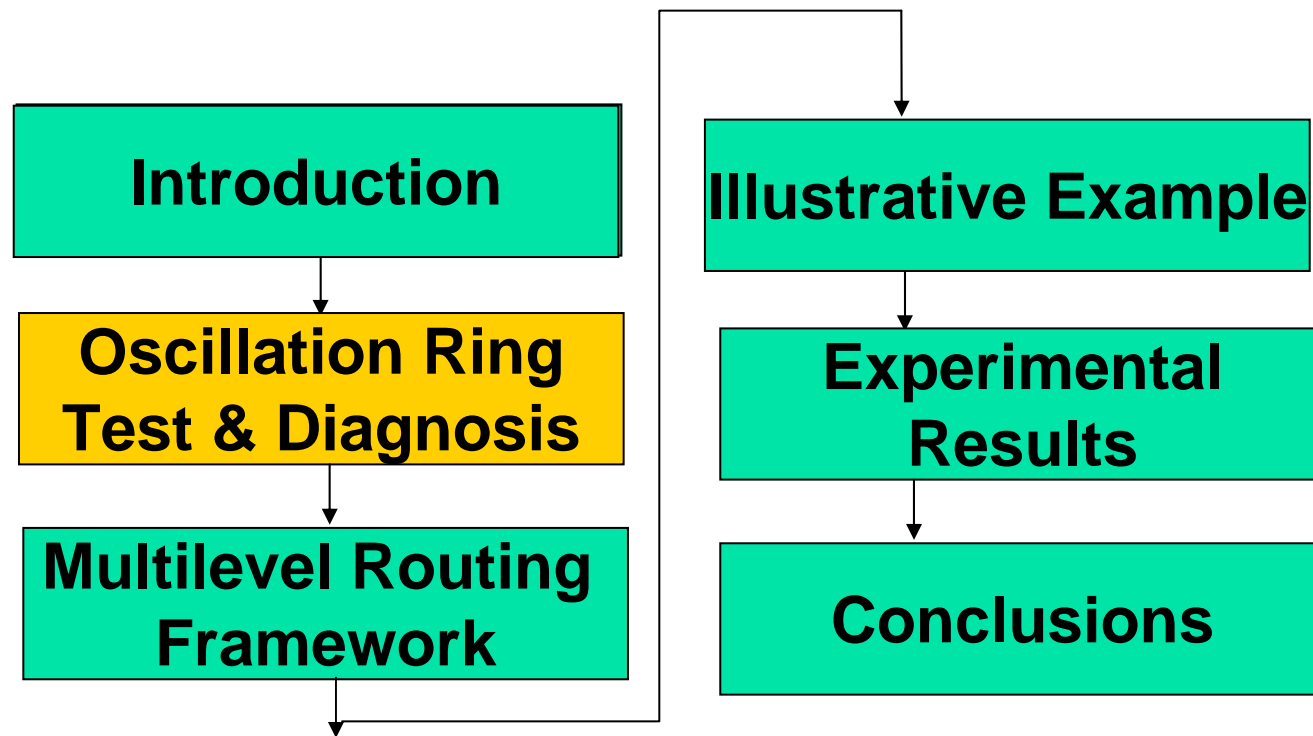


# Our Work (Cont'd)

- Propose a new testability-driven multilevel routing framework:

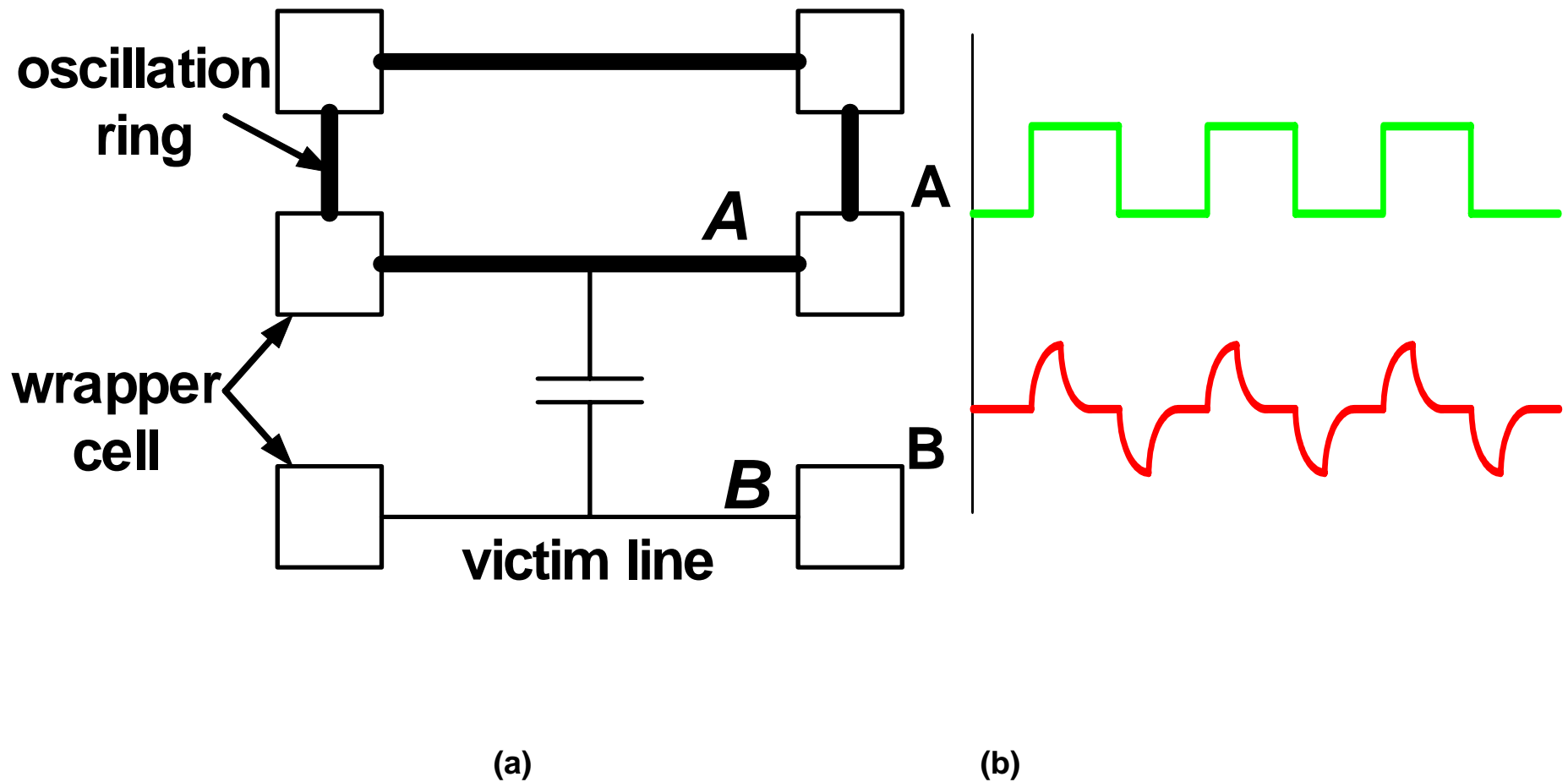


# Outline

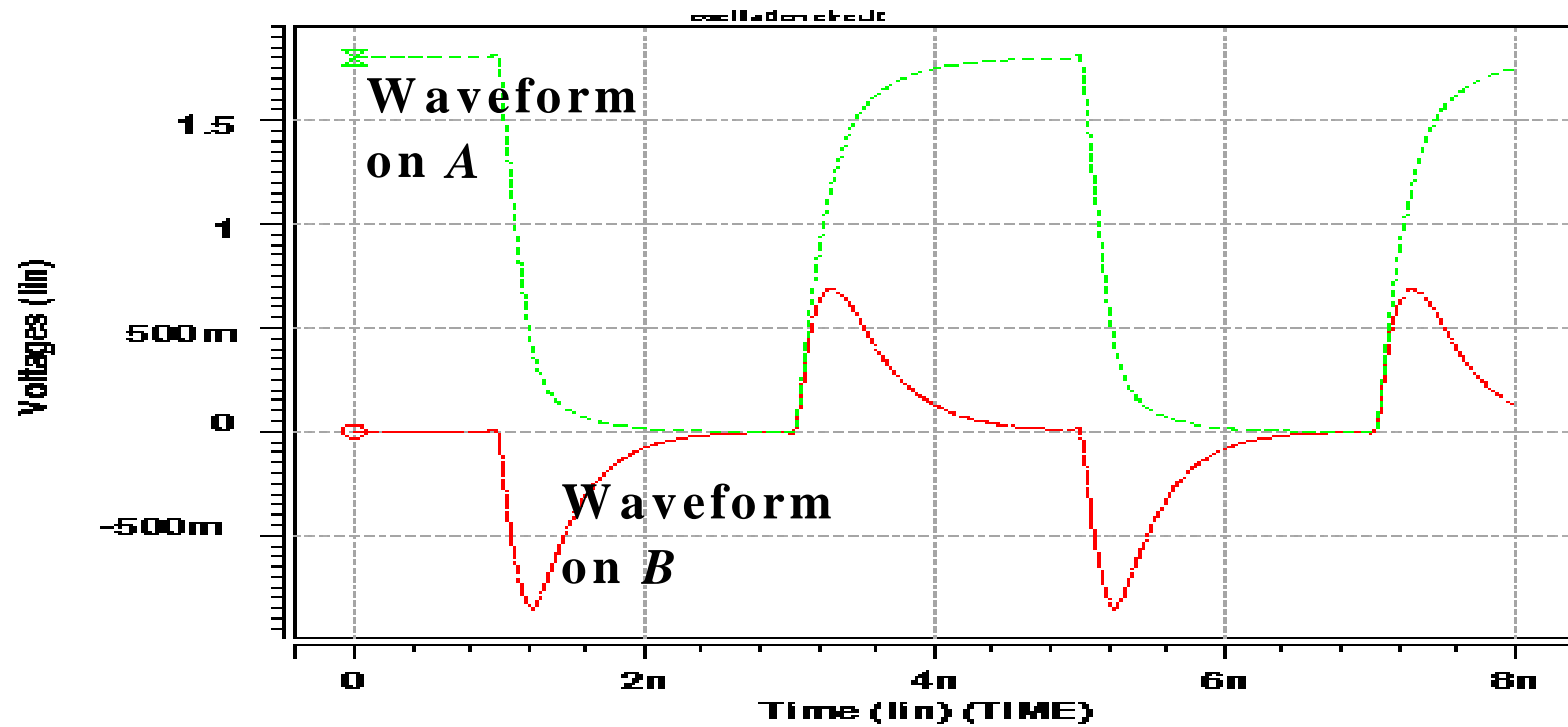


# Oscillation Ring for Interconnect Test (ORT)

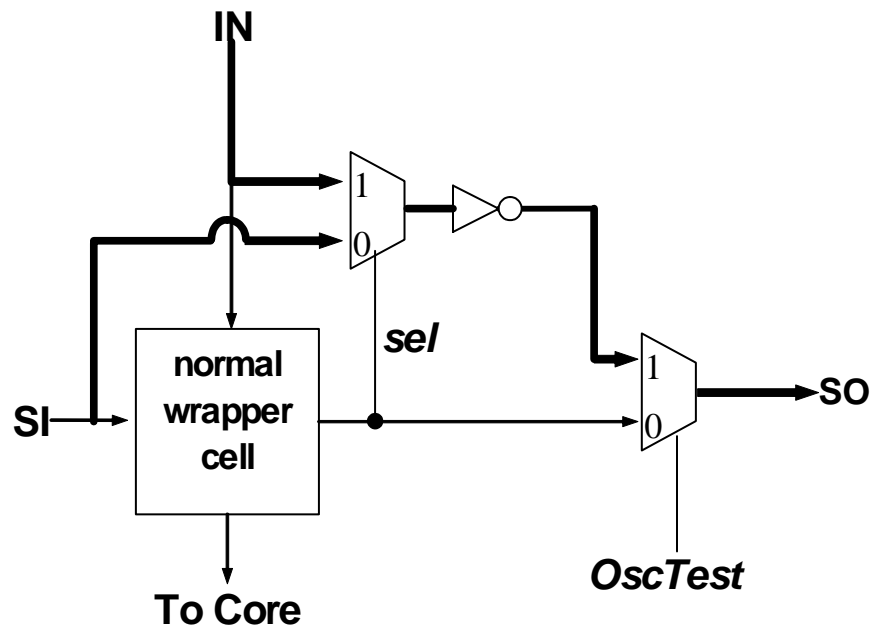
by Katherine Shu-Min Li



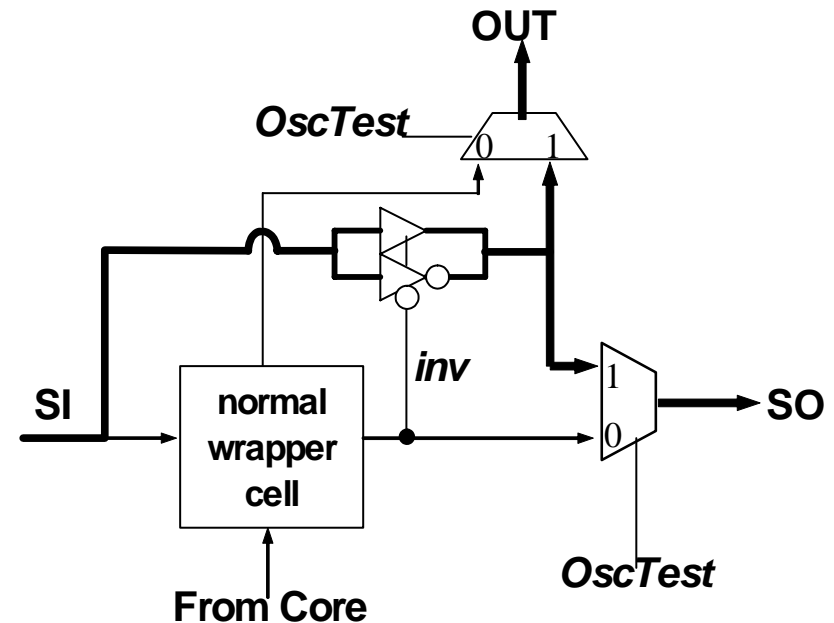
# SPICE Simulation Waveforms



# P1500 Modified Wrapper Cells for SOC

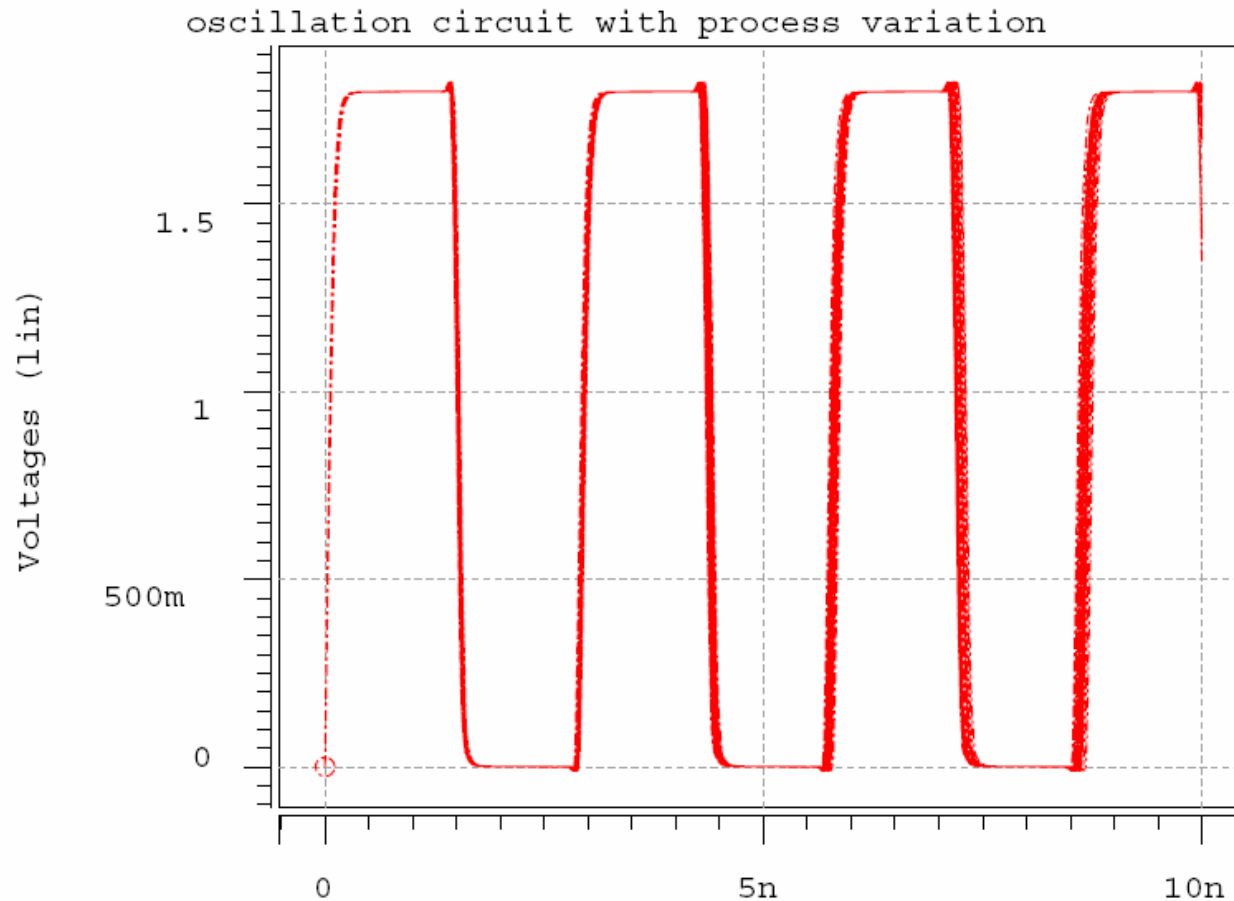


(a) Input Cell



(b) Output Cell

# Process Variation Effects on Oscillation Signals in Nanotechnology



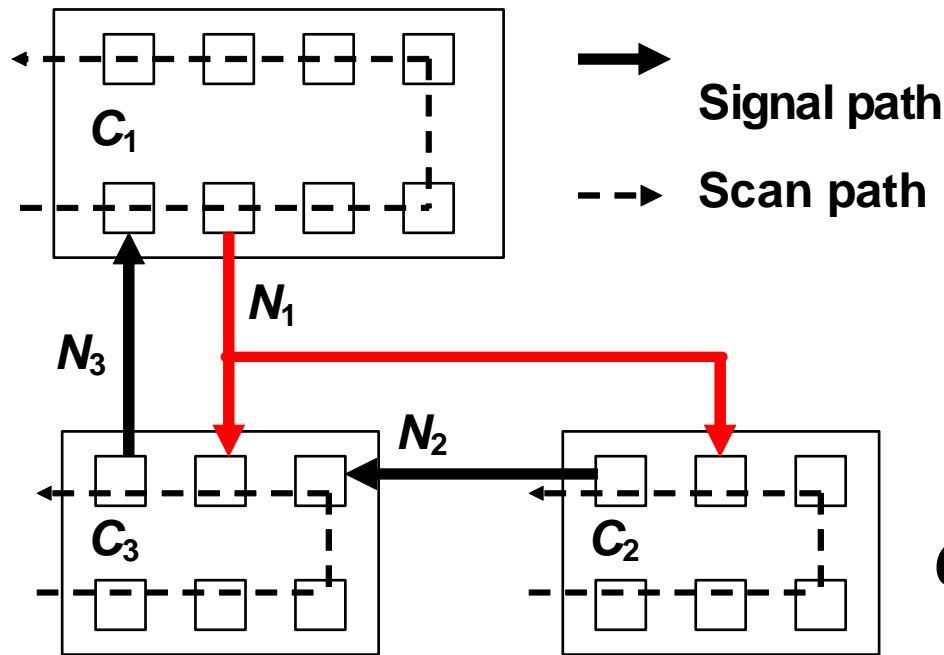
# Interconnect Modeling

- **Interconnect Detection Model**
  - Interconnect Model for Oscillation Ring Test (ORT)
  - 2-pin nets
- **Interconnect Diagnosis Model**
  - Interconnect Model for Oscillation Ring Diagnosis (ORD)
  - Net segments

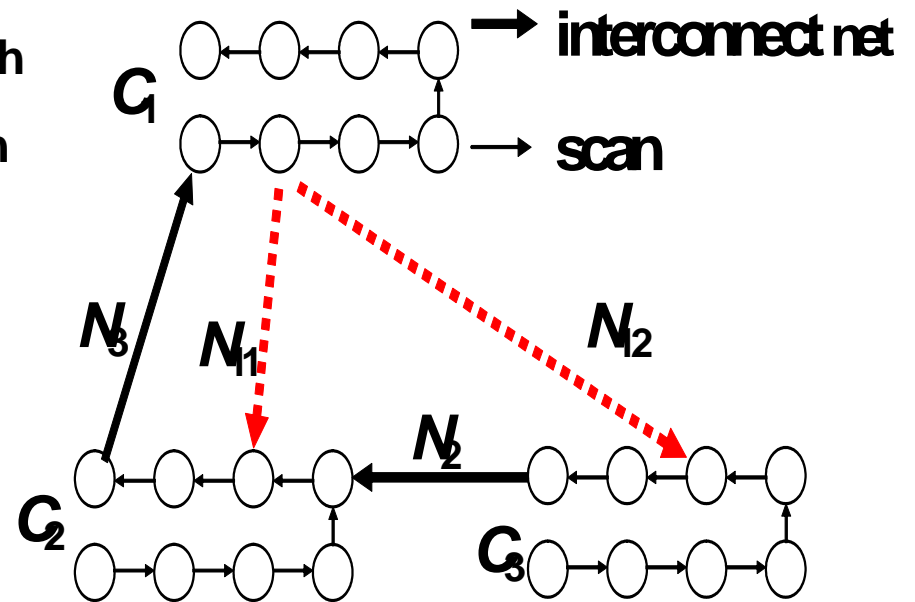
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  - **Interconnect Model for Oscillation Ring Diagnosis (ORD)**
  - **Net segments**

# Graph Model for Oscillation Ring Test



**(a) Hypernets**

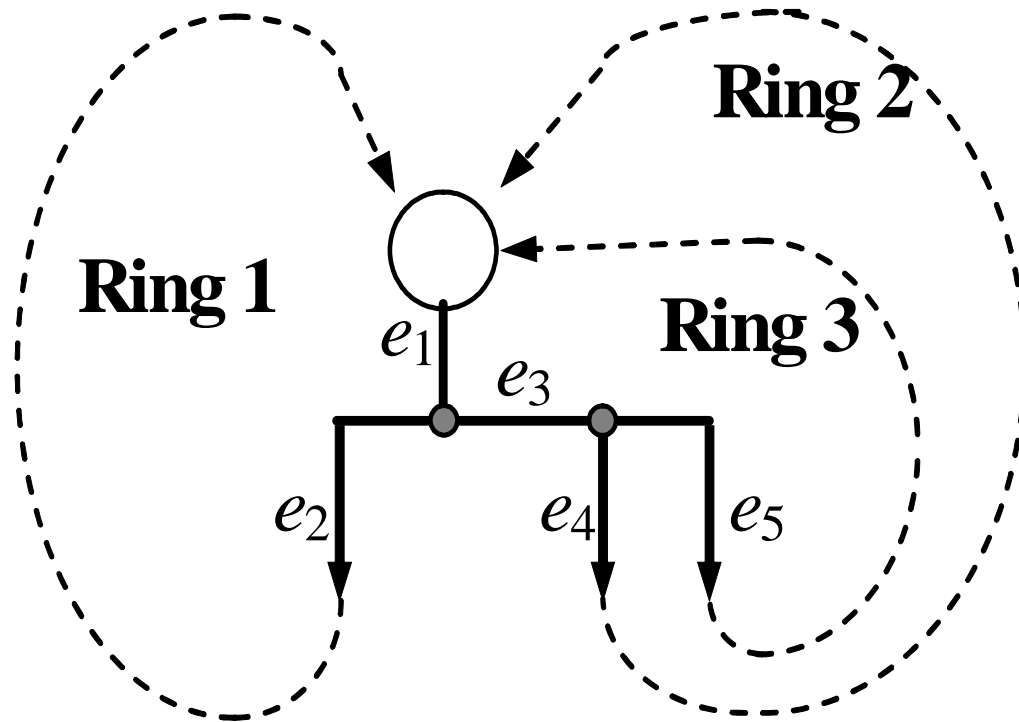


**(b) 2-pin nets**

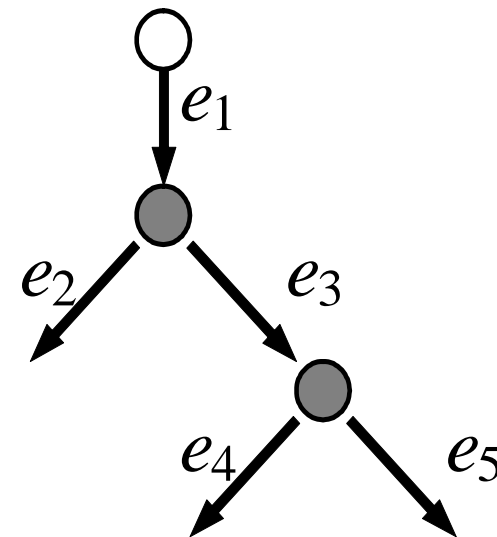
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# Interconnect Diagnosis Model (ORD)

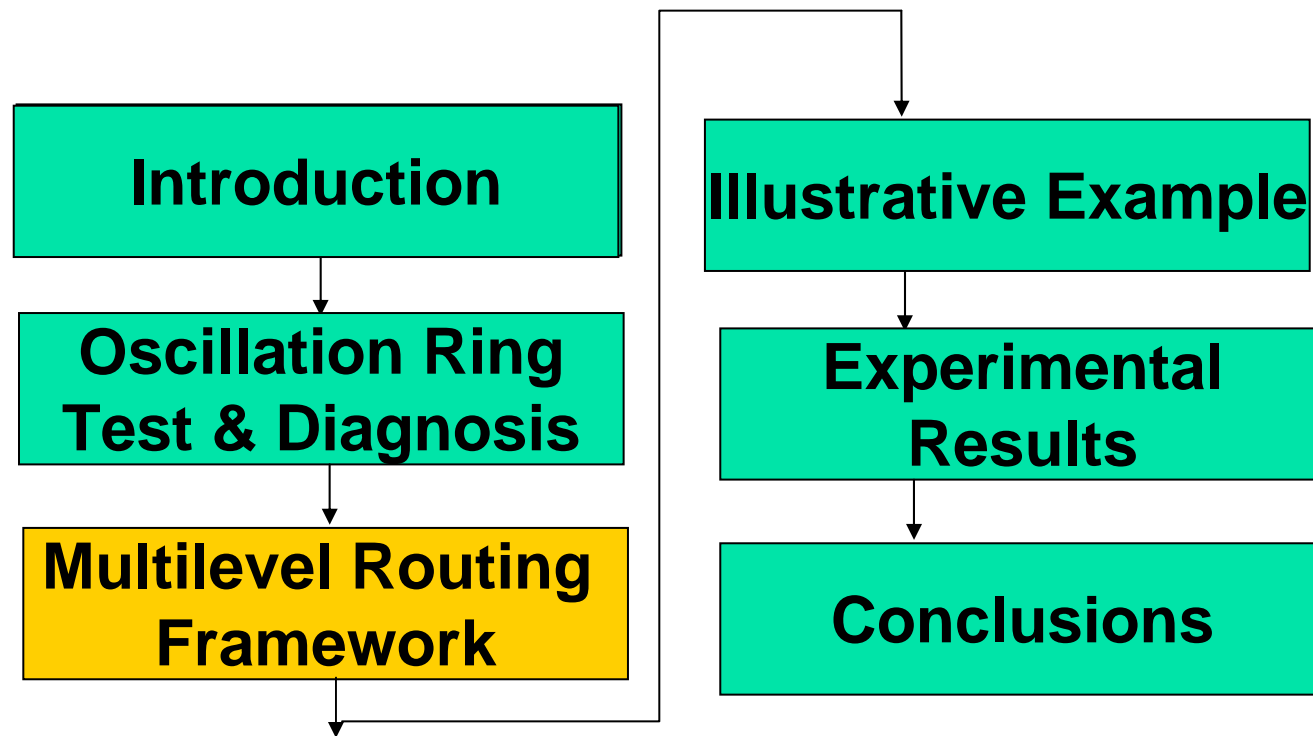


(a) Hypernets

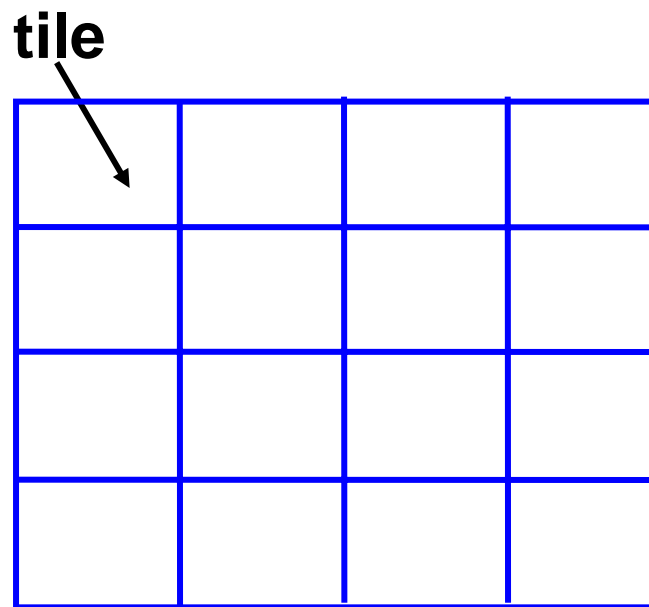


(b) Interconnect Net Segments

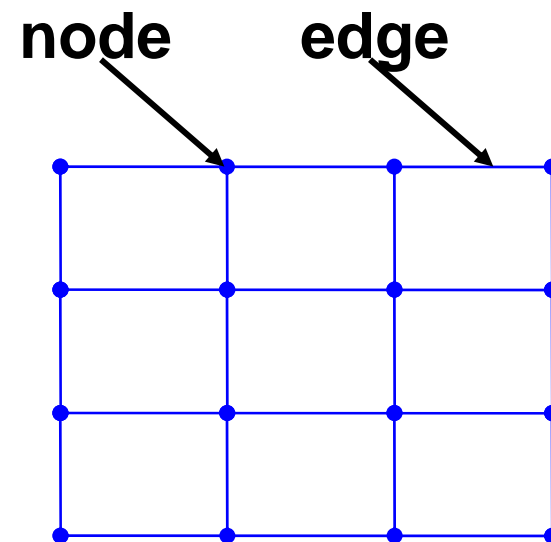
# Outline



# Routing Model

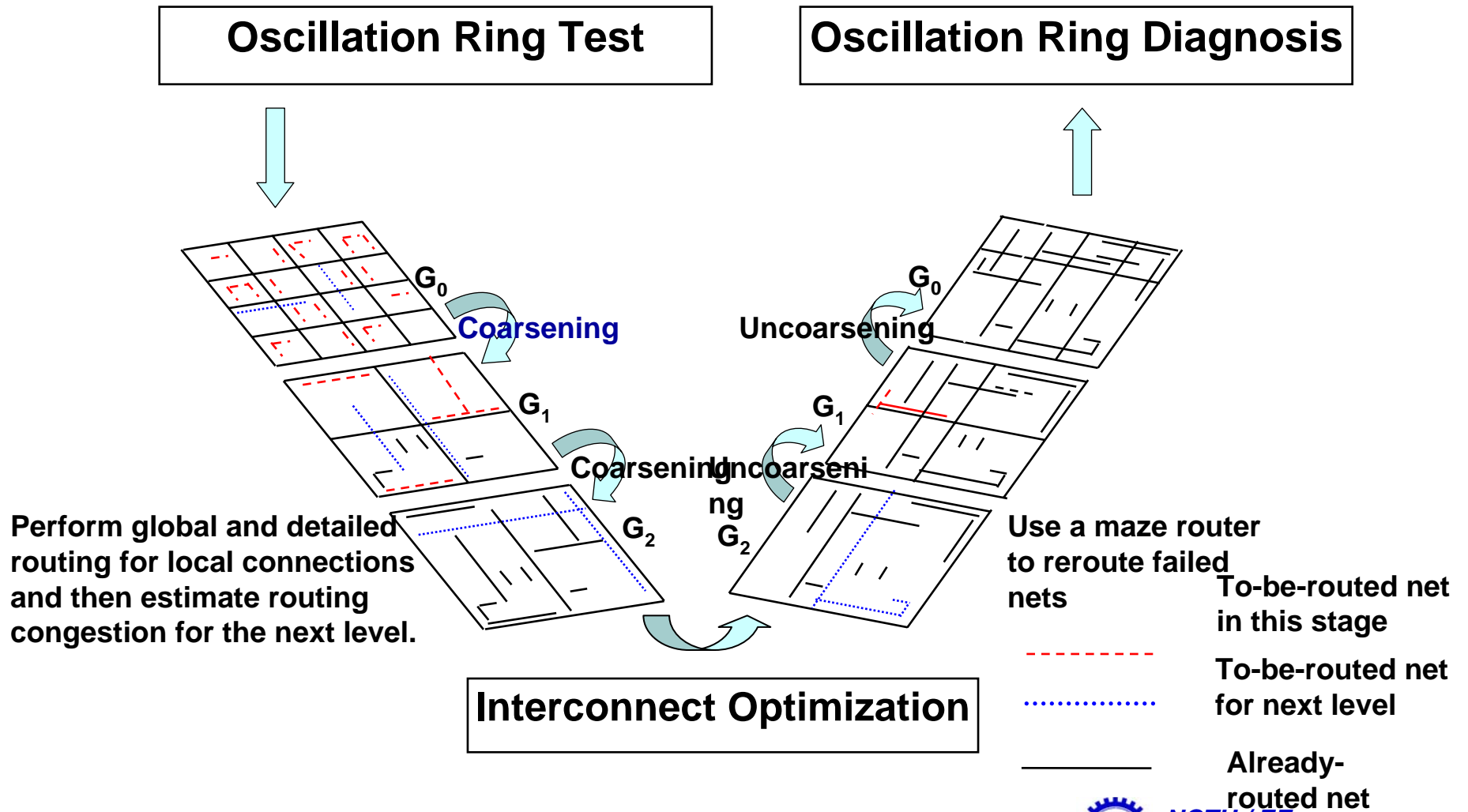


(a) Routing Plane



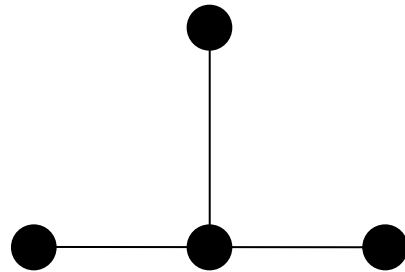
(b) Routing Graph Model

# Testability-Aware Integrated Multilevel Framework

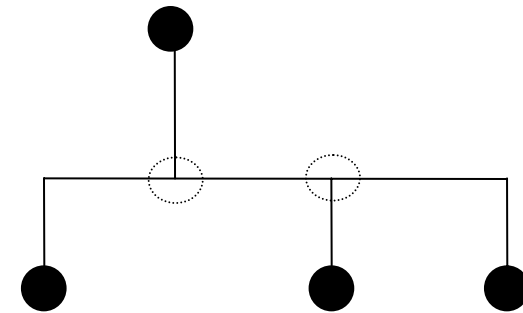


# Diagnosability-Aware Routing Structure

by Katherine Shu-Min Li



(a) Router Diagnosis  
Model: **3 nets**

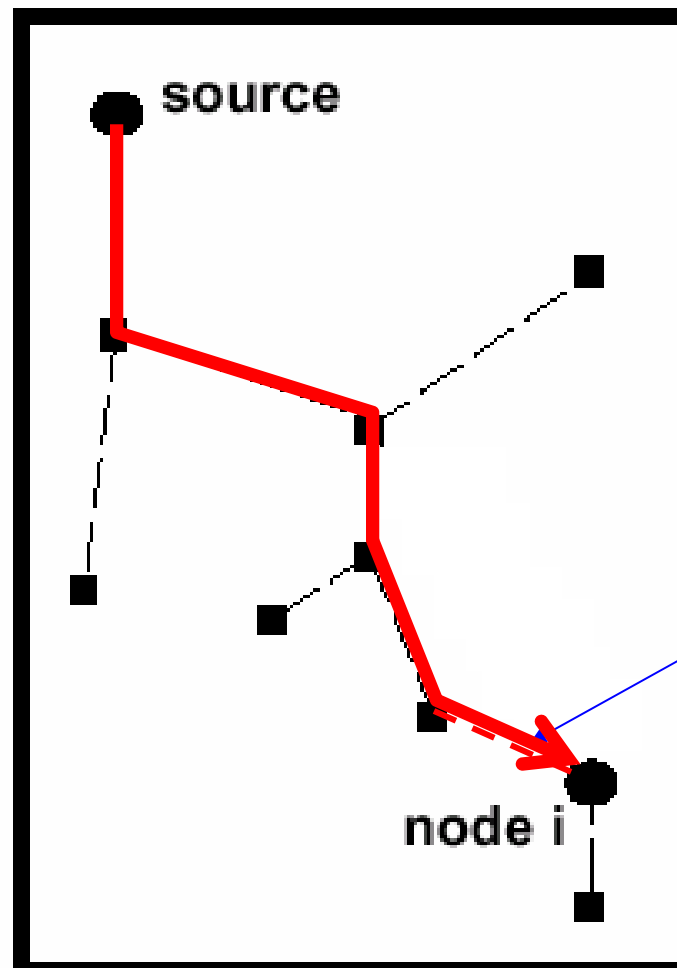


(b) Router Diagnosis  
Model based on Steiner  
Tree: **5 nets**



# Recalling Modification

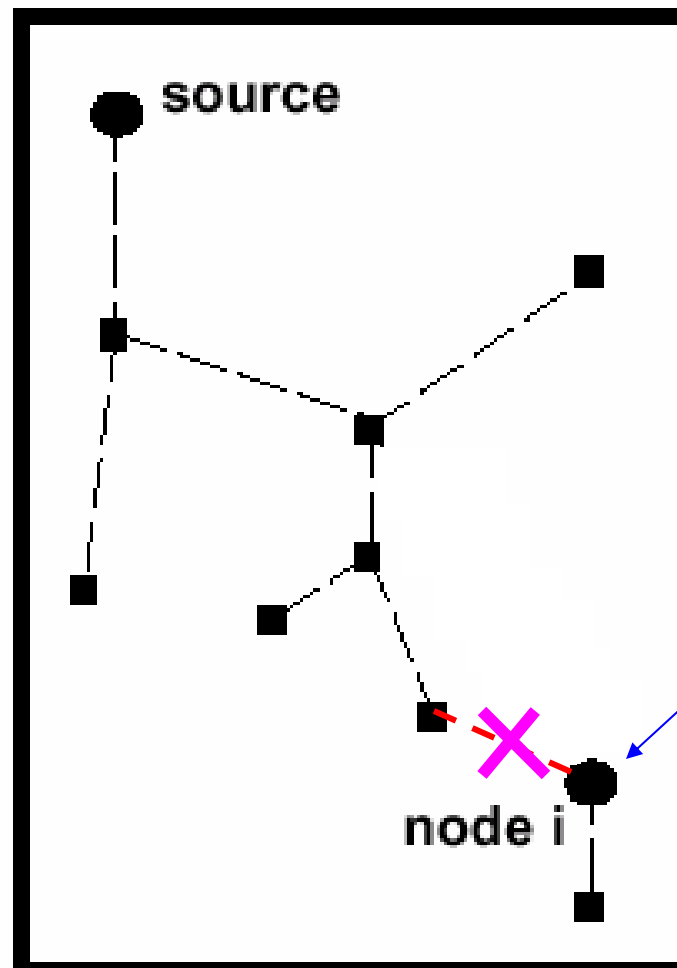
timing analysis



target connection

# Recalling Modification

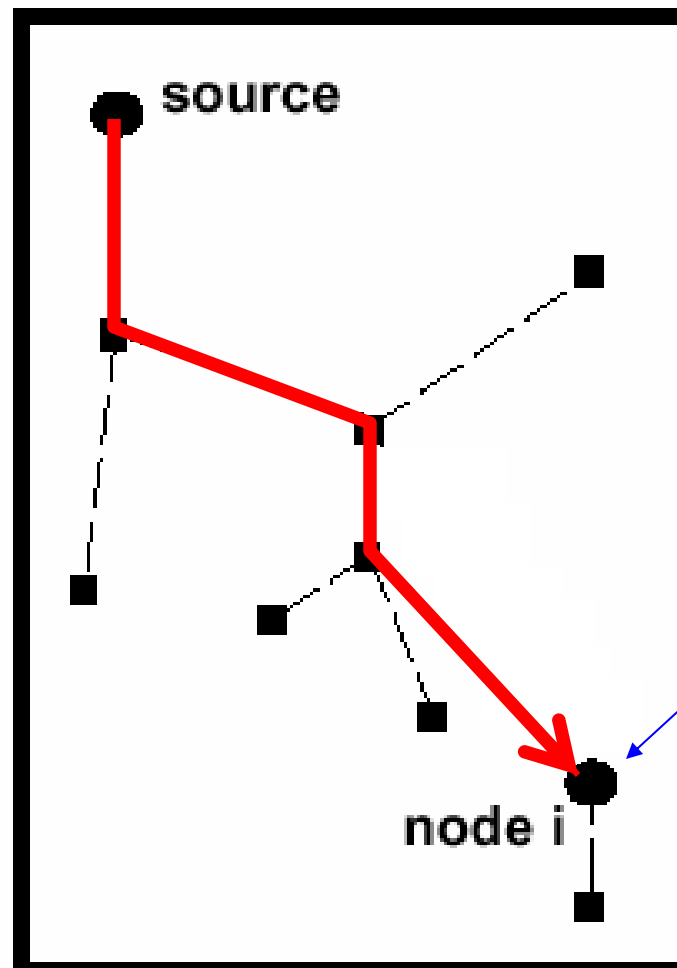
delete the connection



timing violation

# Recalling Modification

timing analysis  
again



connect to a  
new parent



# MINCOUNT\_Shortest Path Algorithm with $n(v)$ computation

**MINCOUNT\_SPA( $G, dist, s$ )**

1. Intialize\_Source( $G, s$ );
2.  $S \leftarrow \emptyset$ ;
3.  $Q \leftarrow V[G]$ ;
4. while  $Q \neq \emptyset$
5.  $u \leftarrow \text{Extract\_Min}(Q)$ ;
6.  $S \leftarrow S \cup \{u\}$ ;
7. for each  $v \in \text{Adj}[u]$
8. **Count\_Nodes( $u, v, dist$ );**

**Count\_Nodes( $u, v, dist$ )**

1. if  $d(v) \geq d(u) + dist(u, v)$
2.  $d(v) \leftarrow d(v) + dist(u, v)$ ;
3. if  $n(v) \geq n(u) + node(u, v)$
4.  $n(v) \leftarrow n(u) + node(u, v)$ ;
5. record  $u$  as the predecessor routing region of  $v$ .

# Cost Metric for Routing Density Control

Cost Function in Uncoarsing Stage

$$\alpha(R_e) = \sum_{e \in R_e} c_e$$

$$c_e = \begin{cases} \frac{1}{2^{[(p_e/t) - d_e]}} & d_e < (p_e/t) \\ 1 & d_e \geq (p_e/t) \end{cases}$$

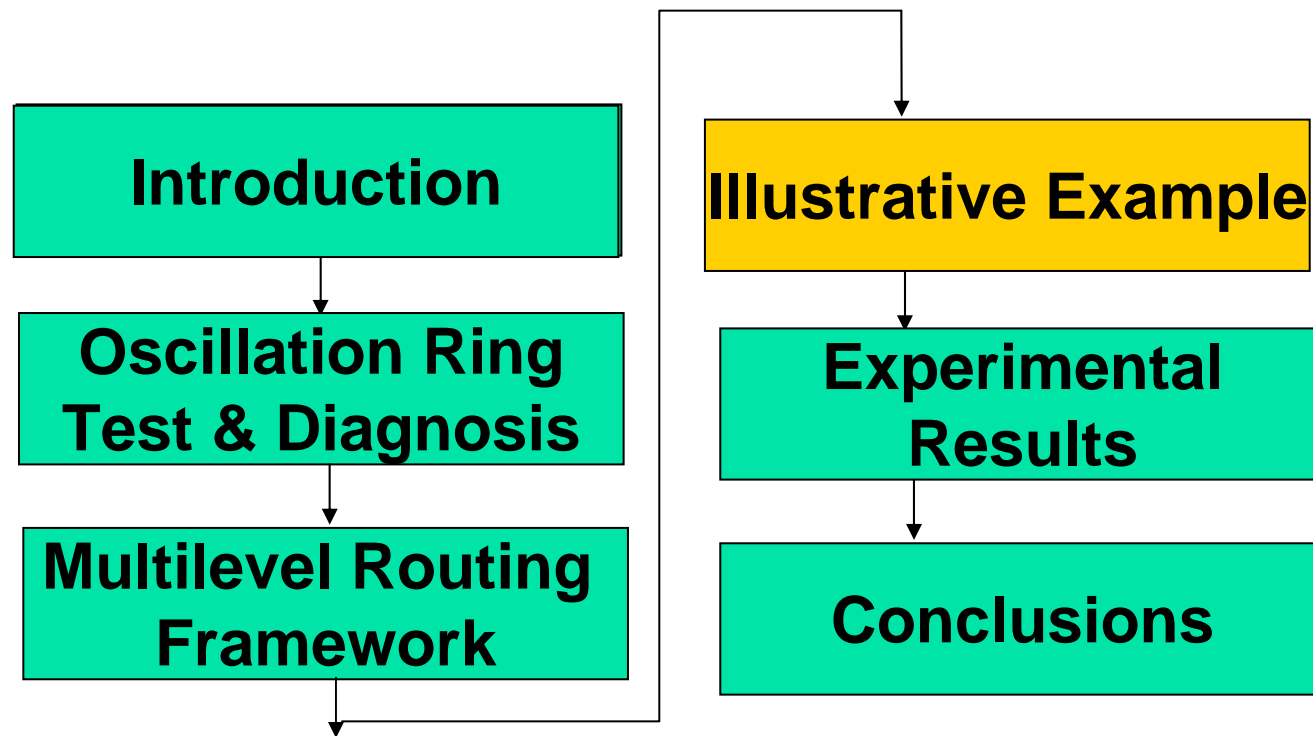
- $\alpha: E_i \rightarrow R$
- $R_e$
- $c_e$ : congestion of edge
- $p_e$ : capacity of nets
- $d_e$ : number of nets

Cost Function in Coarsing Stage

$$\beta(R_e) = \sum_{e \in R_e} (a \cdot c_e + b \cdot o_e)$$

- $a, b$ : user-defined parameters
- $o_e \in \{0,1\}$

# Outline



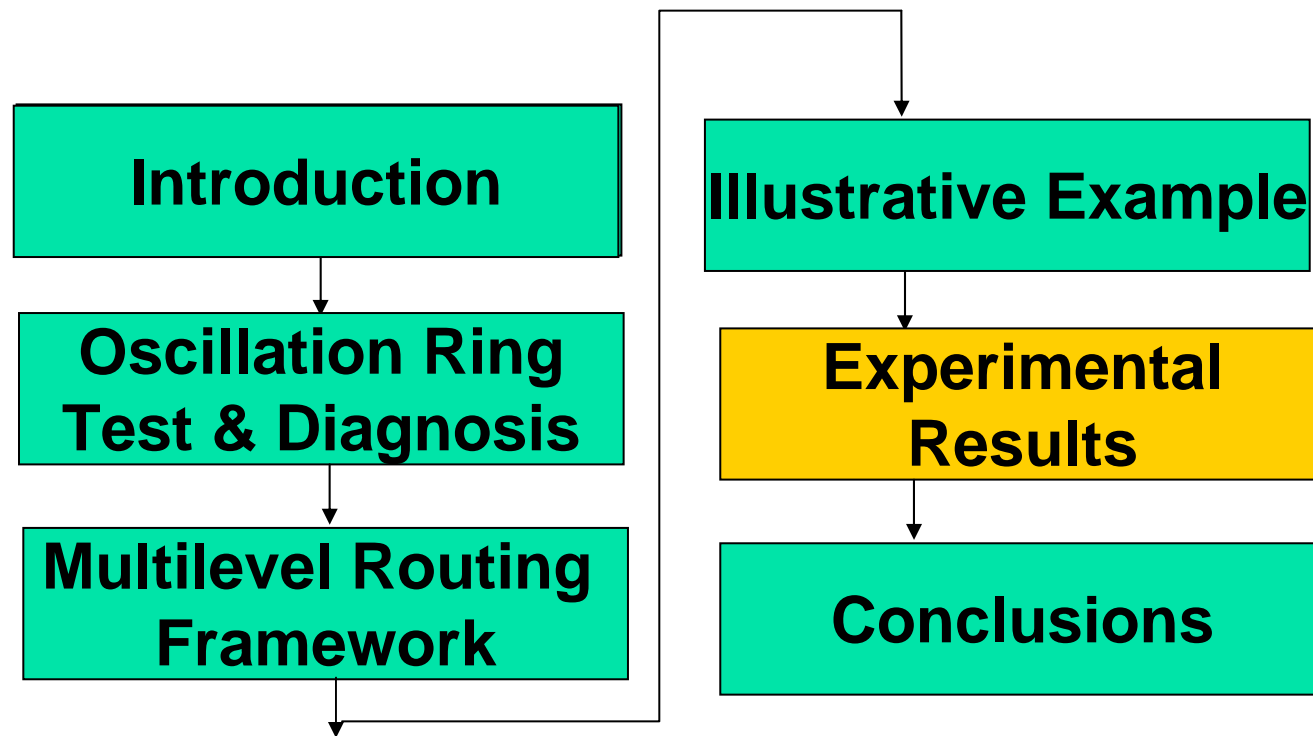
# An Illustrated Example

$$f_i = f \times \frac{n_i}{n}$$

$$\varepsilon = \frac{1}{f_{\min} \times T_0} \leq \zeta$$

- $f_i$ : frequency of the  $i$ th oscillation ring
  - $n_i$ : counter's content of the  $i$ th oscillation ring
  - $\varepsilon$ : counter's maximum measurement error
  - $\xi$ : delay measurement resolution
- Let  $4 \text{ MHz} \leq f_i \leq 400 \text{ MHz}$ ,  $f_{\min} = 4 \text{ MHz}$ ,  $\xi = 0.001$ , thus,  $n_i = 1/\xi = 1,000$ , we have  $T_0 = 250 \mu\text{s}$ .

# Outline



# Experimental Results

- **Testability enhancement of interconnect detection and diagnosis**
- **Congestion control for multi-objective optimization**

# Experimental Results

## for Testability Enhancement of Interconnect Detection and Diagnosis

by Katherine Shu-Min Li

Circuit	Statistics				#rings constructed for testability $ R_t $ & diagnosis $ R_d $	
	#core	#pad	#hyp	#2-pin	$ R_t $	$ R_d $
ac3	27	75	211	416	133(33.3ms)	374(93.5ms)
ami33	33	42	117	343	242(60.5ms)	303(75.8ms)
ami49	49	22	361	475	156(39ms)	386(96.5ms)
apte	9	73	92	136	73(18.3ms)	122(30.5ms)
hp	11	45	72	195	81(20.3ms)	164(41ms)
xerox	10	2	161	356	218(54.5ms)	342(85.5ms)



# Experimental Results

- Testability enhancement of interconnect detection and diagnosis
- Congestion control for multi-objective optimization

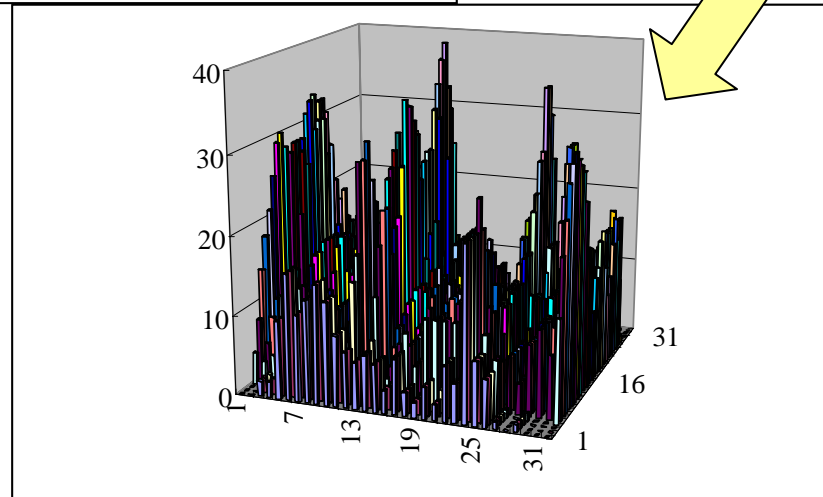
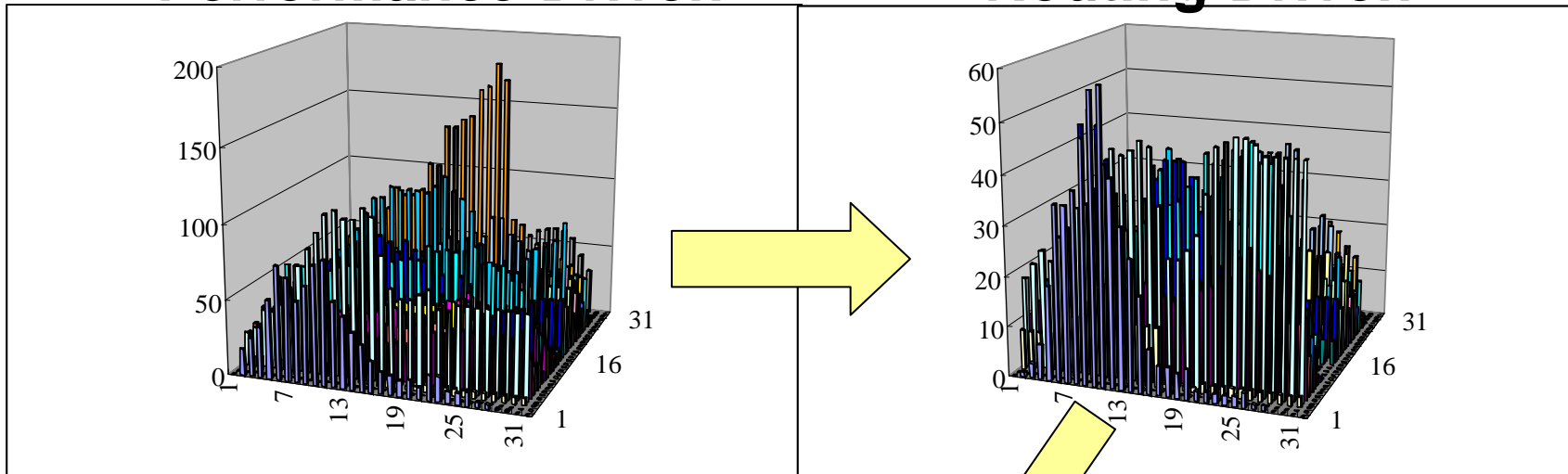
# Routing Benchmark Circuits

<b>Circuit</b>	<b>Size (mm)</b>	<b>#Layers</b>	<b>#Nets</b>	<b>#Pins</b>
<b>Mcc1</b>	<b>39000×45000</b>	<b>4</b>	<b>1694</b>	<b>3101</b>
<b>Mcc2</b>	<b>152400×152400</b>	<b>4</b>	<b>7541</b>	<b>25024</b>
<b>Struct</b>	<b>4903x4904</b>	<b>3</b>	<b>3551</b>	<b>5717</b>
<b>Primary1</b>	<b>7552x4988</b>	<b>3</b>	<b>2037</b>	<b>2941</b>
<b>Primary2</b>	<b>10438x6468</b>	<b>3</b>	<b>8197</b>	<b>11226</b>
<b>S5378</b>	<b>4330x2370</b>	<b>3</b>	<b>3124</b>	<b>4734</b>
<b>S9234</b>	<b>4020x2230</b>	<b>3</b>	<b>2774</b>	<b>4185</b>
<b>S13207</b>	<b>6590x3640</b>	<b>3</b>	<b>6995</b>	<b>10562</b>
<b>S15850</b>	<b>7040x3880</b>	<b>3</b>	<b>8321</b>	<b>12566</b>
<b>S38417</b>	<b>111430x6180</b>	<b>3</b>	<b>21035</b>	<b>32210</b>
<b>S38584</b>	<b>12940x6710</b>	<b>3</b>	<b>28177</b>	<b>42589</b>

# Routing Density Distribution for MCC1 with Absolute Net Counts

Performance-Driven

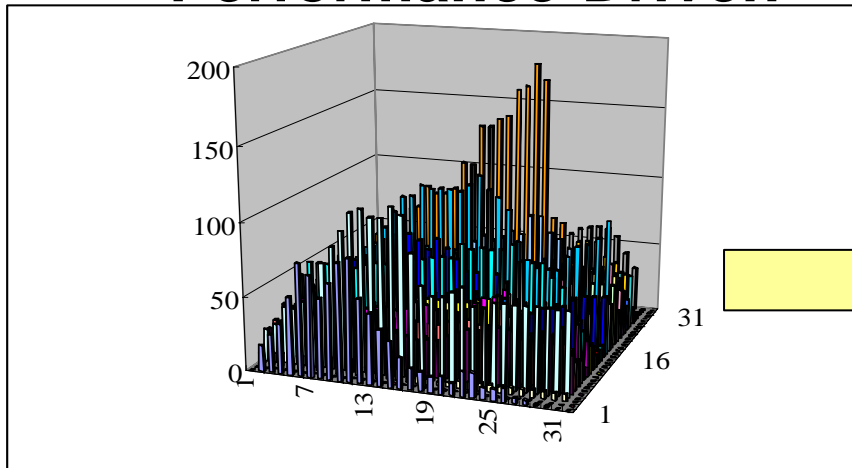
Routing-Driven



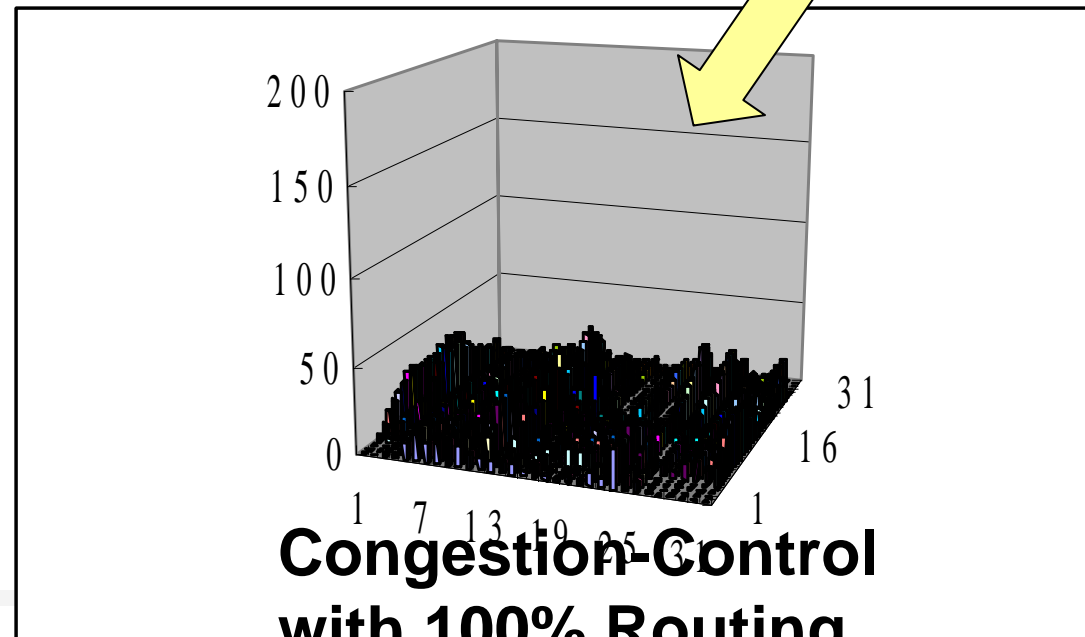
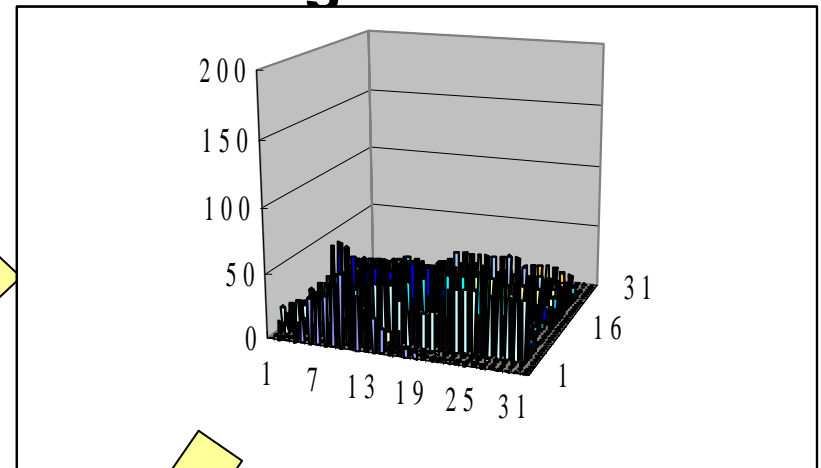
**Congestion-Control  
with 100% Routing**

# Routing Density Distribution for MCC1 with Normalized Net Counts

Performance-Driven



Routing-Driven



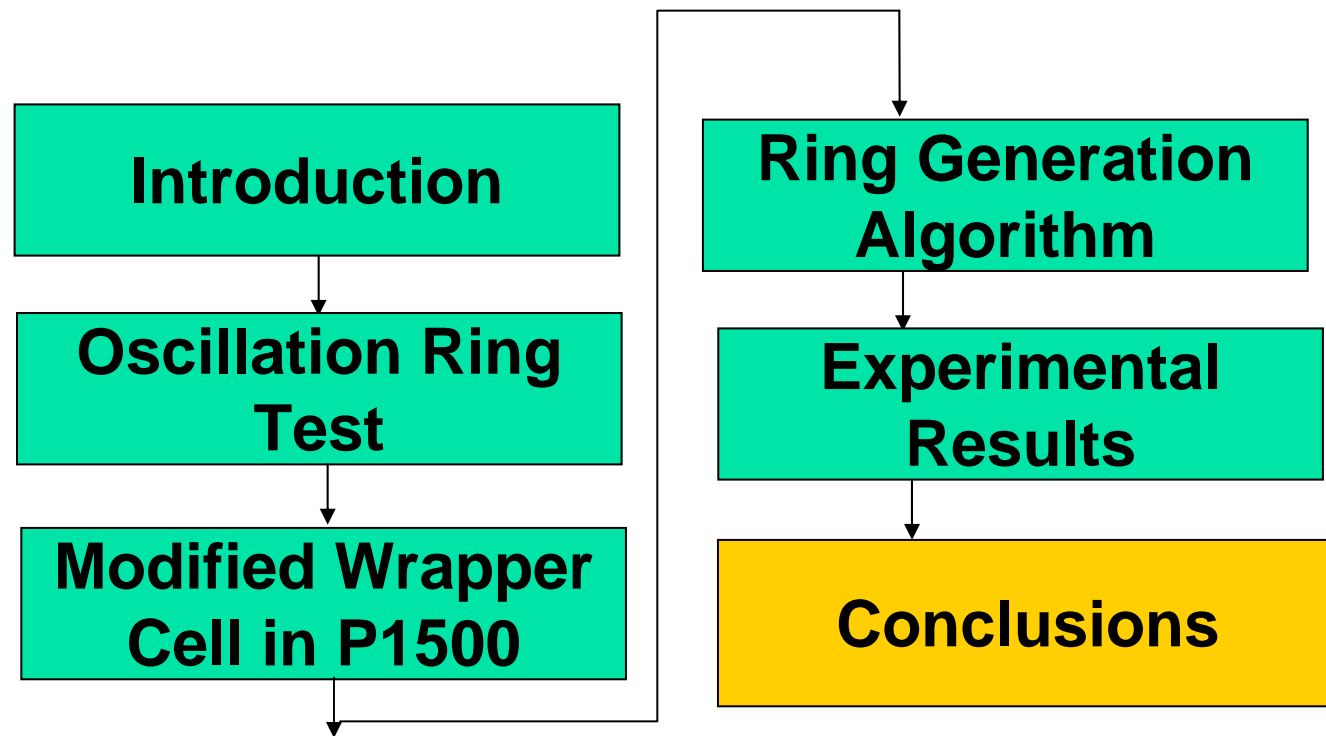
# Comparison of Maximum Density with both Maximum Delay and Average

Circuit	(A) Performance-Driven [LIN]				(B) Routability-Driven [LIN]				(C) Proposed Balanced Density with 100% routability			
	$d_{max}$	$d_{avg}$	#PEAK _Nets	CPU	$d_{max}$	$d_{avg}$	#PEAK _Nets	CPU	$d_{max}$	$d_{avg}$	#PEAK _Nets	CPU
Mcc1	5.E+07	1.E+07	181	223.68	2.03E+0 8	3.32E+0 7	61	77.11	2.03E+08	3.33E+0 7	45	72.63
Mcc2	7.E+07	5.E+06	274	5964.2	8.46E+0 7	5.12E+0 6	135	2855.5	8.51E+07	5.11E+0 6	96	2592.34
Struct	1.E+06	7.E+04	32	307.91	1.52E+0 6	7.13E+0 4	9	56.33	1.52E+06	7.13E+0 4	7	56.53
Primary 1	3.E+05	3.E+04	51	241.96	7.00E+0 5	5.51E+0 4	17	63.9	6.99E+05	5.50E+0 4	15	64.36
Primary 2	4.E+06	2.E+05	91	1808.56	3.92E+0 6	2.09E+0 5	28	298.17	3.91E+06	2.09E+0 5	25	295.32
S5378	9.E+04	6.E+03	49	23.28	8.91E+0 4	6.39E+0 3	17	4.13	8.94E+04	6.41E+0 3	15	4.29
S9234	1.E+05	9.E+03	61	16.78	2.53E+0 5	1.19E+0 4	15	2.91	2.53E+05	1.19E+0 4	14	2.9
S13207	4.E+05	2.E+04	114	65.45	4.64E+0 5	2.04E+0 4	30	14.44	4.64E+05	2.03E+0 4	27	14.57
S15850	6.E+05	3.E+04	140	181.82	2.66E+0 6	6.68E+0 4	30	22.04	2.66E+06	6.67E+0 4	26	21.77
S38417	5.E+05	3.E+04	272	741.53	8.52E+0 6	3.94E+0 5	27	50.02	8.52E+06	3.94E+0 5	23	50.08
S38584	2.E+06	6.E+04	295	1453.8	1.76E+0 8	1.25E+0 7	31	127.8	1.76E+08	1.25E+0 7	29	122.5
<b>Compa rison</b>	<b>0.27</b>	<b>0.32</b>	<b>4.84</b>	<b>3.34</b>	<b>1.00</b>	<b>1.00</b>	<b>1.24</b>	<b>1.08</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>

# Comparison of Routing Statistical Density

Circuit	(A) Performance-Driven [LIN]				(B) Routability-Driven [LIN]				(C) Proposed Balanced Density with 100% routability			
	#AvgN <i>ets_y</i>	#AvgN <i>ets_h</i>	$\sigma_v$	$\sigma_h$	#AvgN <i>ets_y</i>	#AvgN <i>ets_h</i>	$\sigma_v$	$\sigma_h$	#AvgN <i>ets_y</i>	#AvgN <i>ets_h</i>	$\sigma_v$	$\sigma_h$
Mcc1	28.19	31.78	20.59	24.35	10.03	11.5	10.45	10.82	9.91	11.33	7.58	7.33
Mcc2	39.35	44.05	37.26	46.98	19.39	21.65	23.53	25.8	18.74	20.88	17.3	18.54
Struct	4.97	4.86	4.62	5.03	1.42	1.41	1.24	1.67	1.42	1.41	1.07	1.59
Primary1	2.29	1.74	3	5.67	0.7	0.6	1.05	1.95	0.7	0.6	1.2	1.8
Primary2	7.22	7.49	5.56	18.23	2.05	1.85	1.59	4.57	2.05	1.85	1.56	4.45
S5378	12.53	13.46	9.16	8.4	4.38	3.44	3.45	2.13	4.4	3.46	3.44	2.1
S9234	14.16	9.99	12.91	7.04	3.95	2.56	3.25	1.62	3.95	2.56	3.24	1.6
S13207	28.43	20.49	18.4	11.08	9.3	5.93	5.77	2.76	9.29	5.92	5.23	2.81
S15850	36.61	34.48	23.89	20.42	10.29	7.41	5.63	2.92	10.31	7.41	5.39	2.91
S38417	44.58	27.38	37.36	27.94	7.31	4.27	4.75	2.17	7.3	4.27	4.44	2.18
S38584	43.99	30.53	35.93	20.12	9.06	5.8	5.74	2.86	9.05	5.79	5.43	2.88
<b>Comparison</b>	<b>3.40</b>	<b>3.46</b>	<b>3.73</b>	<b>4.05</b>	<b>1.01</b>	<b>1.01</b>	<b>1.19</b>	<b>1.23</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>

# Outline



# Conclusion

- **Present an effective multilevel routing framework**
  - **Embedded OR Scheme to form prerouting and postrouting stage**
    - Show that the embedded oscillation ring test and diagnosis scheme is feasible based on the simulation results with TSMC .18  $\mu\text{m}$  process technology
    - OR scheme achieves 100% fault detection coverage and maximal diagnosability for testing interconnects in SoC
  - **Congestion Control in bottom-up and top-down two stages**
    - Apply a congestion-driven routing algorithm to reduce the multiple-fault probability, CMP and OPC induced effects, and crosstalk effects for yield enhancement

*Thank you!*

