A 3-D FPGA Wire Resource Prediction Model Validated using a 3-D Placement and Routing Tool

Young-Su Kwon, Payam Lajevardi, Anantha P. Chandrakasan, Frank Honore, and Donald E. Troxel

Microsystems Technology Laboratory

Massachusetts Institute of Technology

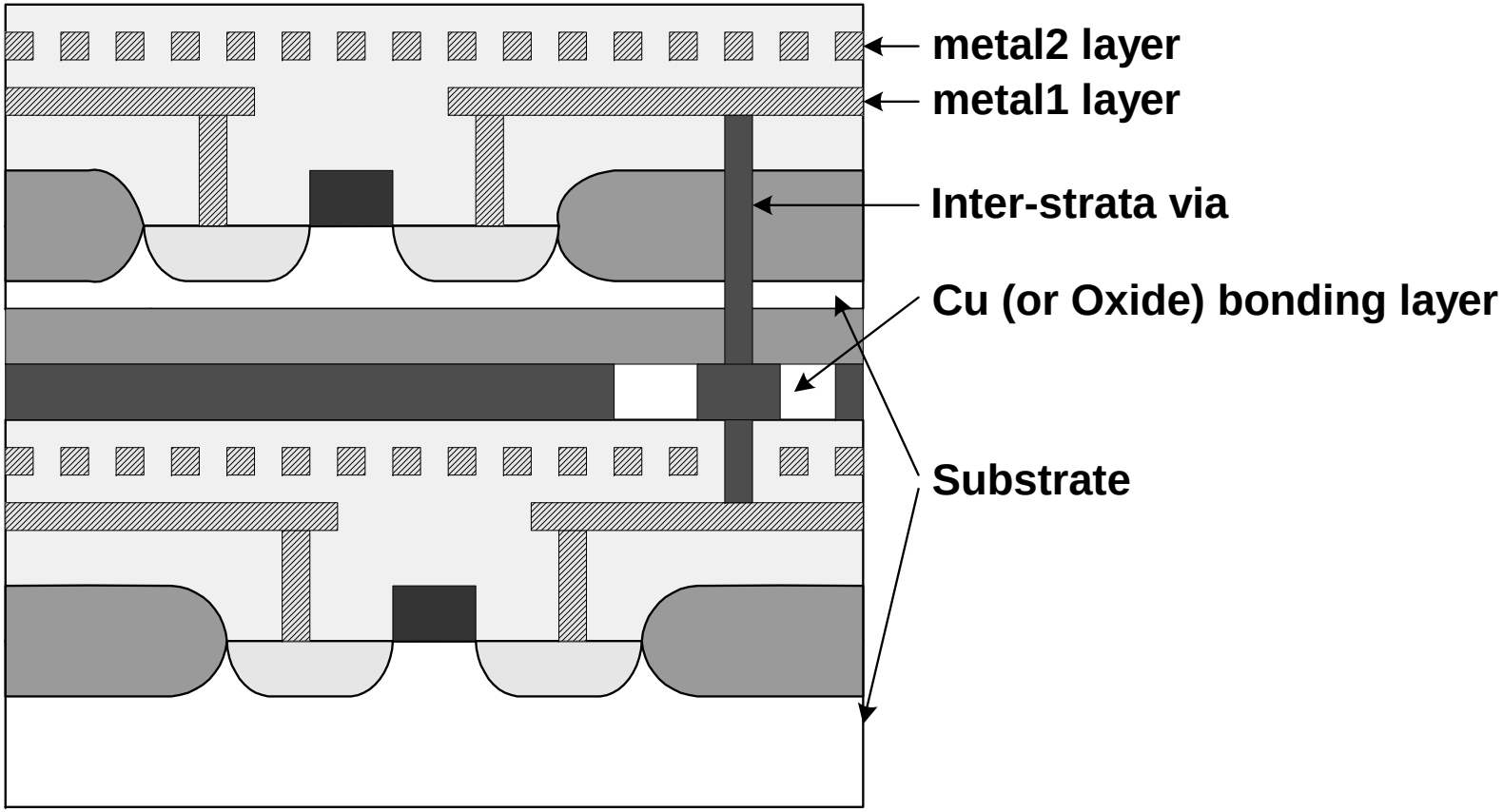
Contents

- Introduction
- 3-D FPGA Architecture and CAD
- 3-D FPGA Wire Resource Prediction Model
- Experiments
- Conclusion

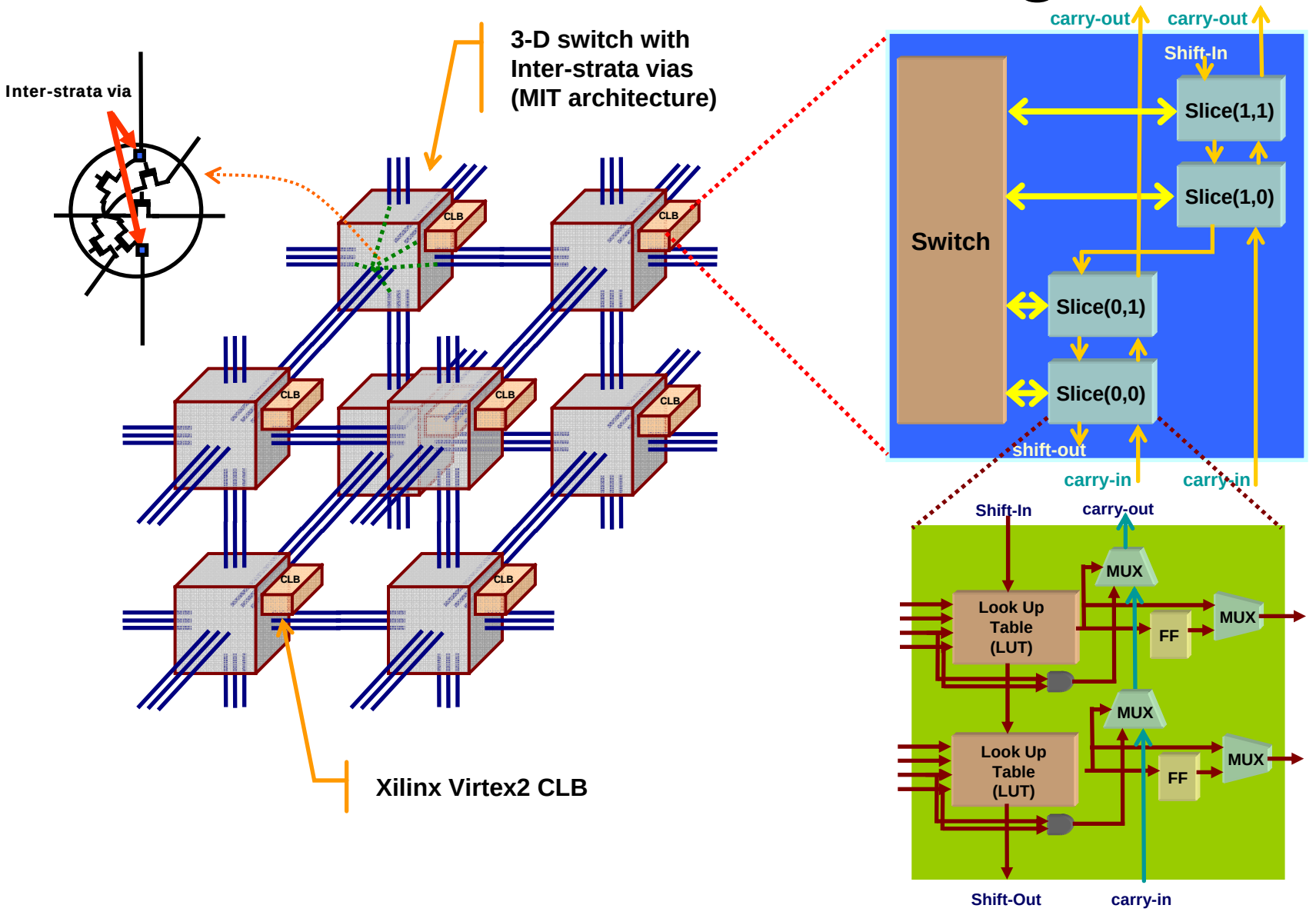
Introduction

- Performance of FPGAs is limited by interconnection resource.
- 3-D integration of FPGAs overcomes interconnection limitation by locating instances in 3-D spaces.
- 3-D FPGA reduces total wirelength, improves speed and reduces power consumption by reduced switching capacitance.

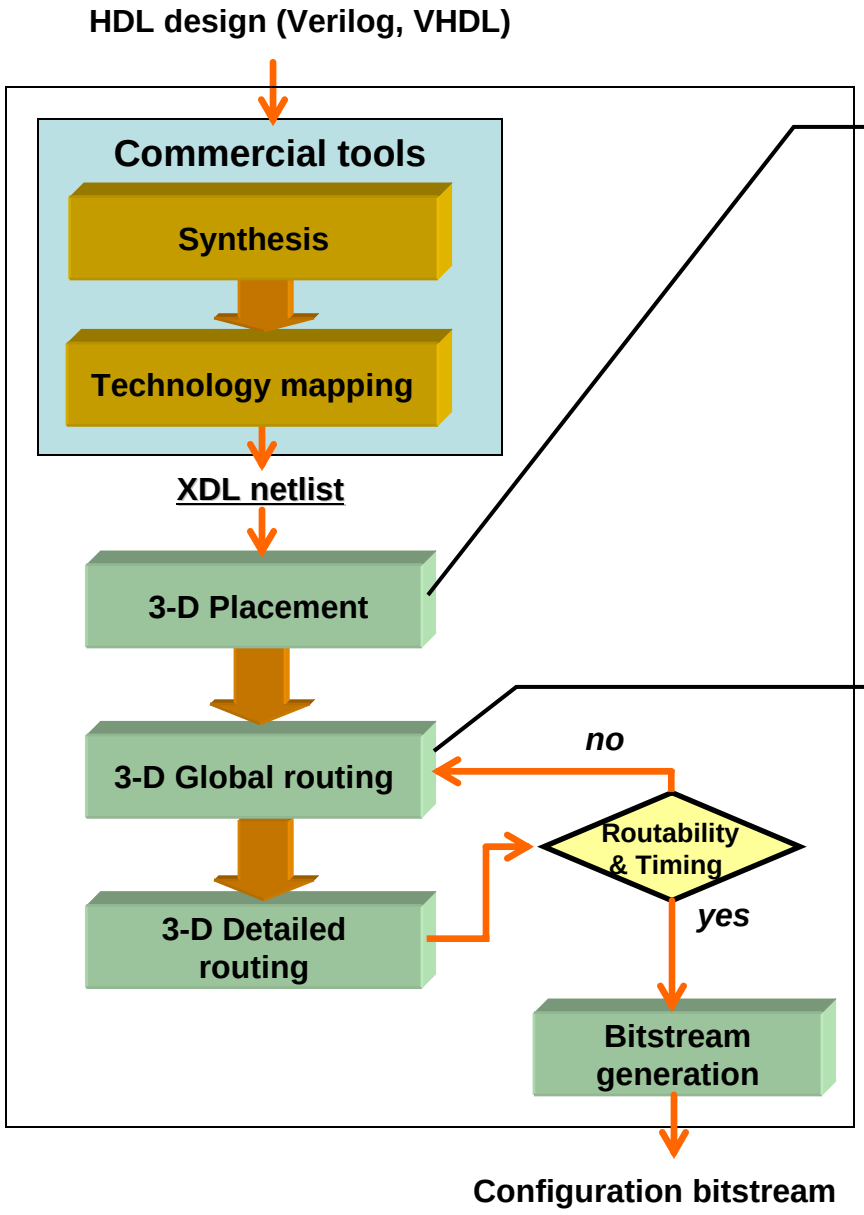
3-D Integration



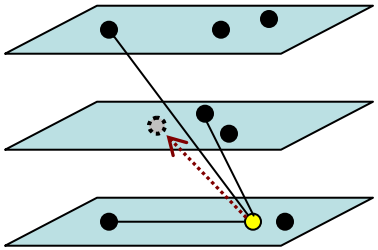
3-D FPGA Block Diagram



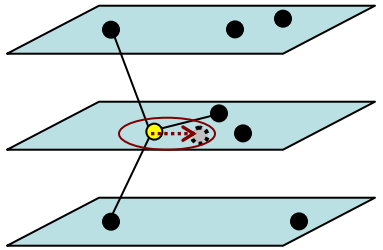
3-D FPGA CAD Flow



Two-phase simulated annealing : inter-strata and intra-stratum optimization

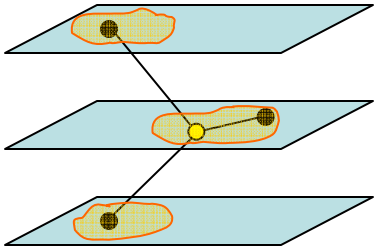


Inter-strata optimization searches for equilibrium location of each slice.



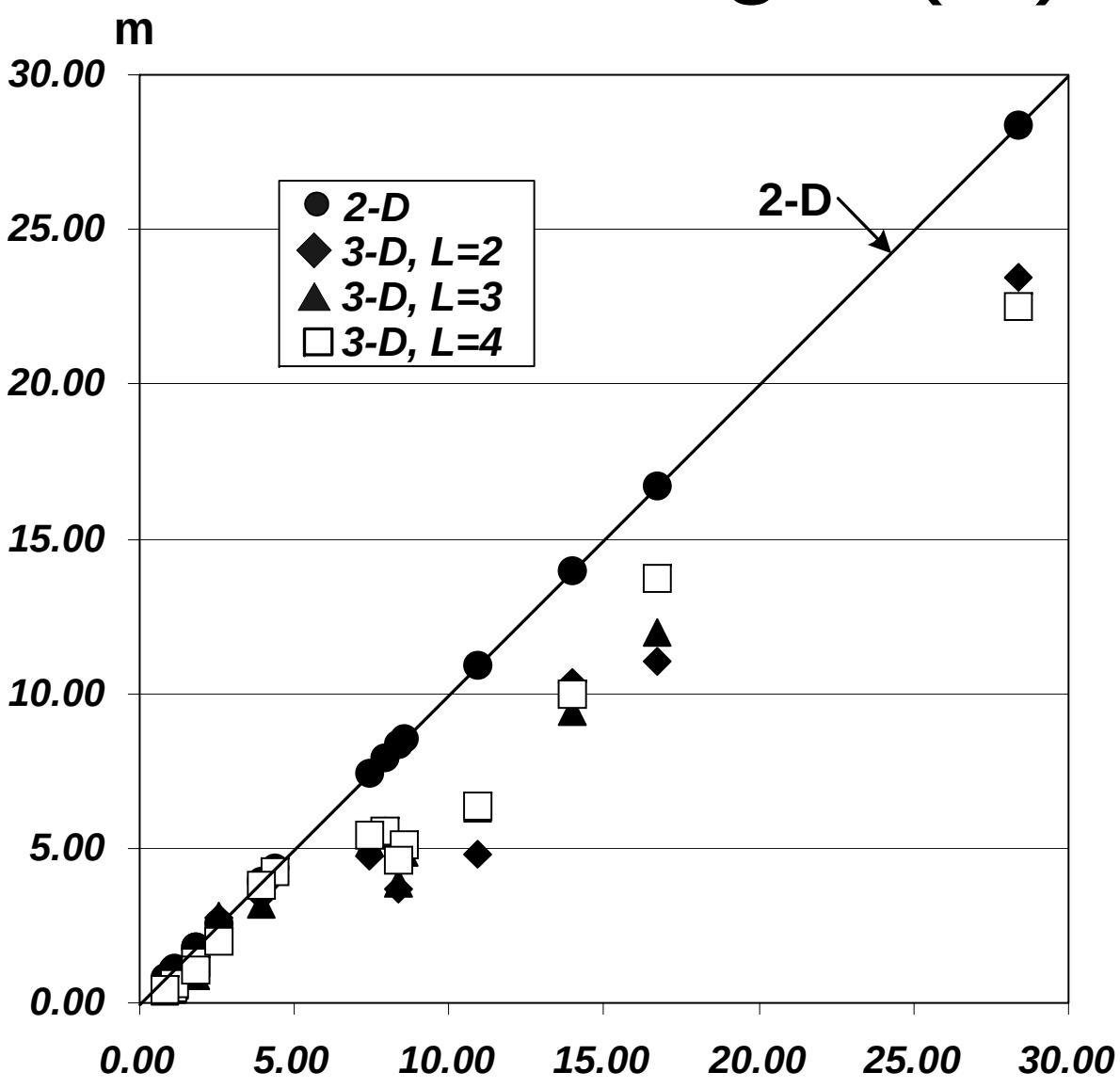
Intra-stratum optimization moves an instance around the current location on the same layer.

Negotiated routing with ripup and reroute considering routability and speed.



In Lee's maze routing, it reduces routing execution time to manage wavefront in each layer.

Total Wirelength (m)



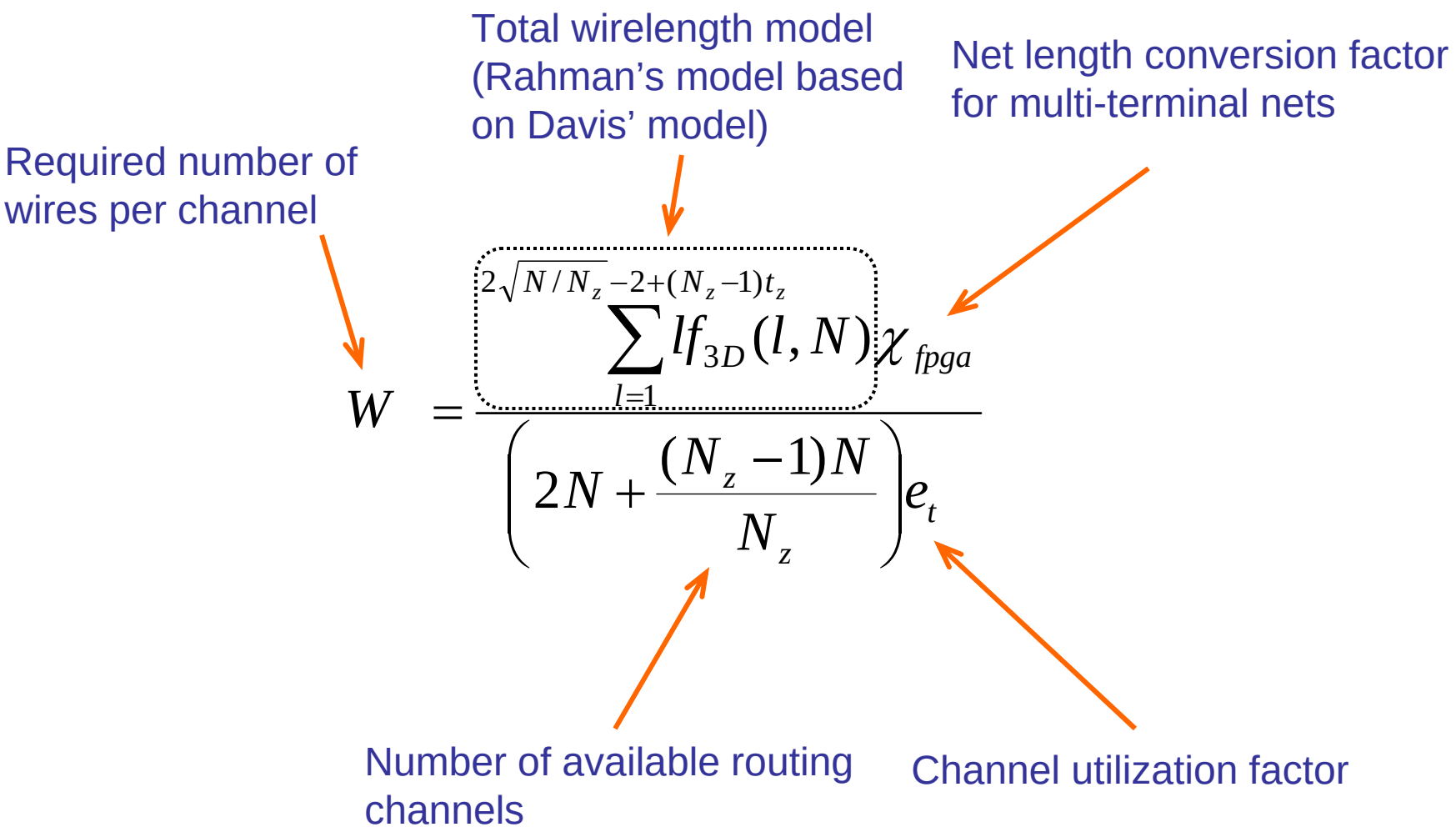
Critical Path Delay (ns)

	2D	3D,L=2	3D,L=3	3D,L=4
addrgen	16.27	13.75	13.12	11.44
bigkey	16.99	14.05	11.28	8.94
clma	6041.08	3749.02	4381.79	4423.25
diffeq	18.65	17.24	14.26	12.56
dsip	9.48	4.33	5.26	6.91
elliptic	373.75	72.47	55.90	66.98
frisc	1614.48	243.26	198.64	367.36
idct	350.12	114.01	153.94	79.36
mac1	181.34	100.47	52.62	35.83
mac2	847.35	745.84	311.27	289.85
matrix	71.45	29.72	19.98	24.89
rgb_interp	9.56	6.95	6.44	6.69
s38417	104.02	41.43	42.08	40.42
s38584	595.49	44.20	68.99	20.22
tseng	80.11	43.25	17.20	23.98
vp2	88.86	85.40	31.09	79.12

Wire Resource Prediction

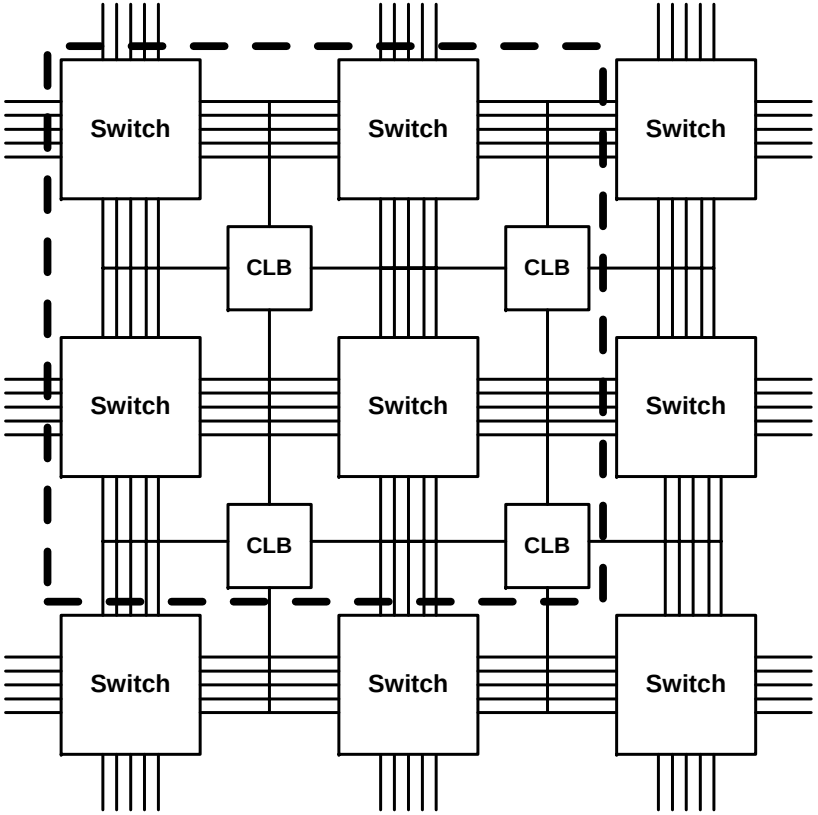
- What is it?
  - Wire resource prediction model predicts the number of wires per channel in FPGAs based on the estimation of total wirelength.
- Where can we use it?
  - Pre-determine of the routability of a circuit
  - Planning FPGA architecture without running P&R repeatedly

3-D FPGA Wire Prediction Model

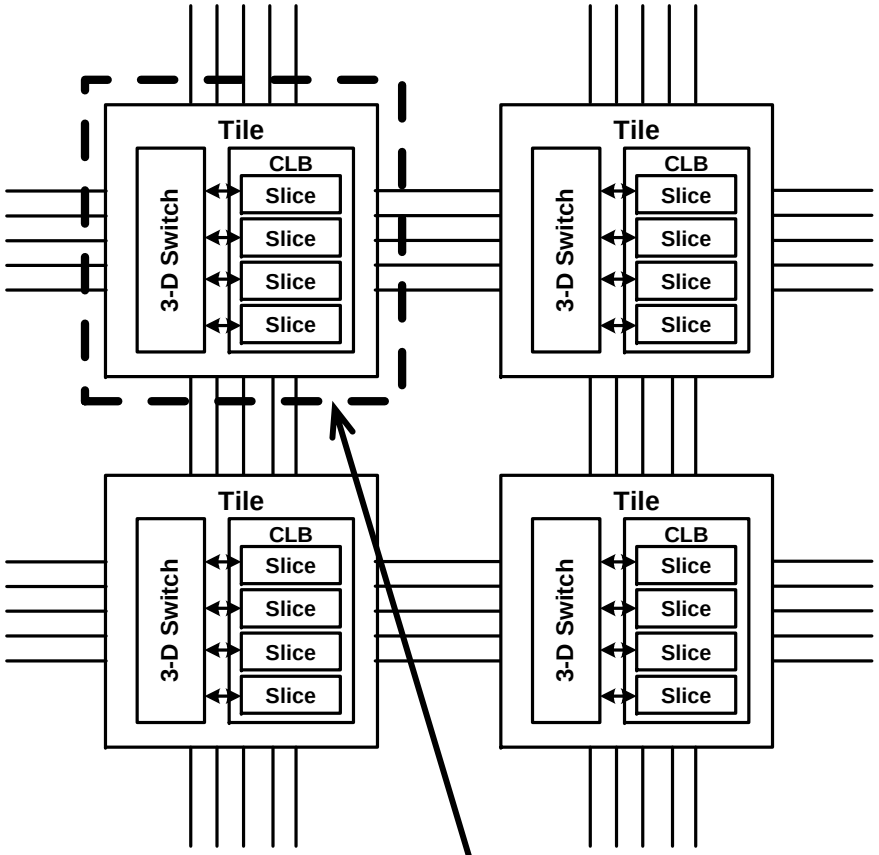


n_s for Routing Architecture

(a) 3-D FPGA in the previous model



(b) Our 3-D FPGA



n_s is the average number of active slices in a CLB

Extension of Wirelength Model

$$f_{3D}(l,N) \propto I_{3D}(l) M_{3D}(l,N)$$ *(Not a closed form equation)*

Number of tile pairs separated by length l

Number of nets with length l

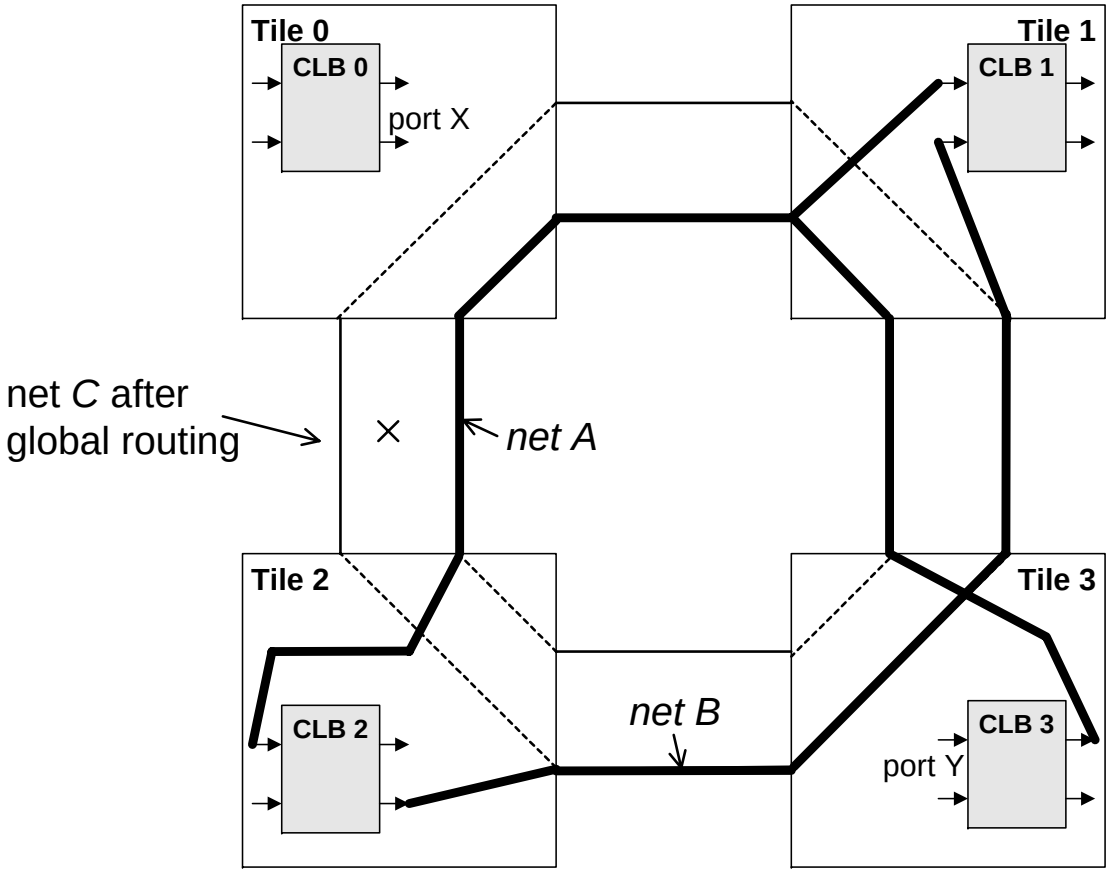
A tile with n_s slices becomes a basic unit.

Rent's Rule $T = kG^p$ → Scale $I_{3D}(l)$ by $n_s n_s^p = n_s^{p+1}$

N is scaled down to N / n_s (N is the number of slices, not tiles)

$$n_s^{p+1} f_{3D}(l, N / n_s)$$

Channel Utilization Factor



Global router determines that net C can be routed but it is not possible in the detailed routing, “routing anomaly”

→ Channel is not fully utilized by the router.

Extended 3-D FPGA Wire Prediction Model

n_s is the average number of active slices in a tile.

Total wirelength model extended by n_s (based on Rahman, Davis model)

Net length conversion factor for multi-terminal nets

$$W^C = \frac{n_s^{p+1} \sum_{l=1}^{2\sqrt{(N/n_s)/N_z}-2+(N_z-1)t_z} l f_{3D}(l, N/n_s)\chi_{fpga}}{\left(2(N/n_s)+\frac{(N_z-1)(N/n_s)}{N_z}\right)e_t^C}$$

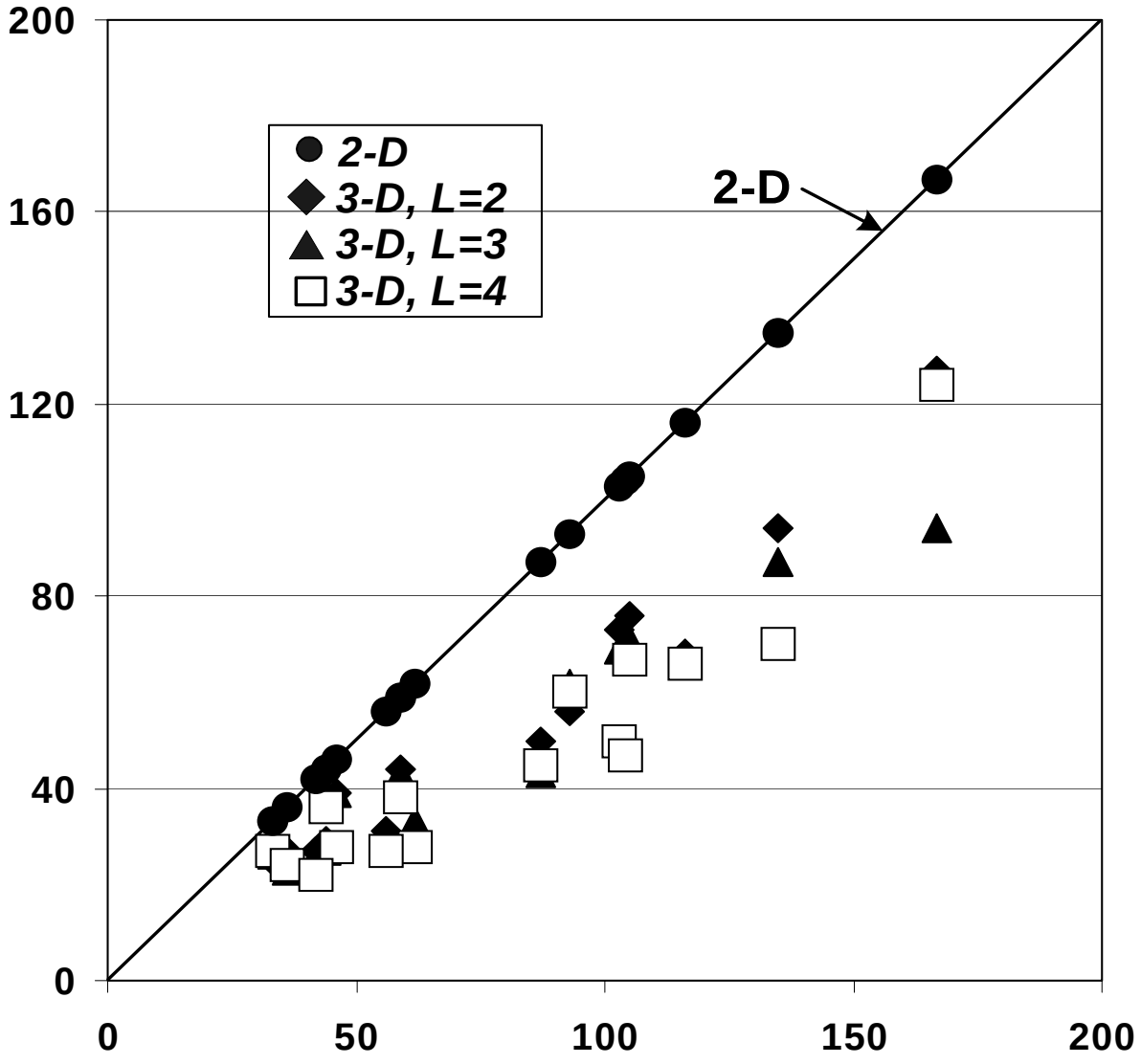
Number of available routing channels

Channel utilization factor

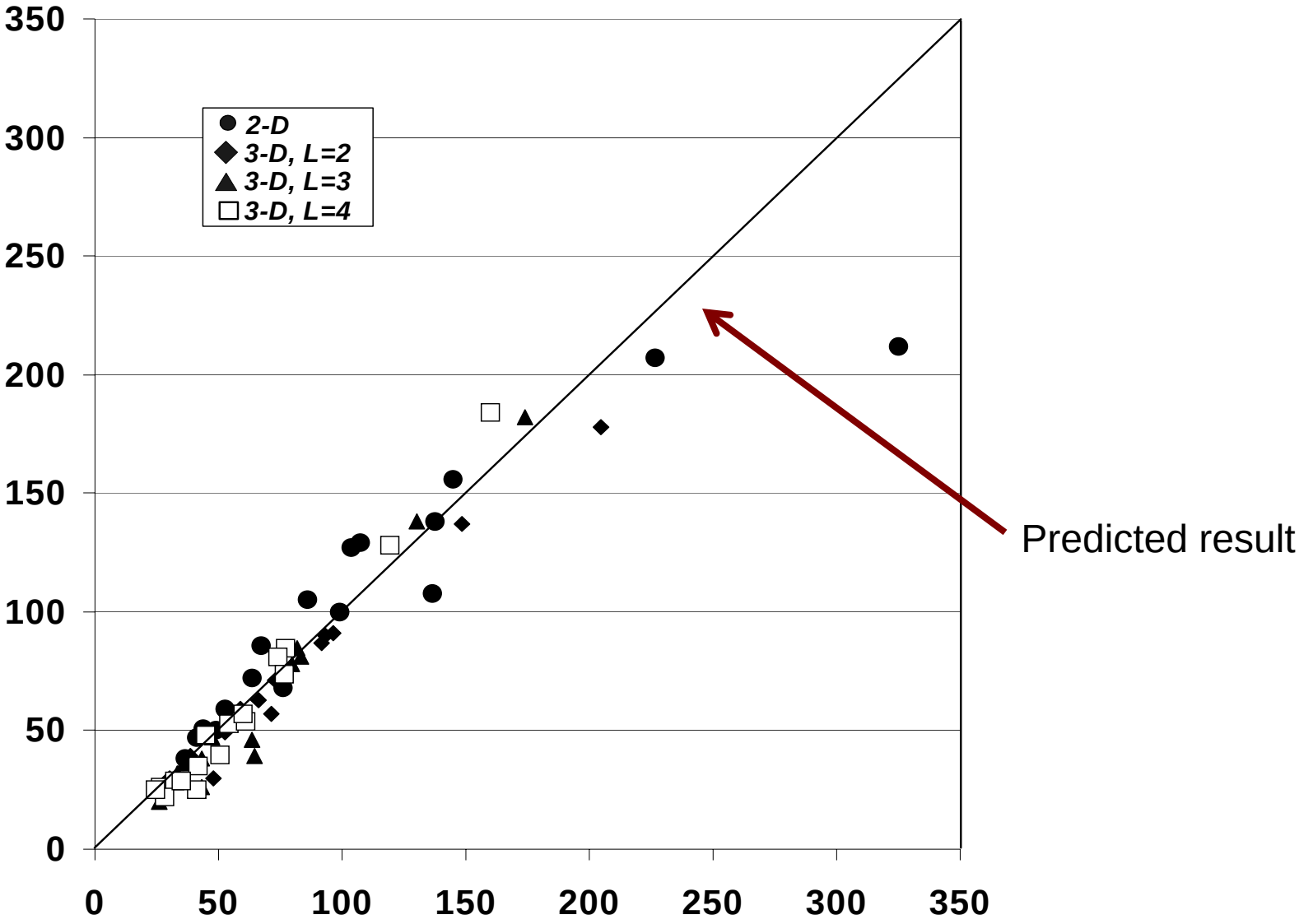
Experimental Results

- 3-D FPGA CAD flow implementation
  - Technology mapper and XDL generation with Xilinx tools.
  - 3-D placement and routing is implemented with C.
- 3-D FPGA Architecture
  - 40x40 tiles with 3 strata.
  - Intra-stratum wire segment of “DIRECT” and inter-strata wire segment of “VDIRECT”
- Benchmark circuits from LGSynth93 and ISPD2001

Required Number of Wires/Channel



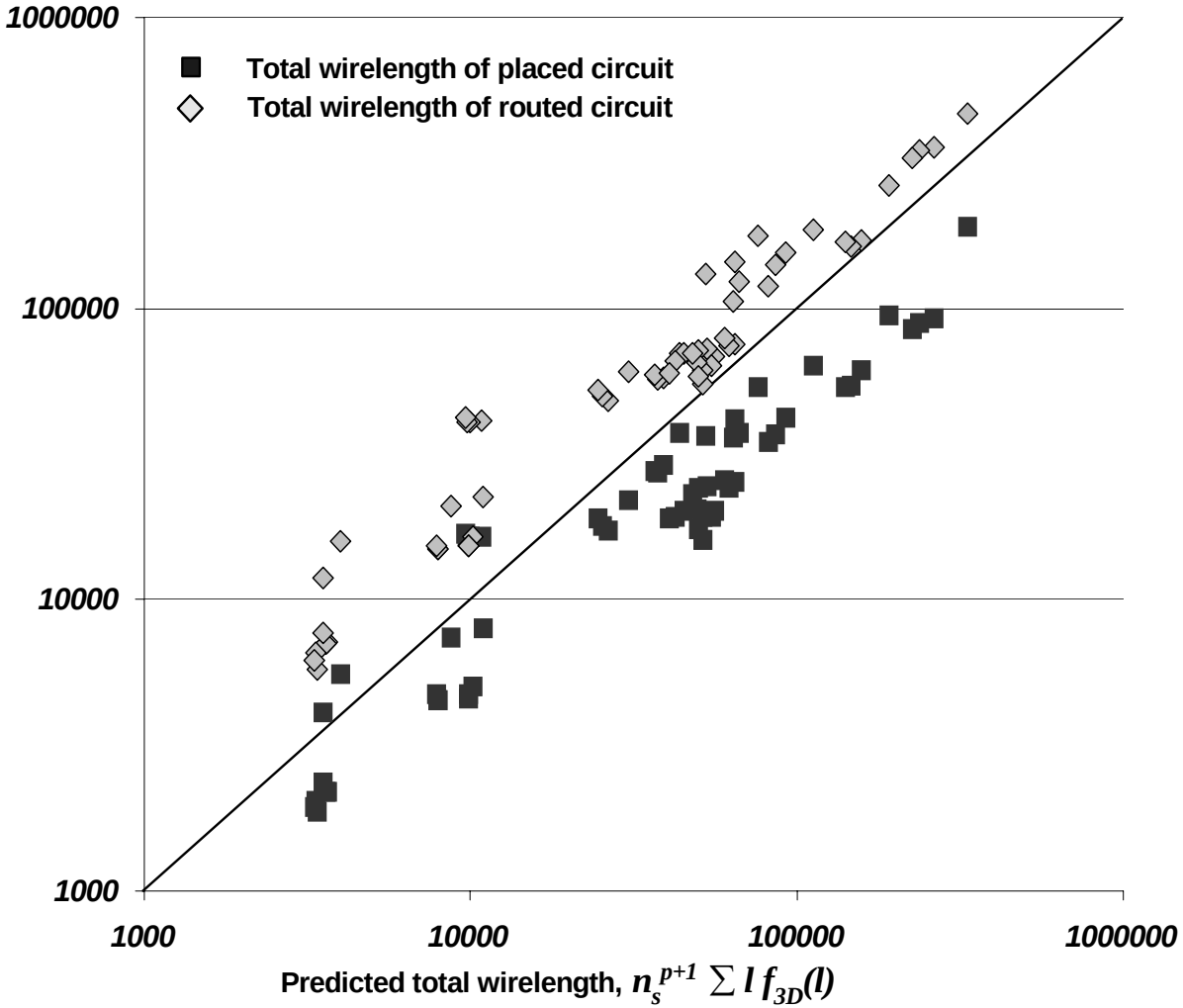
Prediction Results of Required # Wires/Channel



Error Sources

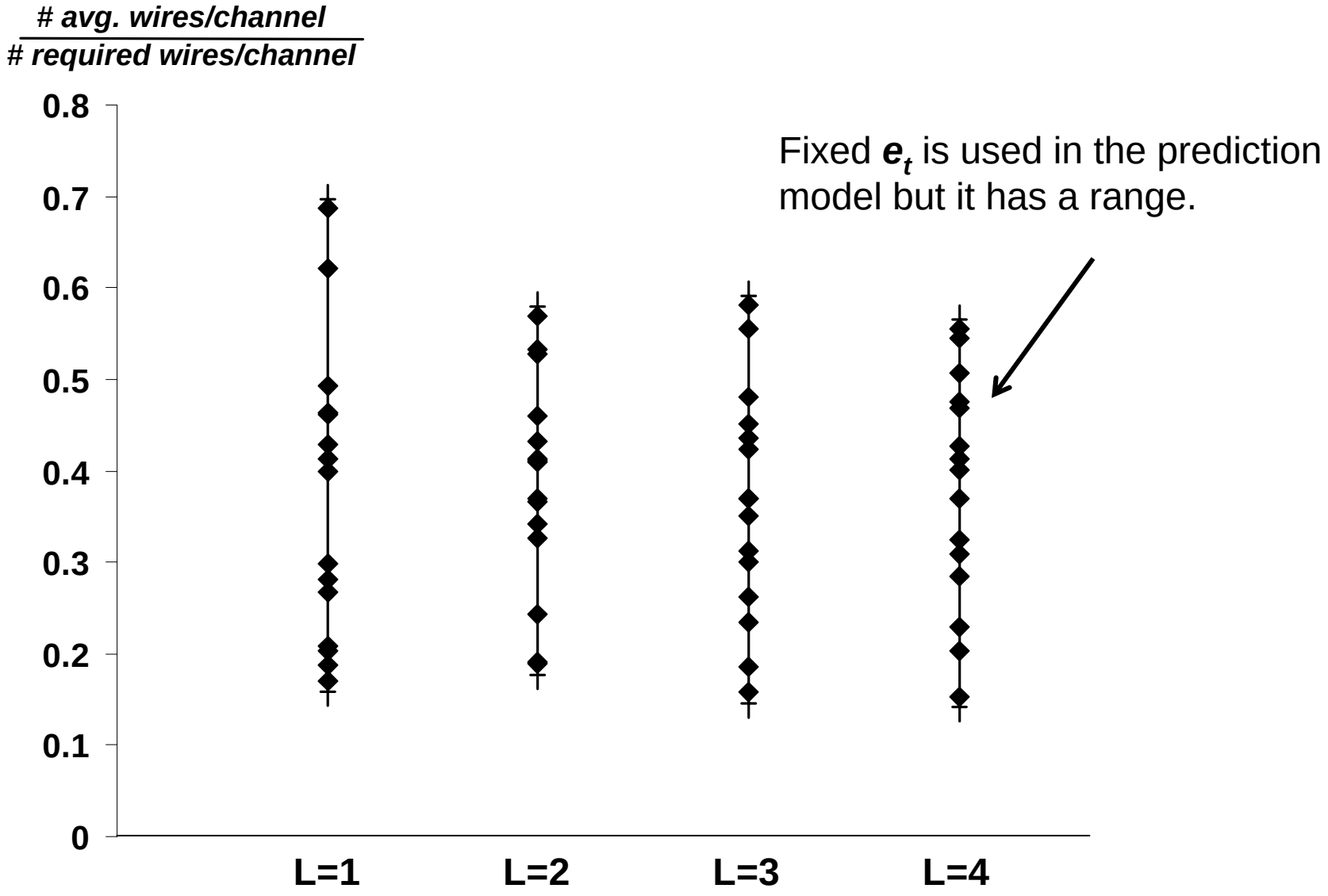
- Deviation in wirelength prediction is the error source.
- Variation of the utilization factor of routing tracks requires an equation for $\boldsymbol{e_t}$.
- Sensitivity of $\boldsymbol{n_s}$ is also an error source but it shows small variation around a fixed value.

Deviation in Total Wirelength

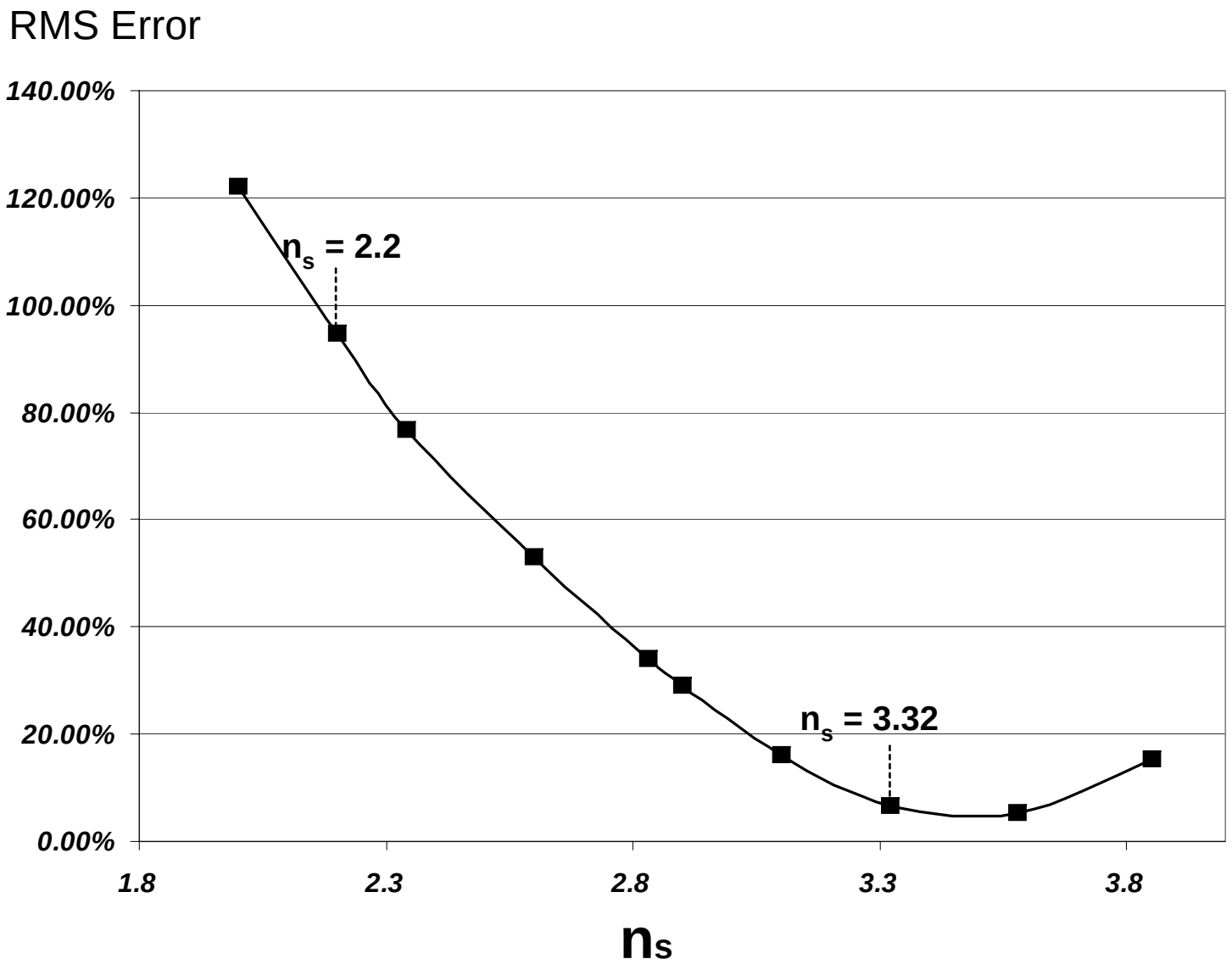


- Each net is routed sequentially with detours in global routing while the prediction model considers only point-to-point interconnection

Variation of e_t



Sensitivity of n_s



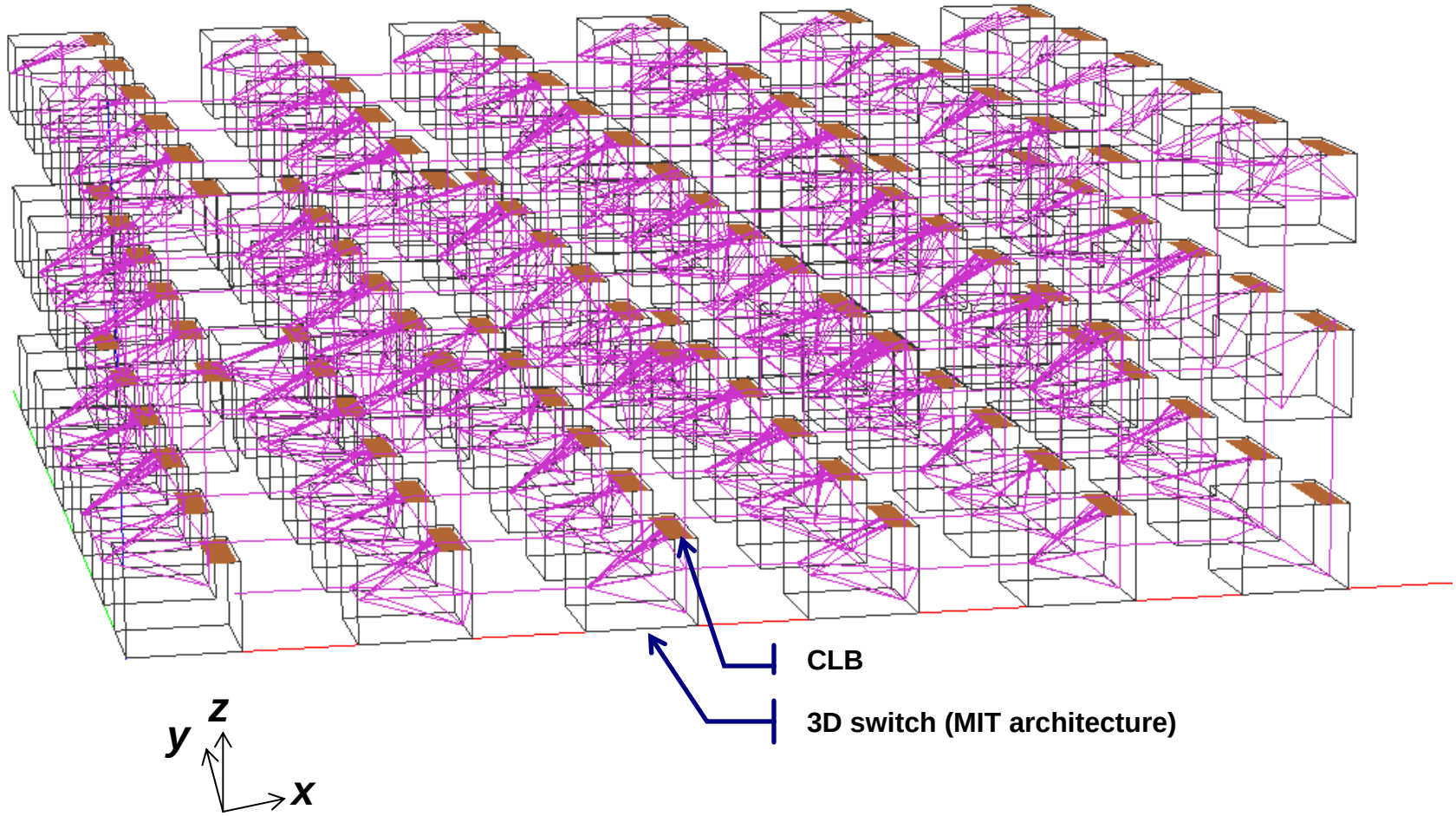
Conclusion

- We propose extended 3-D FPGA wire resource prediction model.
- 3-D FPGA architecture and a placement and routing tool are used to validate the prediction model.
- The required number of wires per channel of prediction model shows an acceptable error compared with that of experimental results.

Appendix

Placed and Routed Result

Visualization tool for 3D FPGA
for rgb_interp example on 3 strata, 6x6 tiles



Total Wirelength (m)

	2D	3D,L=2	3D,L=3	3D,L=4
addrgen	1.07	0.46	0.45	0.47
bigkey	4.37	4.09	4.38	4.22
clma	16.75	11.04	11.95	13.75
diffeq	1.81	1.03	1.14	1.30
dsip	2.58	2.73	2.83	1.98
elliptic	7.94	5.55	5.48	5.54
frisc	13.98	10.34	9.44	9.98
idct	7.40	4.72	5.15	5.40
mac1	8.56	4.91	4.84	5.12
mac2	28.39	23.45	22.50	22.50
matrix	1.11	0.56	0.59	0.63
rgb_interp	0.81	0.43	0.39	0.43
s38417	8.37	3.70	3.85	4.61
s38584	10.93	4.79	6.30	6.33
tseng	1.79	0.93	0.88	1.05
vp2	3.90	3.44	3.21	3.80