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The Impact of Interstratal Interconnect Density on the Performance of Three-Dimensional Integrated Circuits

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Philips Research Leuven
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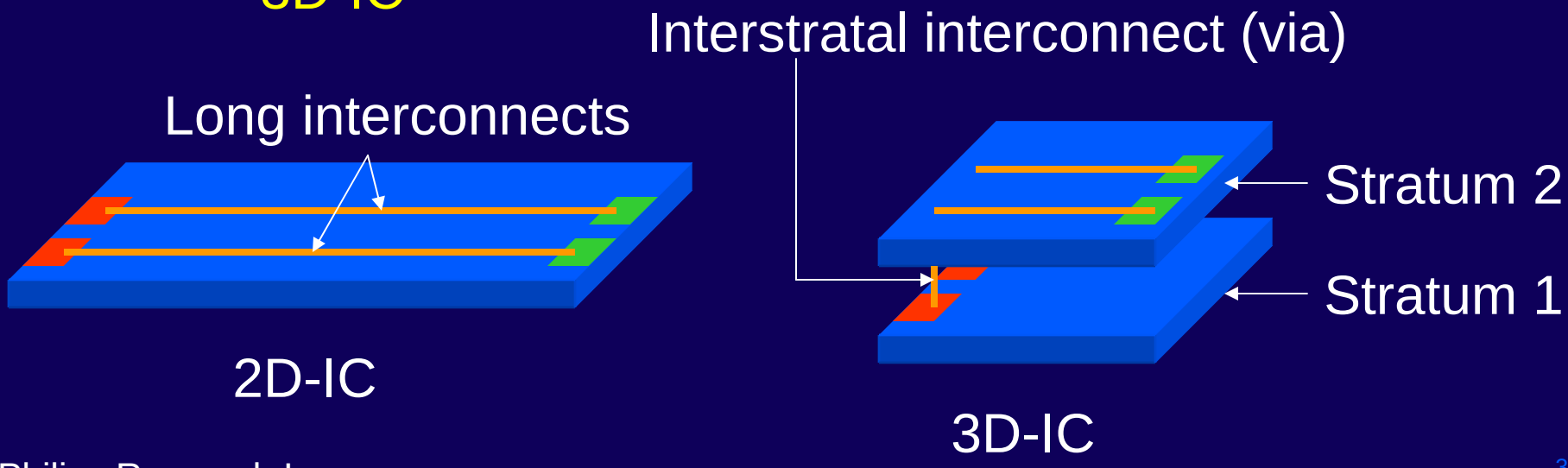
Outline

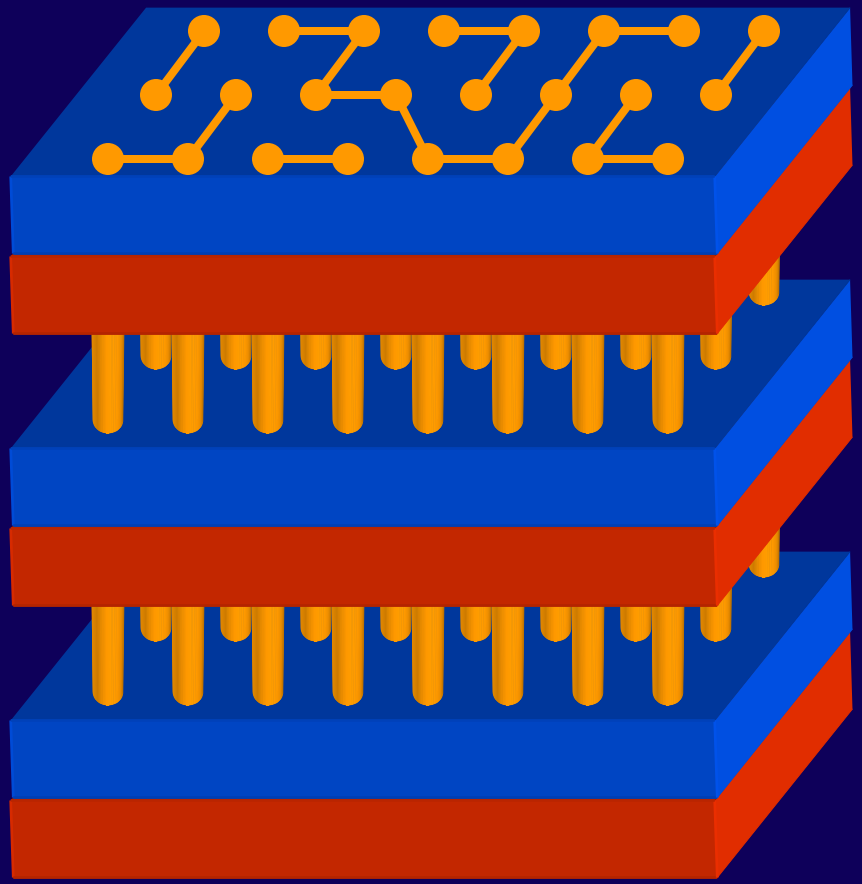
- Introduction
- Method for system-level performance evaluation
- Wire-length distributions
- Results
  - System-level performances of 2D, ideal, semi-ideal and realistic 3D-ICs
  - Recently published data + benchmarking
- Conclusions

Introduction

- Signal delay, high power consumption are the problems associated with long, thin, dense interconnects
- Solutions under investigation
  - Optical interconnect, carbon nanotubes…
  - 3D-IC



Interconnection issues in 3D-IC #1



High-aspect-ratio through-wafer vias

Misalignment between device layers

Interconnection issues in 3D-IC #2

Example of state-of-the-art die-to-die via dimensions

- Via diameter: ~5µm
- Via height: ~50µm
- Via pitch:~10µm

45-nm CMOS cell size: ~1.5µm x 1.5µm

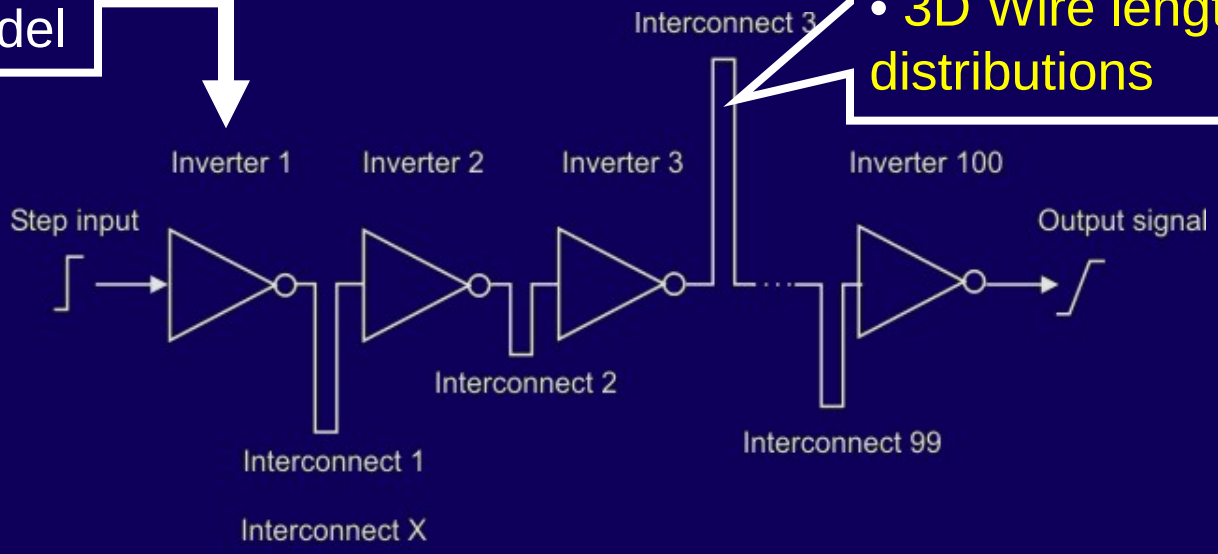
Vertical routing in a 3D-IC at 45-nm node is limited

What are the consequences on 3D-IC performance

Method for system-level performance evaluation

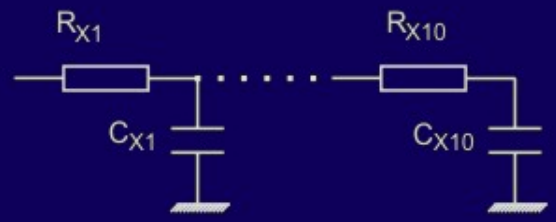
45-nm CMOS compact model

- 45-nm interconnect compact model
- 3D Wire length distributions



- 100 ivx1x critical path
- Delay, dynamic switching energy
- 1000 trials

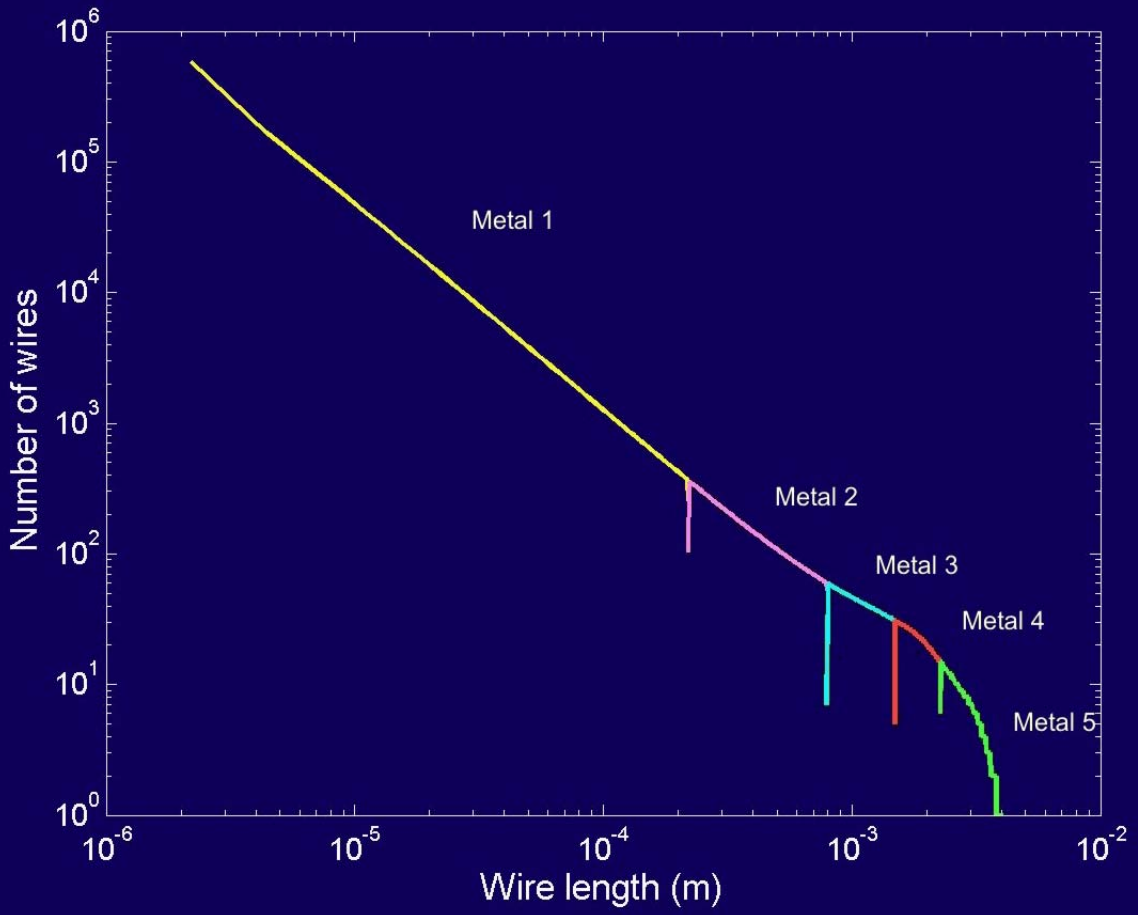
Interconnect X



$R_{XX} = 0.1R_X$

$C_{XX} = 0.1C_X$

Example of a wire-length distribution



902,500 gates
CMOS045
5 metal levels

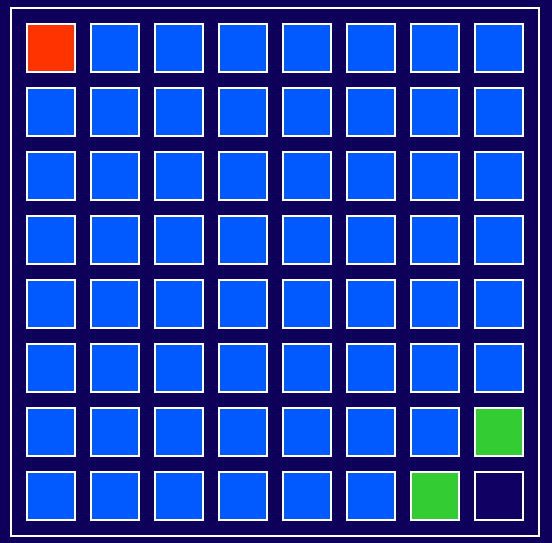
2D wire-length distribution – Davis model

$$f_{2D}(l) = \Gamma M_{2D}(l) I_{2D}(l)$$

Number of gate pairs separated by distance l

Expected number of interconnects between two gates

l = 13 gate pitch



Block A – N_{A2D} gates

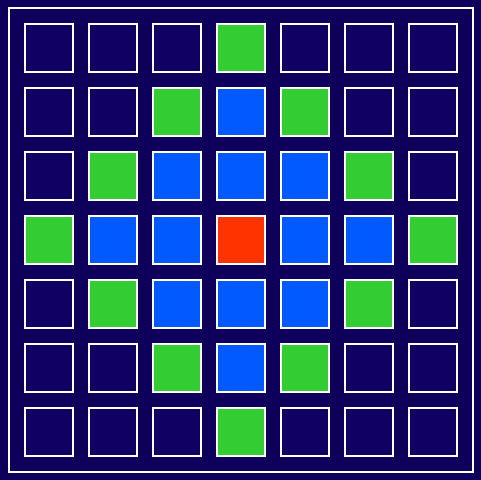
Block B – N_{B2D} gates

Block C – N_{C2D} gates

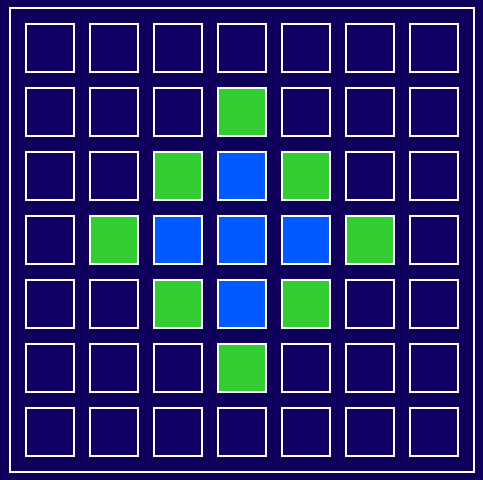
J.A. Davis, V.K.De and J.D.Meindl, IEEE Transactions on Electron Devices, Vol. 45, No. 3, p. 580, (1998)

3D wire-length distribution – Rahman model

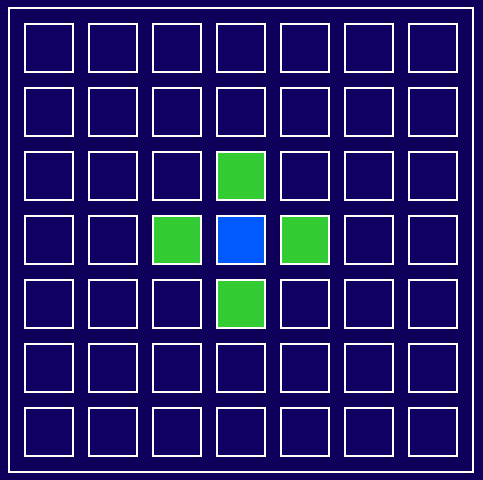
Stratum 1



Stratum 2



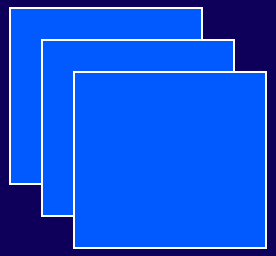
Stratum 3

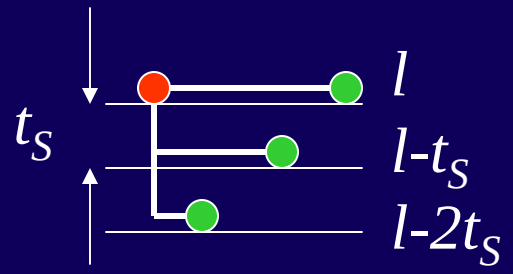


Block A – N_{A3D} gates

Block B – N_{B3D} gates

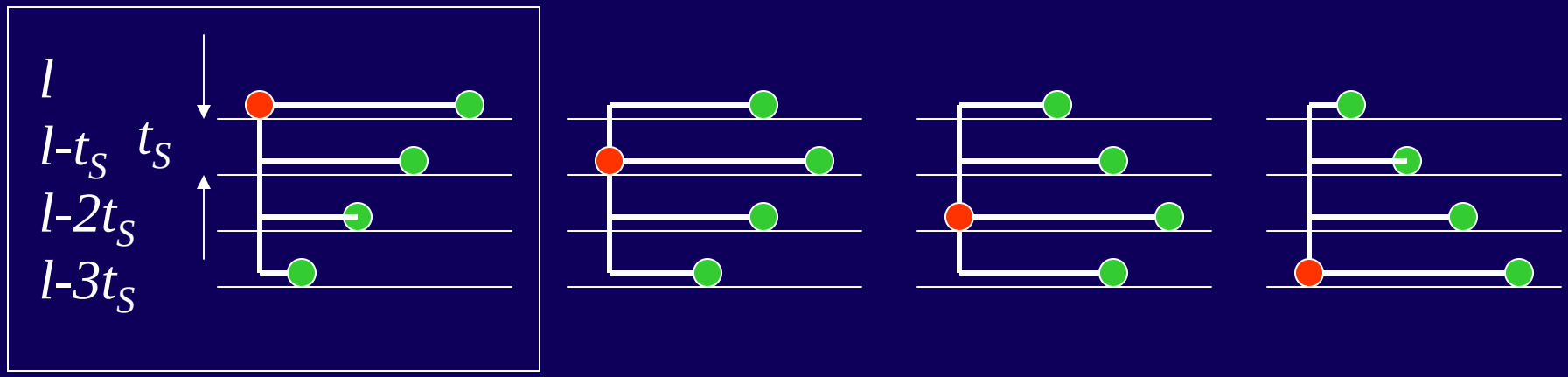
Block C – N_{C3D} gates





A. Rahman and R. Reif, IEEE Transactions on VLSI Systems, Vol. 8, No. 6, p. 671, (2000)

3D wire-length distribution – Rahman model



Average values for $N_{A,\,B,\,C}$

$$N_{A3D} = 1$$

$$N_{B3D}(l) \approx \frac{1}{S}\begin{bmatrix} N_{B2D}(l) + 2N_{B2D}(l-t_S)u(l-t_S) + \ldots + 2N_{B2D}(l-(S-1)t_S)u(l-(S-1)t_S) + \\ N_{B2D}(l) + 2N_{B2D}(l-t_S)u(l-t_S) + \ldots + 2N_{B2D}(l-(S-2)t_S)u(l-(S-2)t_S) \\ + \ldots + N_{B2D}(l) \end{bmatrix}$$

$$N_{C3D}(l) \approx \frac{1}{S}\begin{bmatrix} N_{C2D}(l) + 2N_{C2D}(l-t_S)u(l-t_S) + \ldots + 2N_{C2D}(l-(S-1)t_S)u(l-(S-1)t_S) + \\ N_{C2D}(l) + 2N_{C2D}(l-t_S)u(l-t_S) + \ldots + 2N_{C2D}(l-(S-2)t_S)u(l-(S-2)t_S) \\ + \ldots + N_{C2D}(l) \end{bmatrix}$$

A. Rahman and R. Reif, IEEE Transactions on VLSI Systems, Vol. 8, No. 6, p. 671, (2000)

Observations

Observation 1: Transformation of Rahman model

$$N_{B3D}(l) = N_{B2D}(l) + \frac{1}{S}\sum_{i=1}^{S-1}\left[2(S-i)N_{B2D}(l-it_s)u(l-it_s)\right]$$

$$N_{C3D}(l) = N_{C2D}(l) + \frac{1}{S}\sum_{i=1}^{S-1}\left[2(S-i)N_{C2D}(l-it_s)u(l-it_s)\right]$$

Contribution of the 3rd dimension

Observation 2: In reality

Limited number of interstratal interconnects

↓

Contribution of the 3rd dimension will be much less

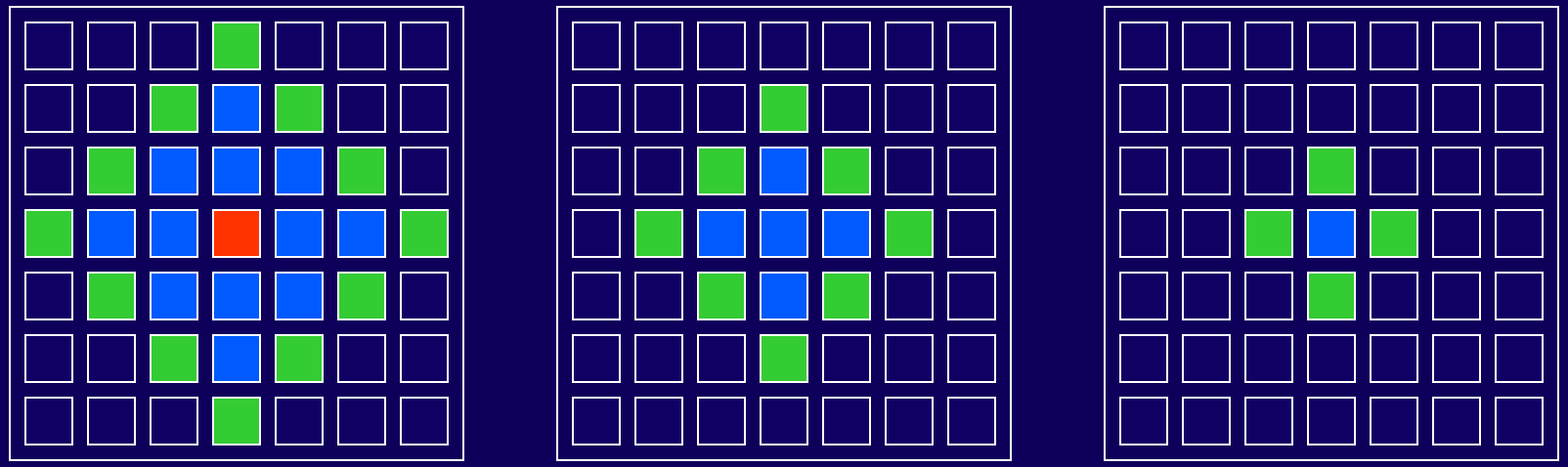
↓

Concept of probability of connection to other strata

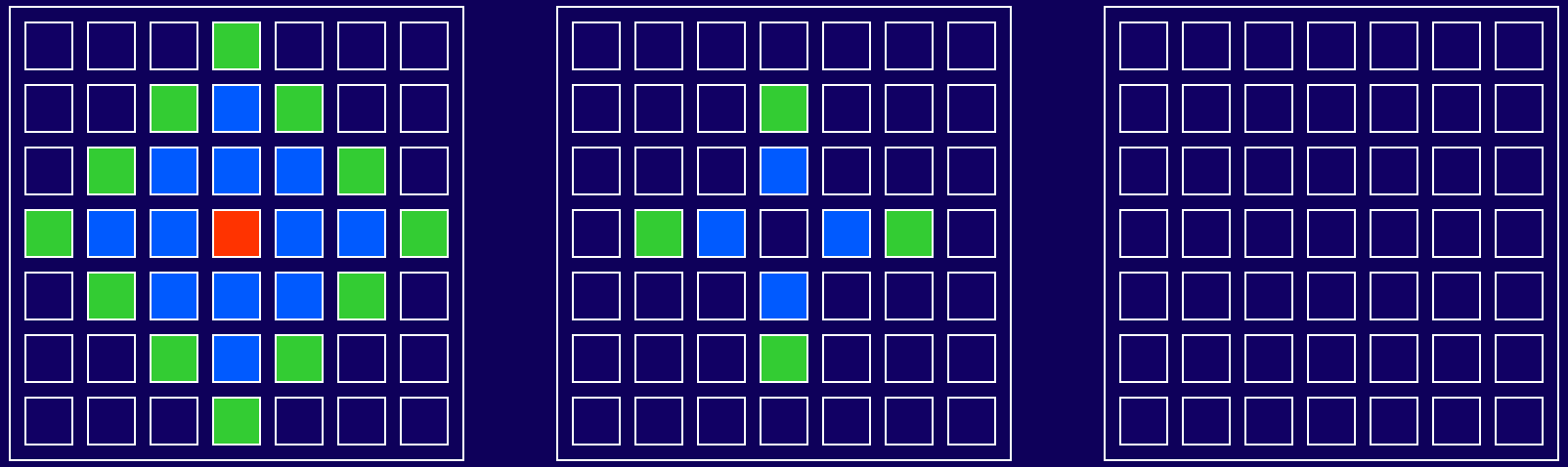
Observation 2: Example

Stratum 1 | Stratum 2 | Stratum 3

Ideal



Reality
(limited number of interstratal interconnects)



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3D wire-length distribution – New model

$$N_{A3D} = 1$$

Remote stratum has remote interconnection chance

$$N_{B3D}(l) = N_{B2D}(l) + \frac{1}{S}\sum_{i=1}^{S-1}\left[2(S-i)N_{B2D}(l-it_s)u(l-it_s)P_{density}^{i}\right]$$

$$N_{C3D}(l) = N_{C2D}(l) + \frac{1}{S}\sum_{i=1}^{S-1}\left[2(S-i)N_{C2D}(l-it_s)u(l-it_s)P_{density}^{i}\right]$$

Chance to have a direct connection to the next stratum. This depends on the interstratal interconnect density

Examples

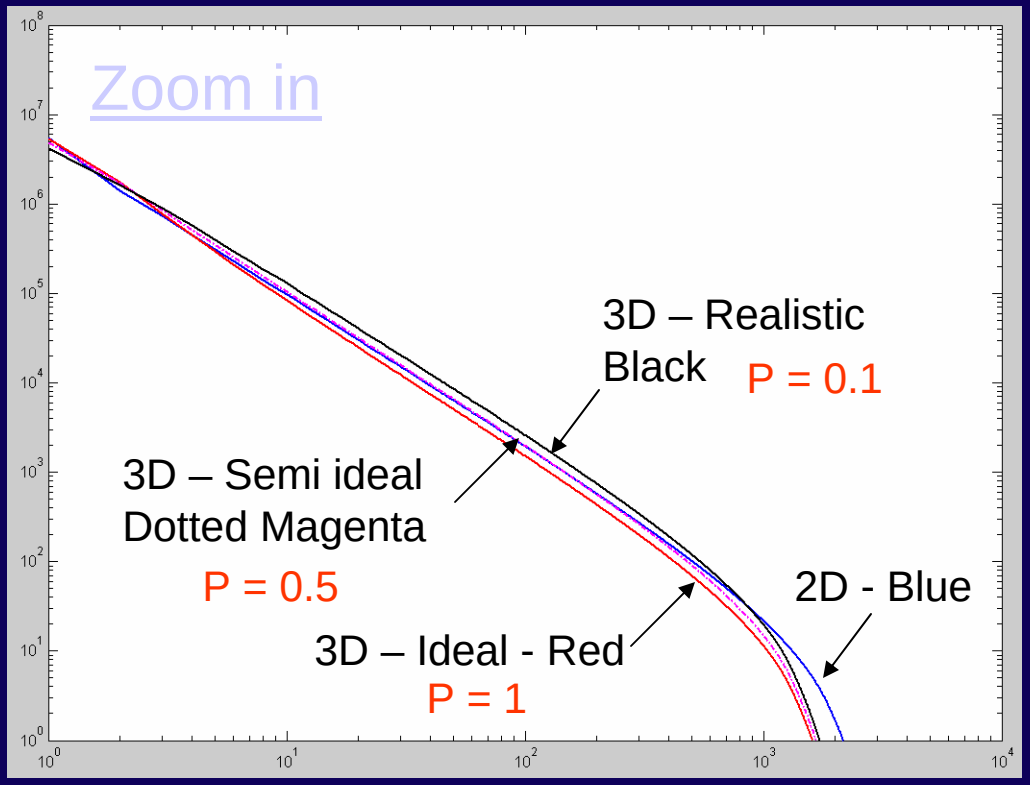
$P_{density}$ = 1 --- Ideal case, back to Rahman model
$P_{density}$ = 0.5 --- Semi-ideal case
$P_{density}$ = 0.1 --- Realistic case

CMOS045 dimensions → Interstratal interconnect pitch

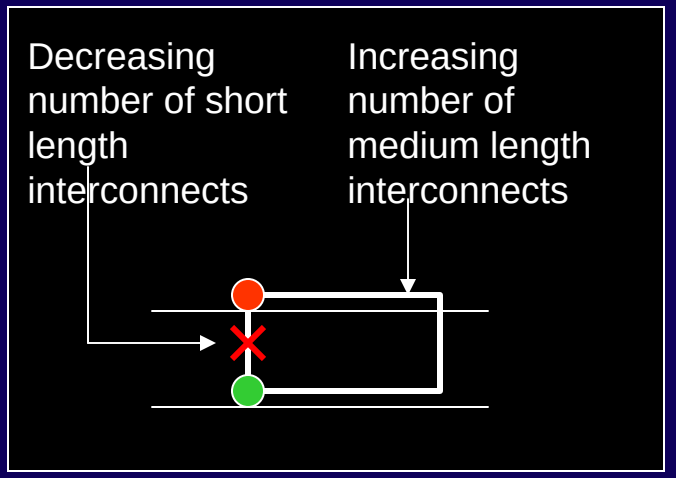
- $P_{density}$ = 1 --- Pitch ~ 1.5 µm
- $P_{density}$ = 0.5 --- Pitch ~ 3 µm
- $P_{density}$ = 0.1 --- Pitch ~ 15µm

Wire-length distributions of 2D, ideal, semi-ideal and realistic 3D-ICs

Wire-length distributions



- 3,500,000 gates
- p = 0.66, αk = 3
- t_S = 1 gate pitch
- 2 strata (3D)
- CMOS045



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45-nm CMOS compact model

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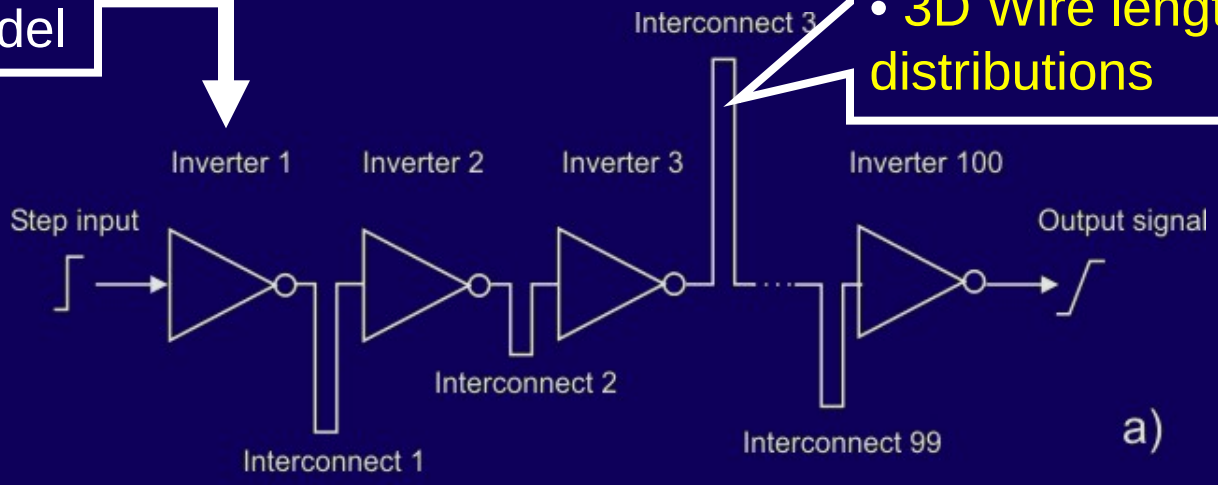
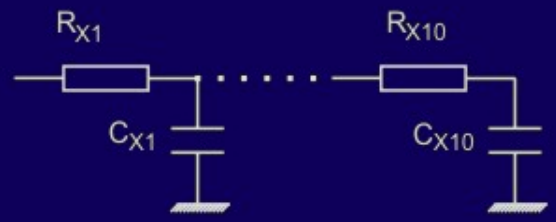


- 100 ivx1x critical path
- Delay, dynamic switching energy
- 1000 trials



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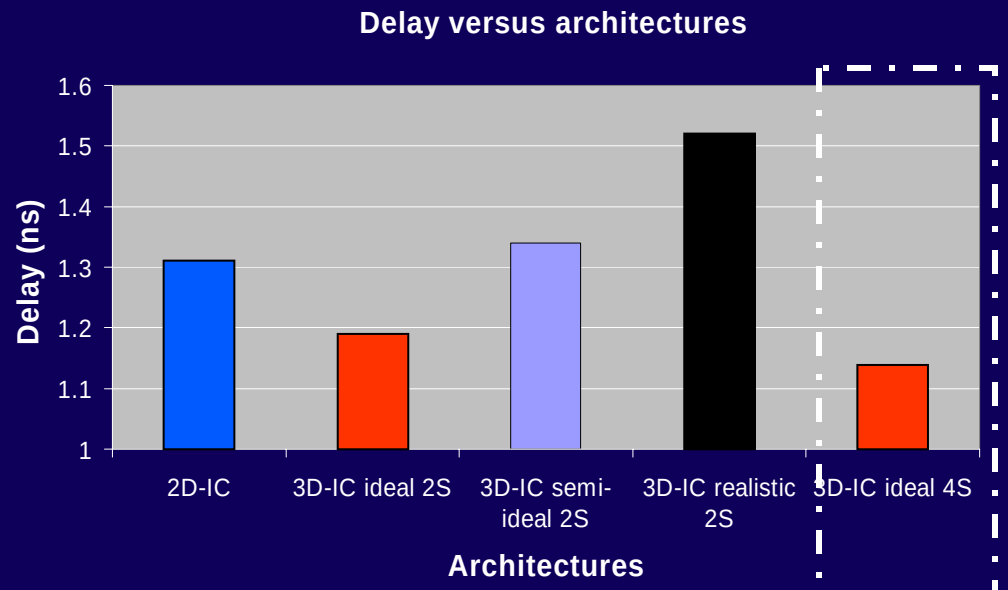
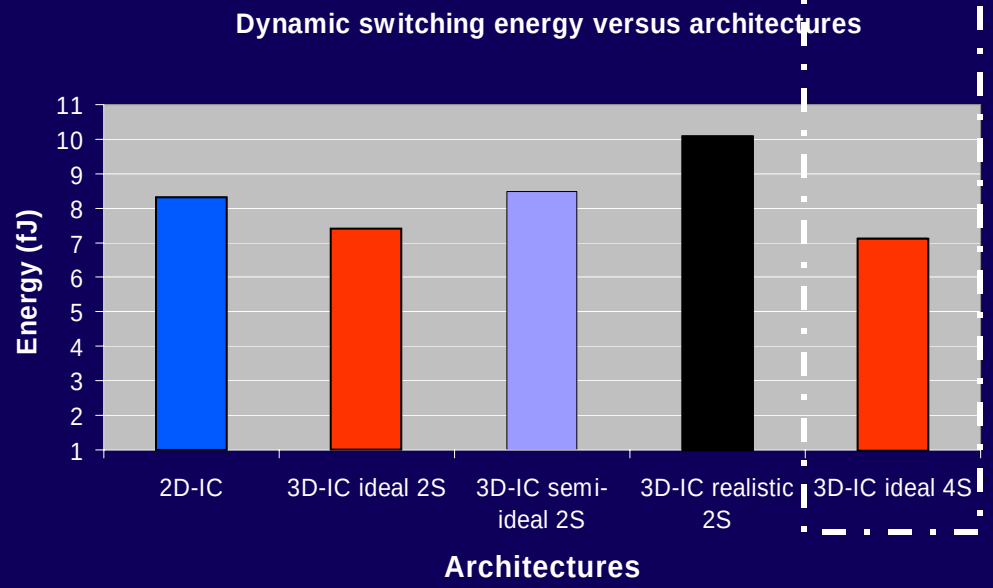
Results



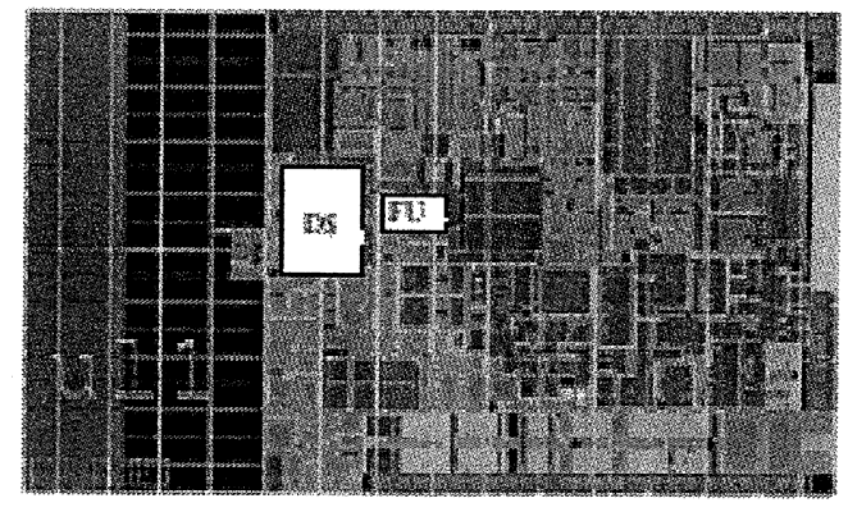


- Ideal 3D interconnect architecture only shows a modest performance improvement (approx. 10%)
- Realistic 3D interconnect architecture does not improve performance
- Increase number of strata does not significantly improve performance

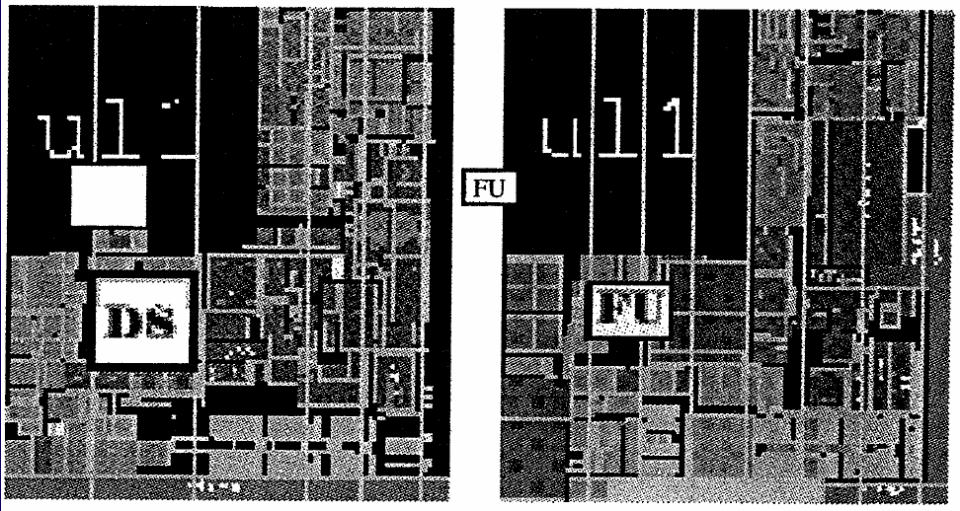
Recently proposed dimensions & properties for 45-nm CMOS

Recently published data on 3D-IC #1

Performance of 3D iA32 microprocessor



2D floor plan of a deeply pipelined iA32 core

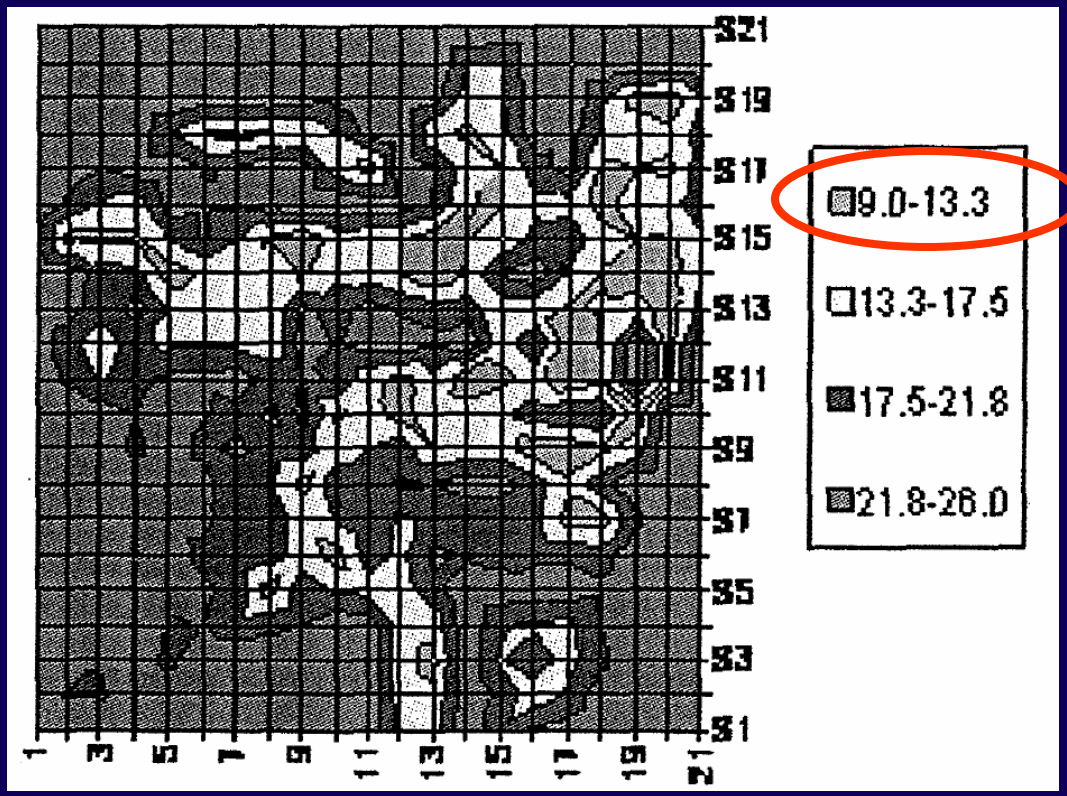


3D floor plan of a deeply pipelined iA32 core

D. Nelson et al, IEEE International Conference of Computer Design ICCD2004, Oct 2004, San Jose, CA

Recent published data on 3D-IC #2

Performance of 3D iA32 microprocessor



Performance improvement

Speed: 15%
Power: 15%

Required die-to-die via pitch (µm) density in 90nm process

D. Nelson et al, IEEE International Conference of Computer Design ICCD2004, Oct 2004, San Jose, CA

Benchmarking

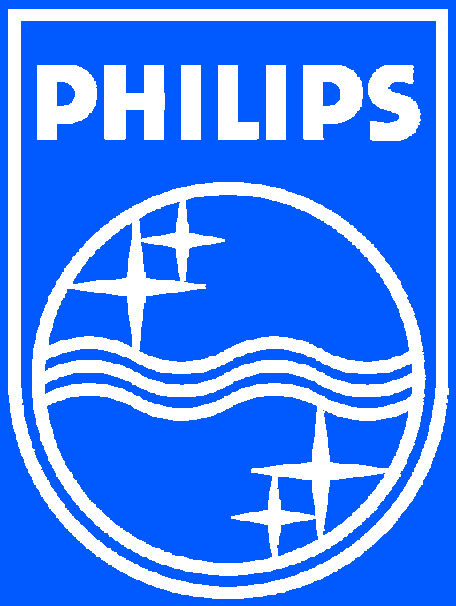
	Our analysis	Published data
Technology node	45-nm	90-nm
Circuit type	Random logic network	Deeply pipelined microprocessor
Number of device layers	2	2
Via pitch density	1.5-µm; 3-µm; 15-µm	Minimum: 9 µm
Performance improvement	1.5-µm via pitch: 10% 3-µm via pitch : - 0% 15-µm via pitch: -15%	15%

Conclusions

- Interstratal interconnect density plays a crucial role in determining the performance of 3D random logic networks
- It is indicated that serious efforts need to be spent on realizing high density interstratal interconnect for CMOS045 and smaller nodes in order to benefit from 3D architecture
- Increasing the number of strata does not significantly increase the performance of a 3D-IC

Acknowledgement

- Virtual Technology Project members:
  - Aatish Kumar
  - Anco Heringa
  - Manish Garg
  - Laurent Le Cam
  - Gerben Doornbos
  - Ranick Ng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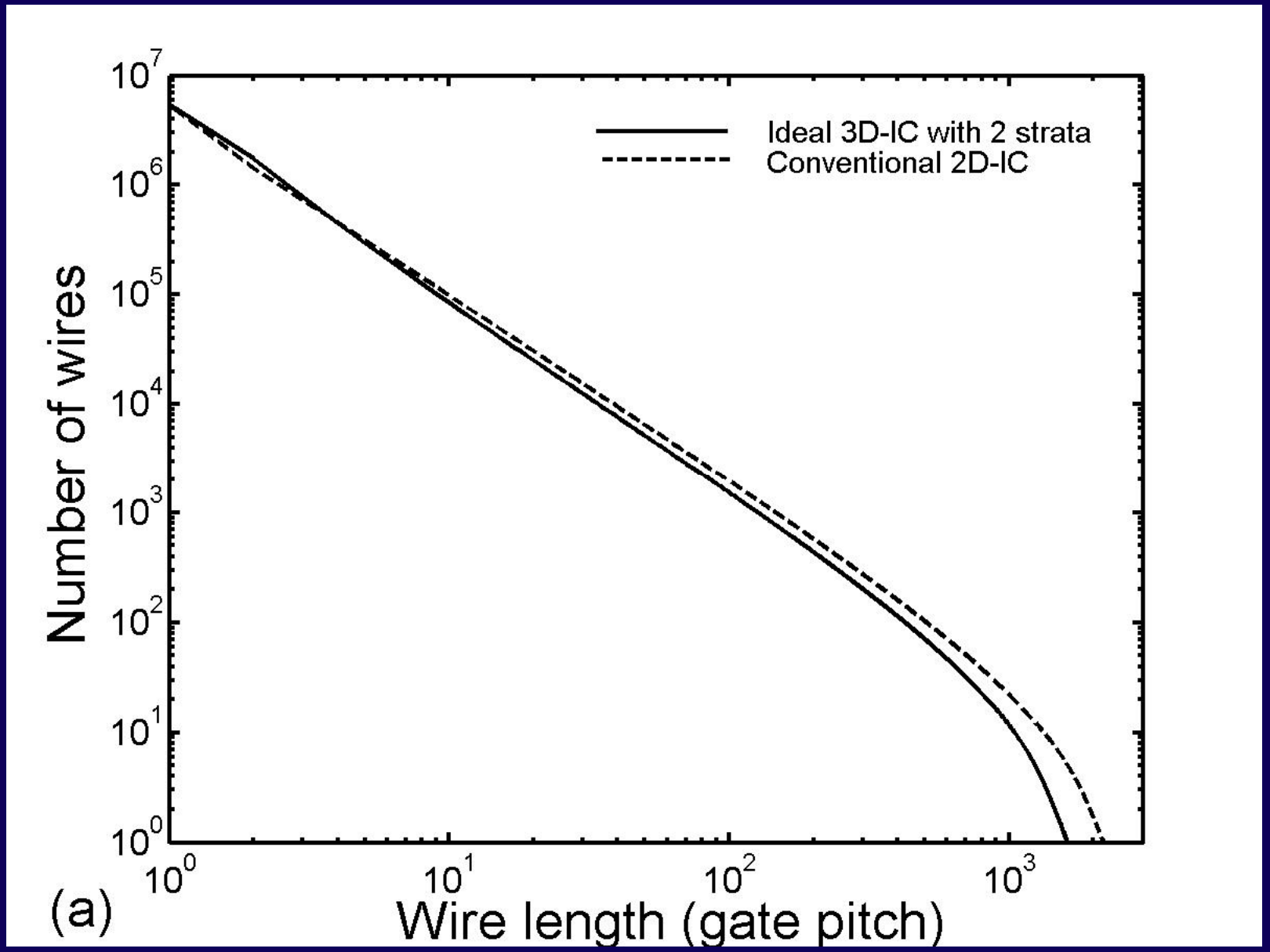
3D wire-length distributions



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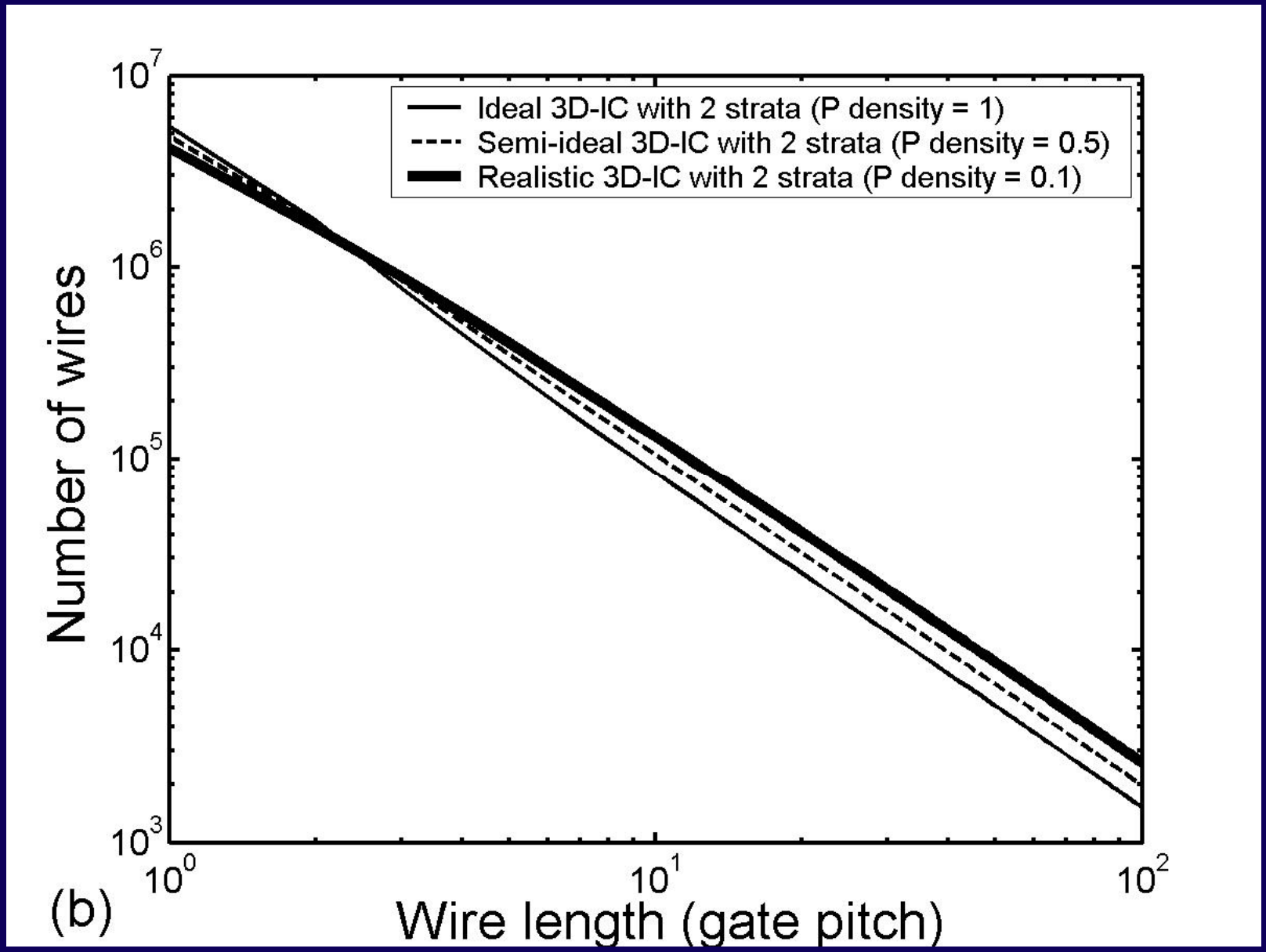

3D wire-length distributions