Thomas J. Watson Research Center

Statistical Analysis & Optimization in the Presence of Gate and Interconnect Delay Variations

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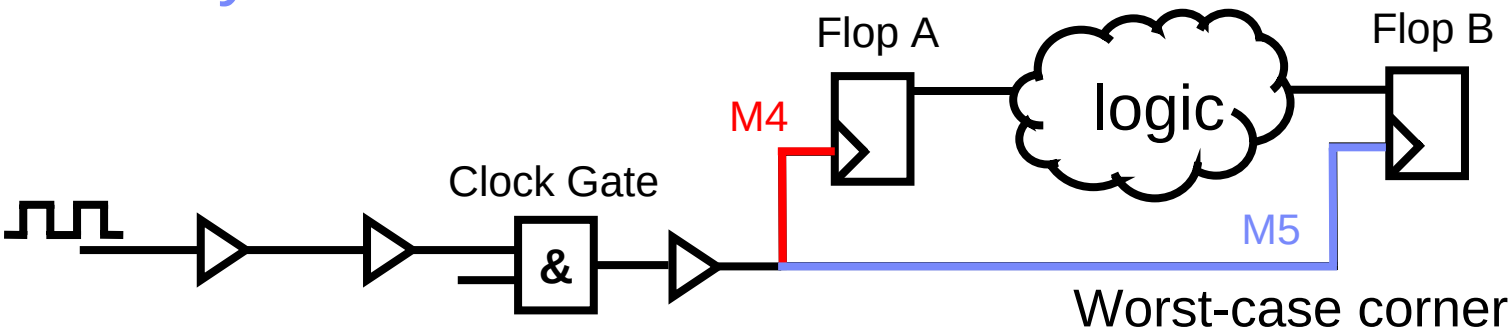
Acknowledgements

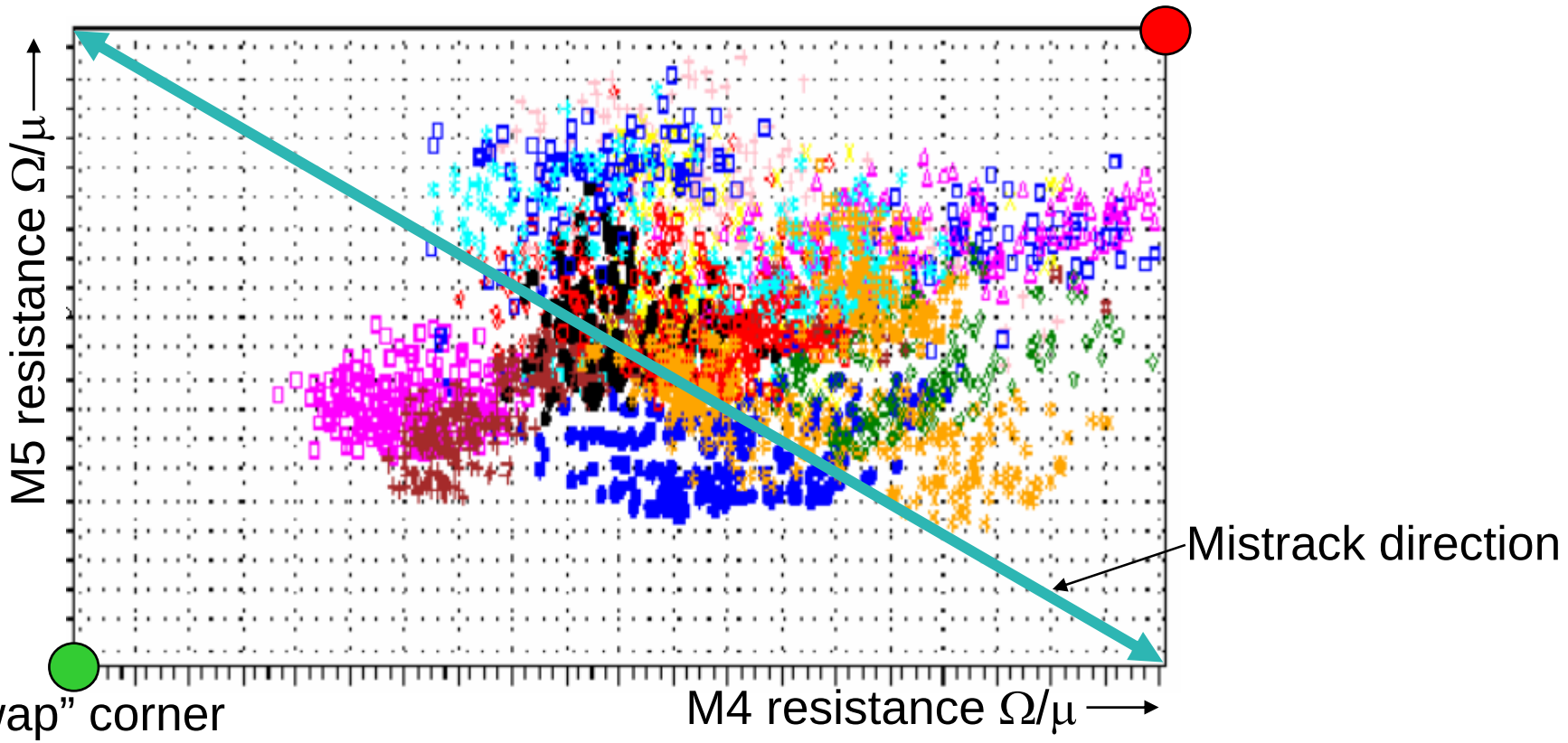
- Peter Habitz of IBM Burlington
- The extended statistical timing and optimization team at IBM Yorktown, Fishkill, Burlington and Poughkeepsie

Focus

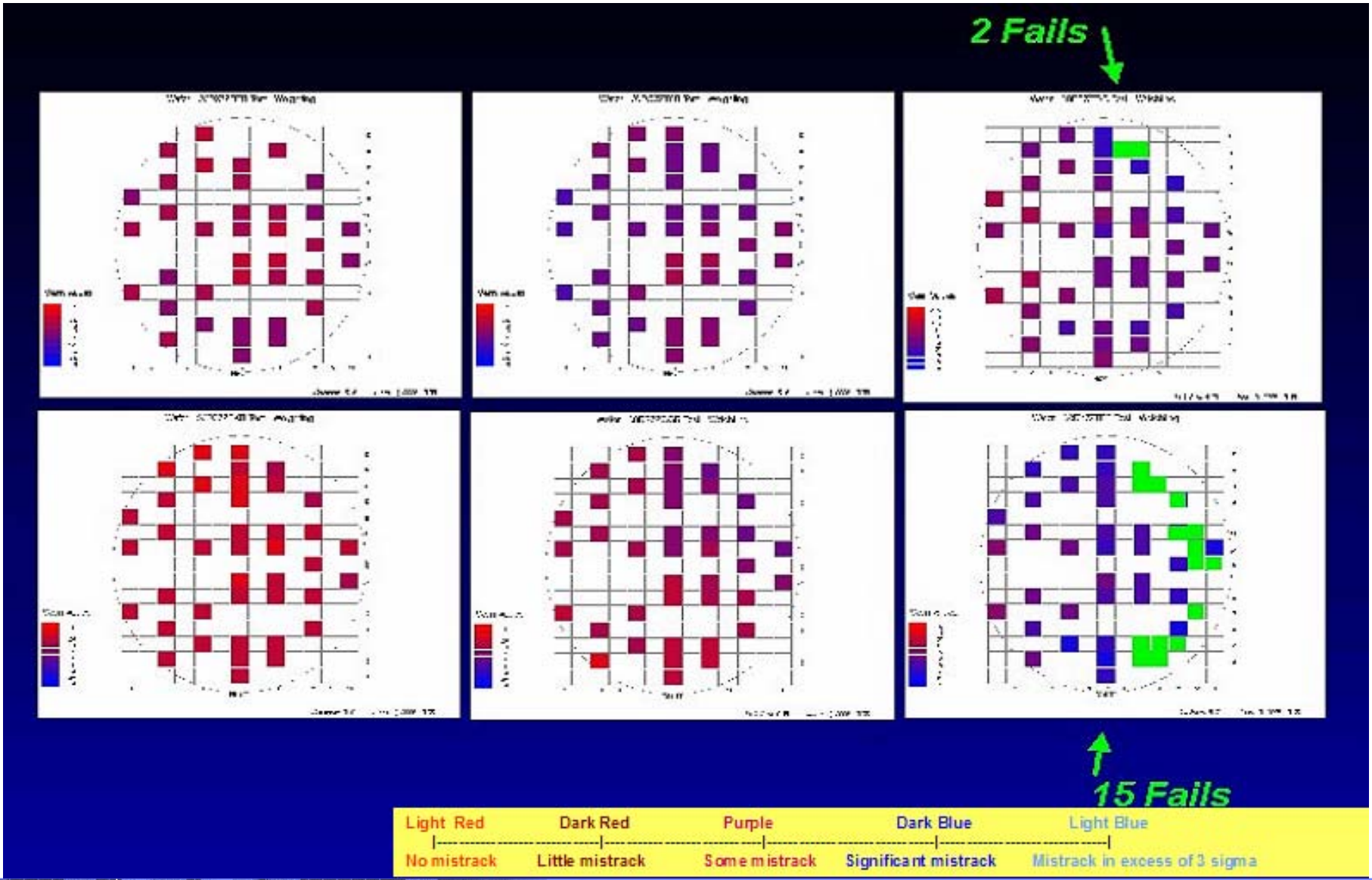
- CLIP ≅ SLIP?
- Focus on on-chip interconnect variability
- Topics
  - Case study
  - Origin of variability
  - Dealing with variability: new challenges in
    - timing
    - extraction
    - robust design
    - optimization
    - manufacturing
    - testing
  - Conclusions

Case study: 180 nm ASIC

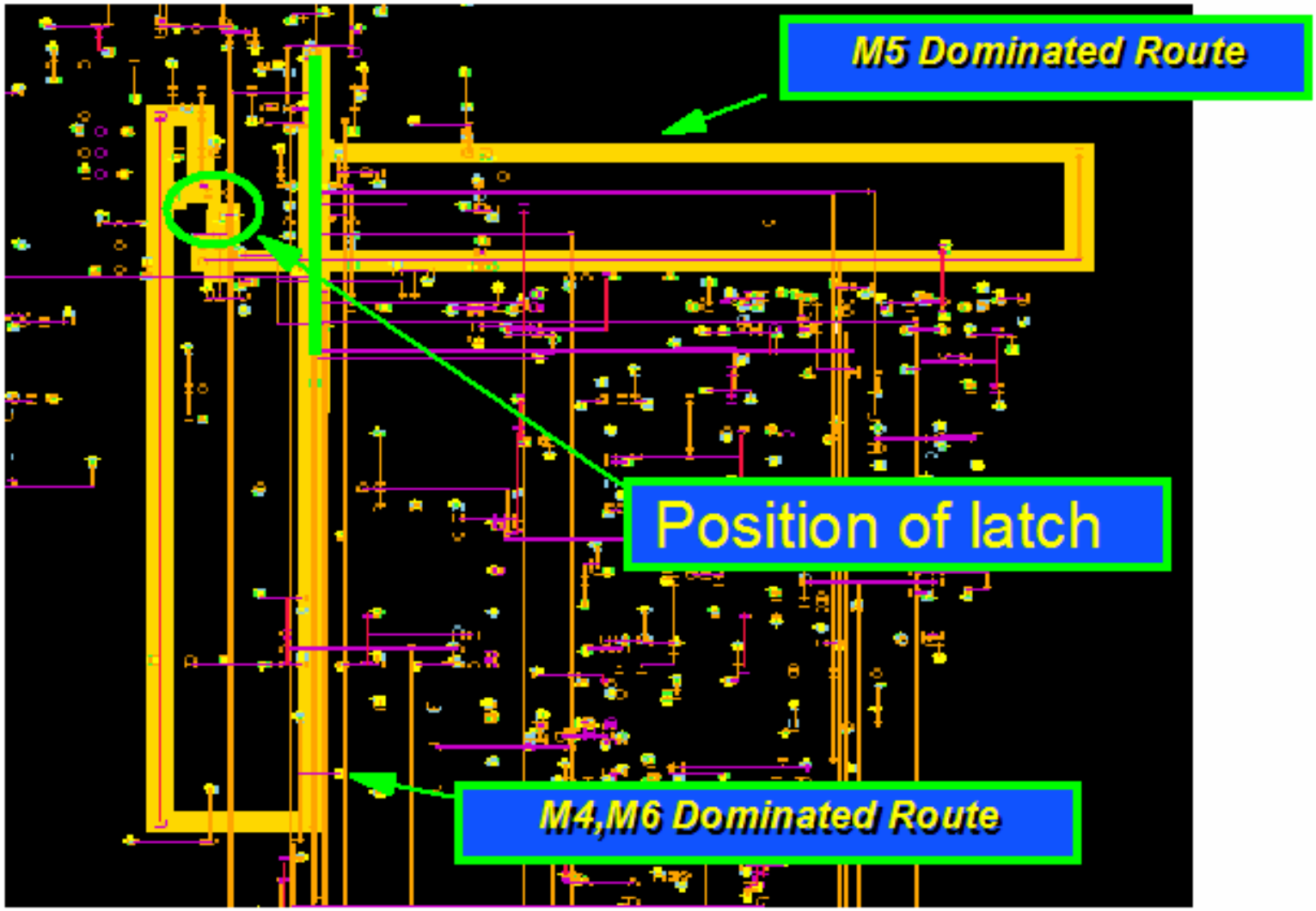




Case study wafers



Case study layout



Case study lessons

- Alternative statement of Murphy's Law: "Variability exacerbates poor design"
- Need to cover 2^n BEOL corners, not 2
- At what technology are statistical techniques necessary?
- Why is wire variability specially important?
  - changes both gate and wire delay
  - not easy to predict which is the worst corner
  - wire delay and coupling effects play a significant role in determining ultimate performance

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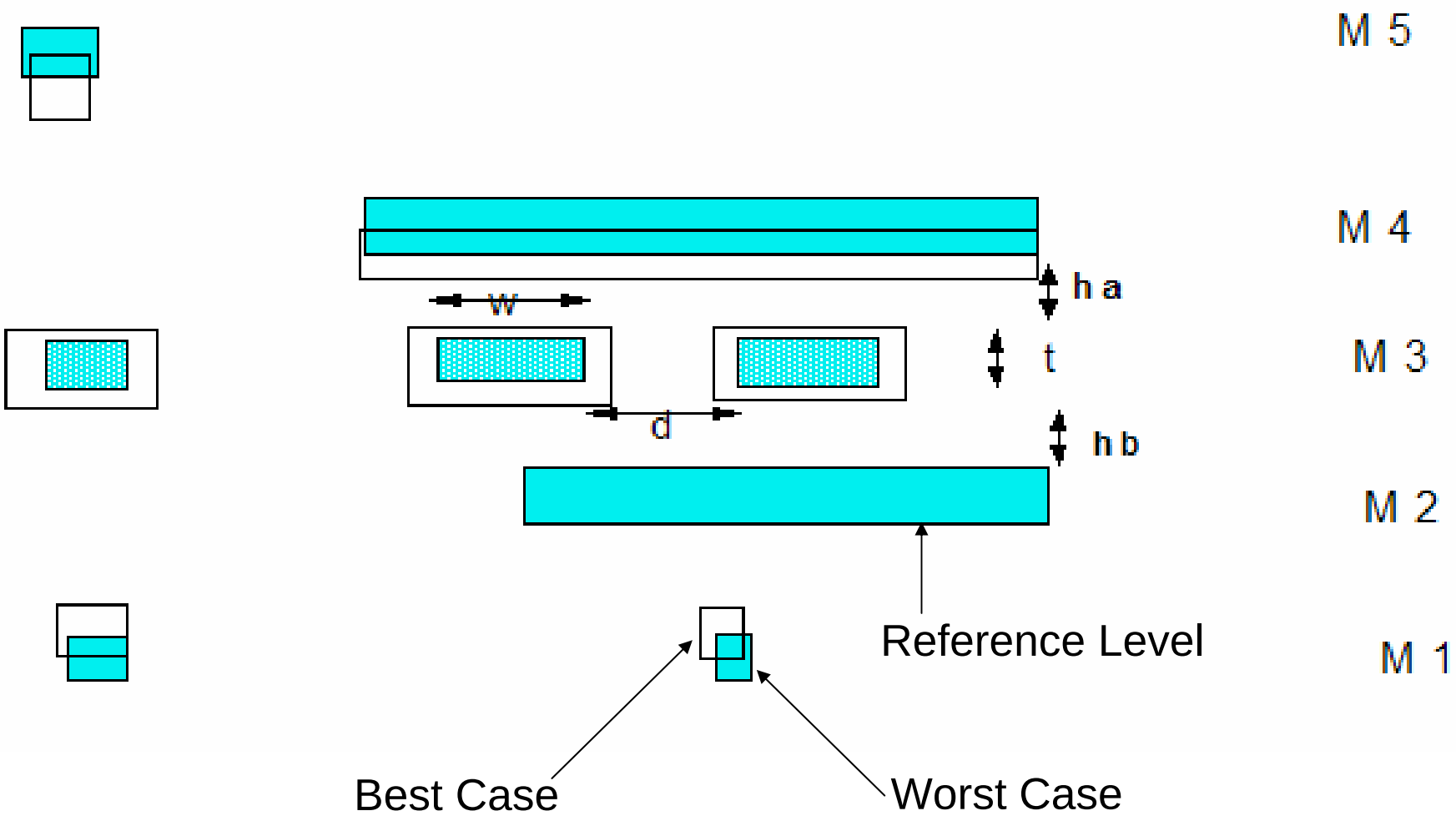
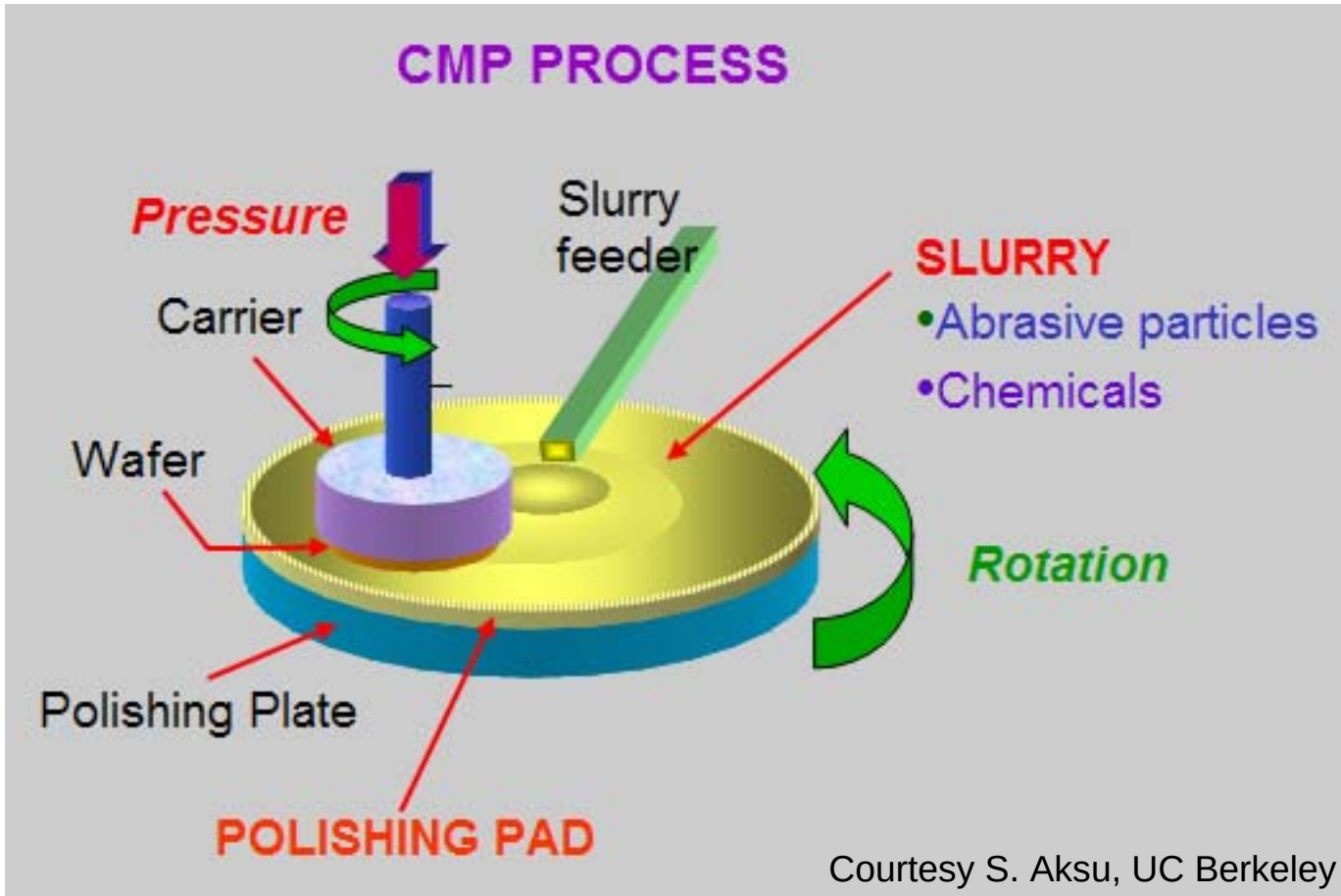
Variability from geometry



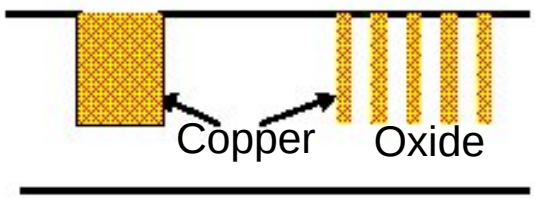
Variability from Chemical Mechanical Polishing



- CMP machine with rotational platen
- Notice that chips on the outside of the wafer move more

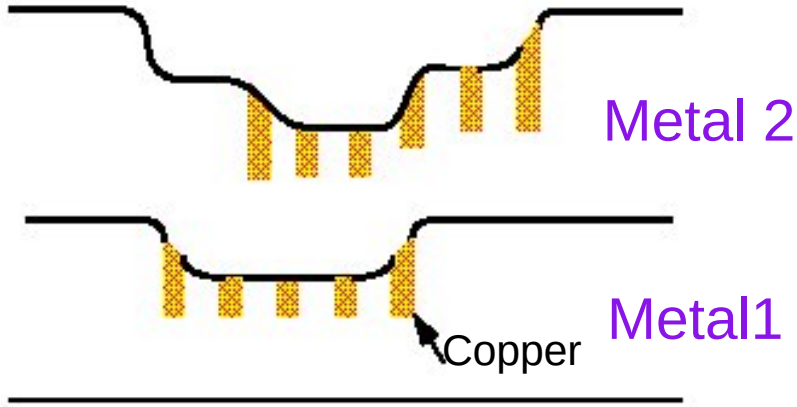
CMP effects

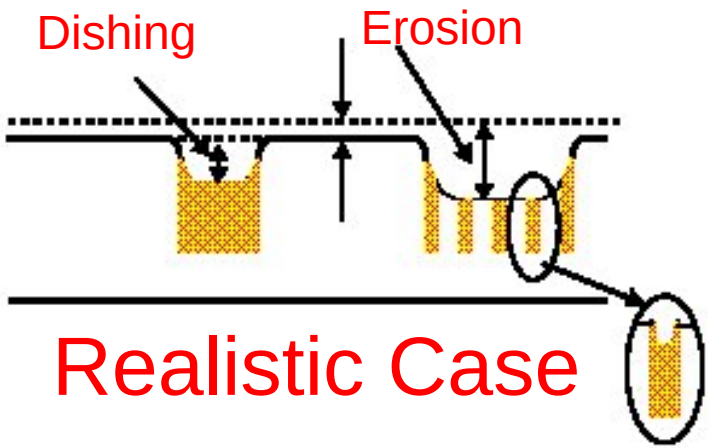
Single Level



Ideal Case

Multi Level

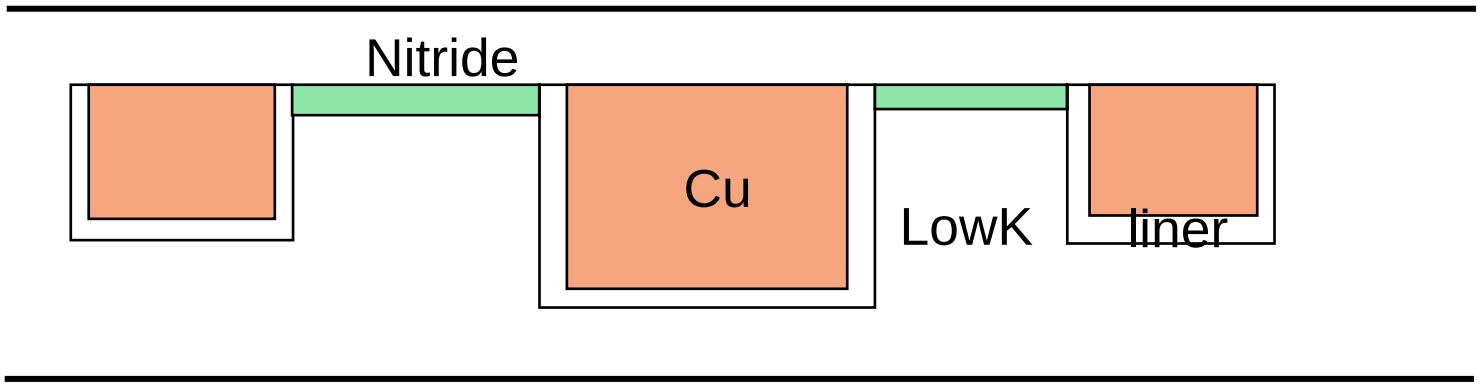




Realistic Case

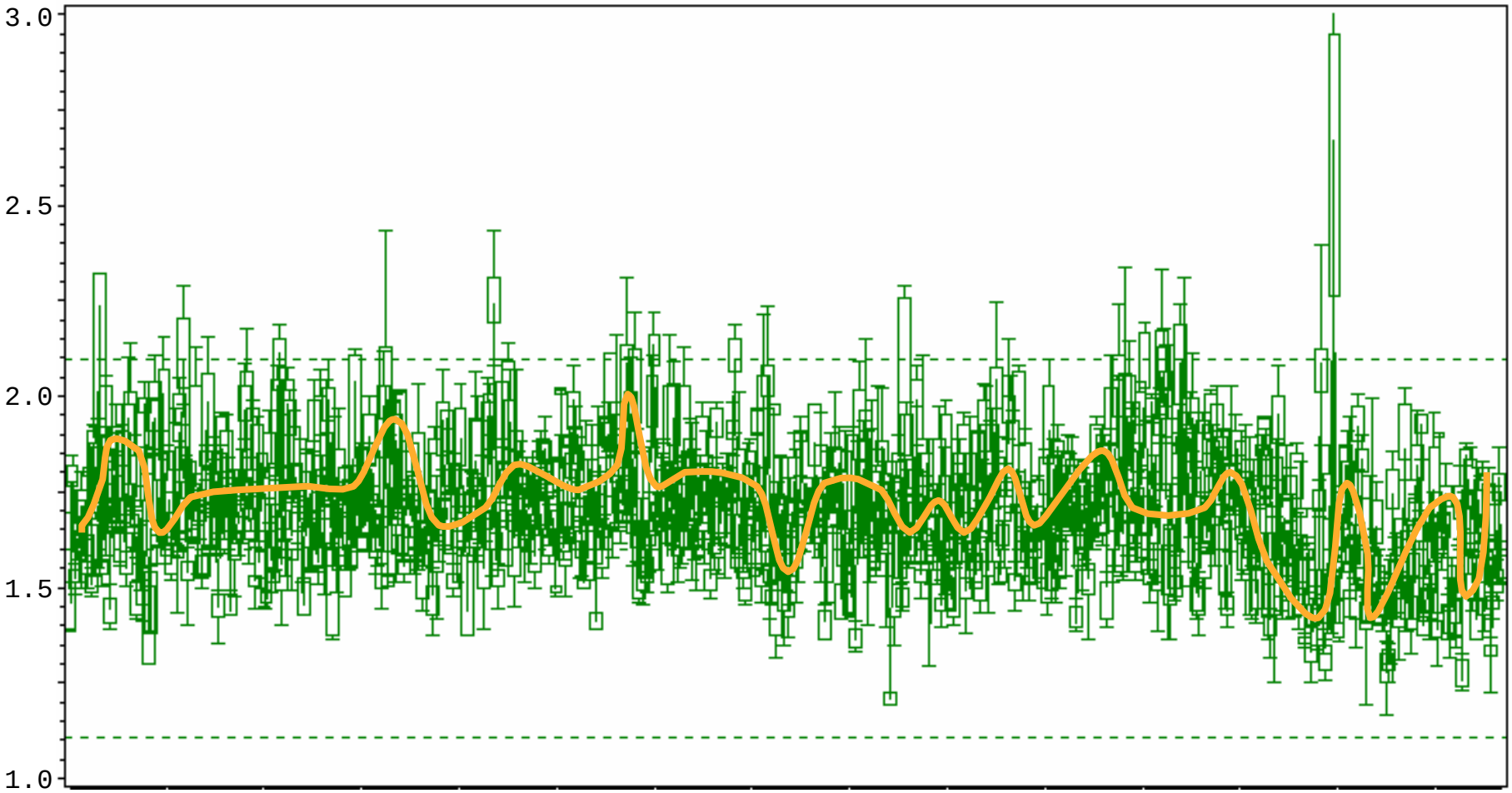
[Praesagus]

Variability from Reactive Ion Etching

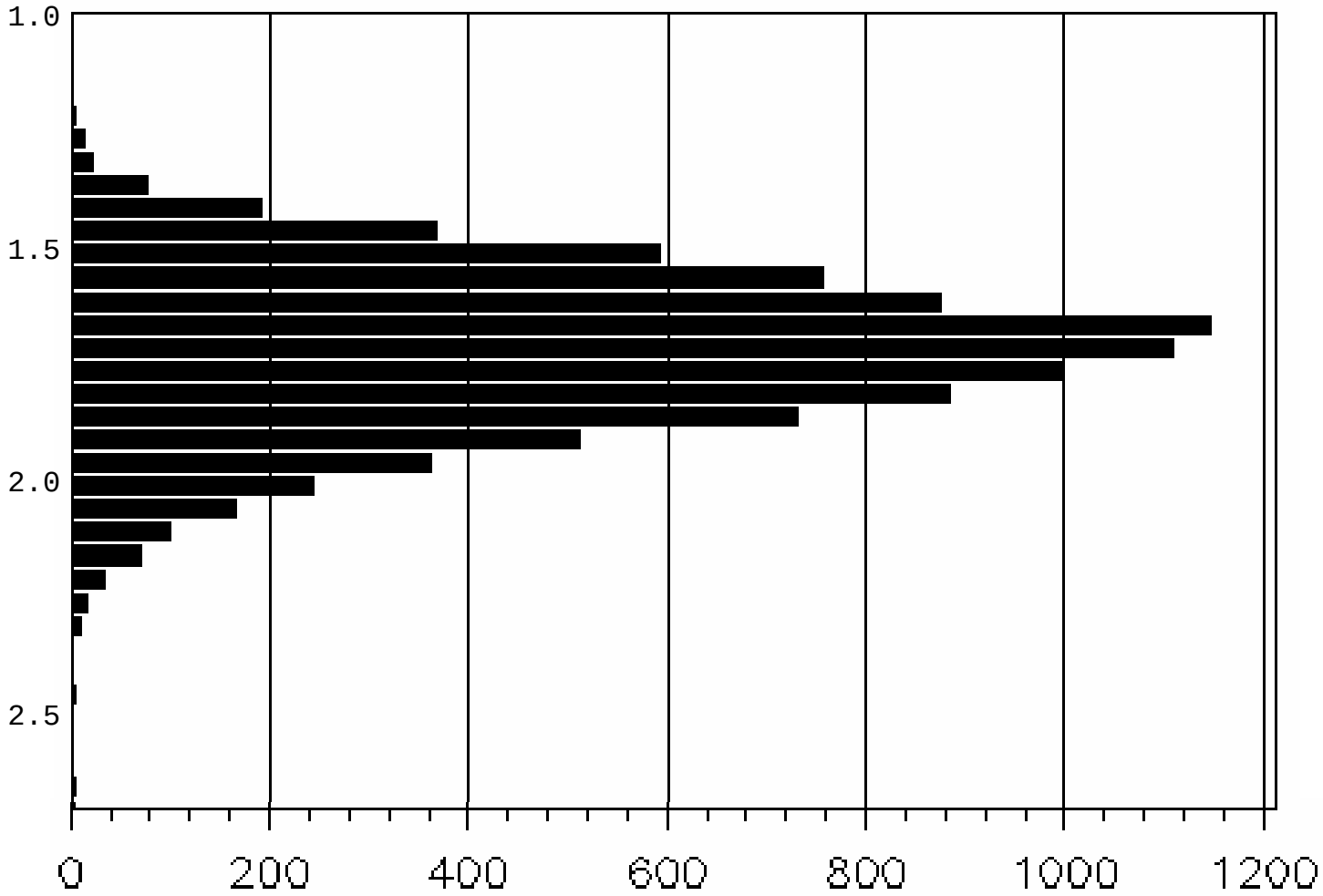


- Wider wires should be treated separately due to RIE etch rate differences
- Thicker wires have resistance, capacitance and inductance ramifications

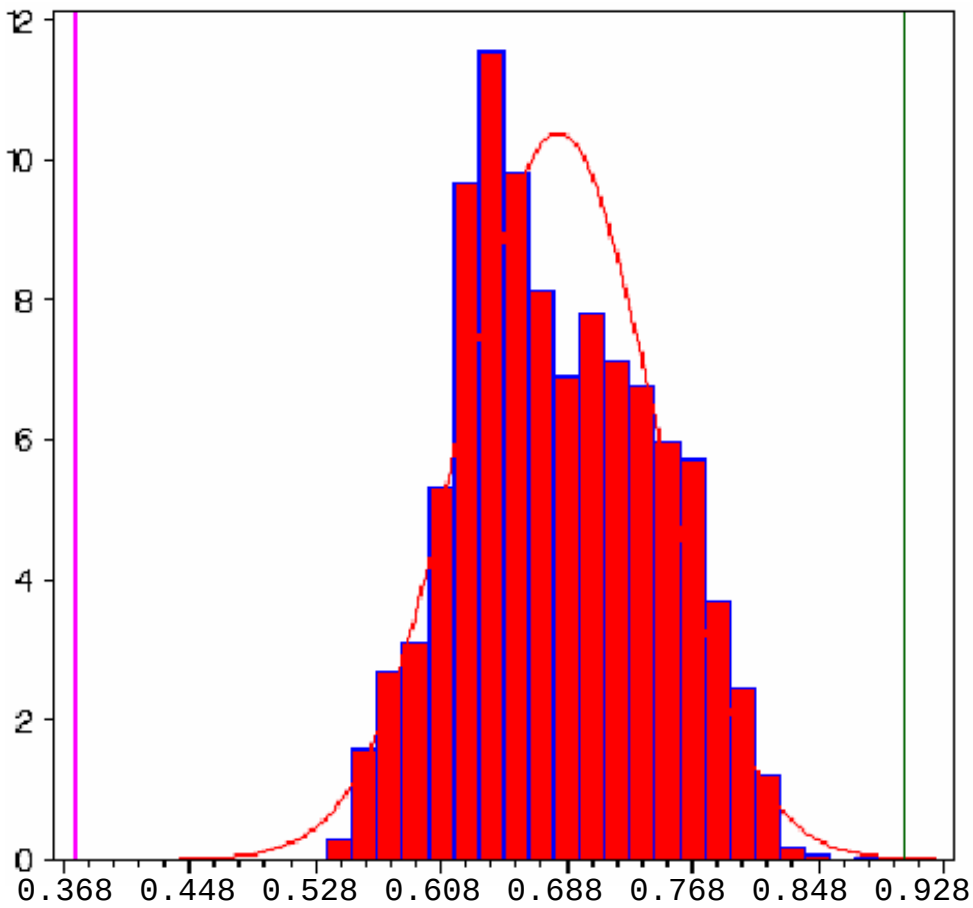
Normalized metal resistance data over 3 months

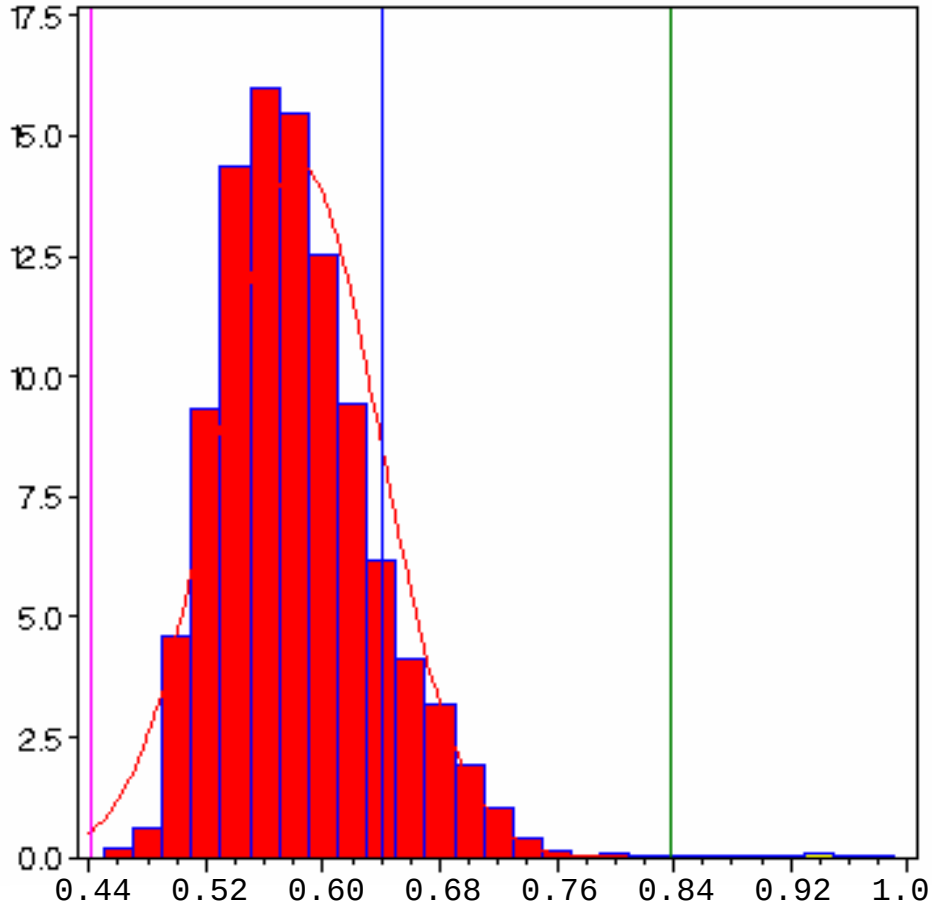


Normalized cumulative statistics

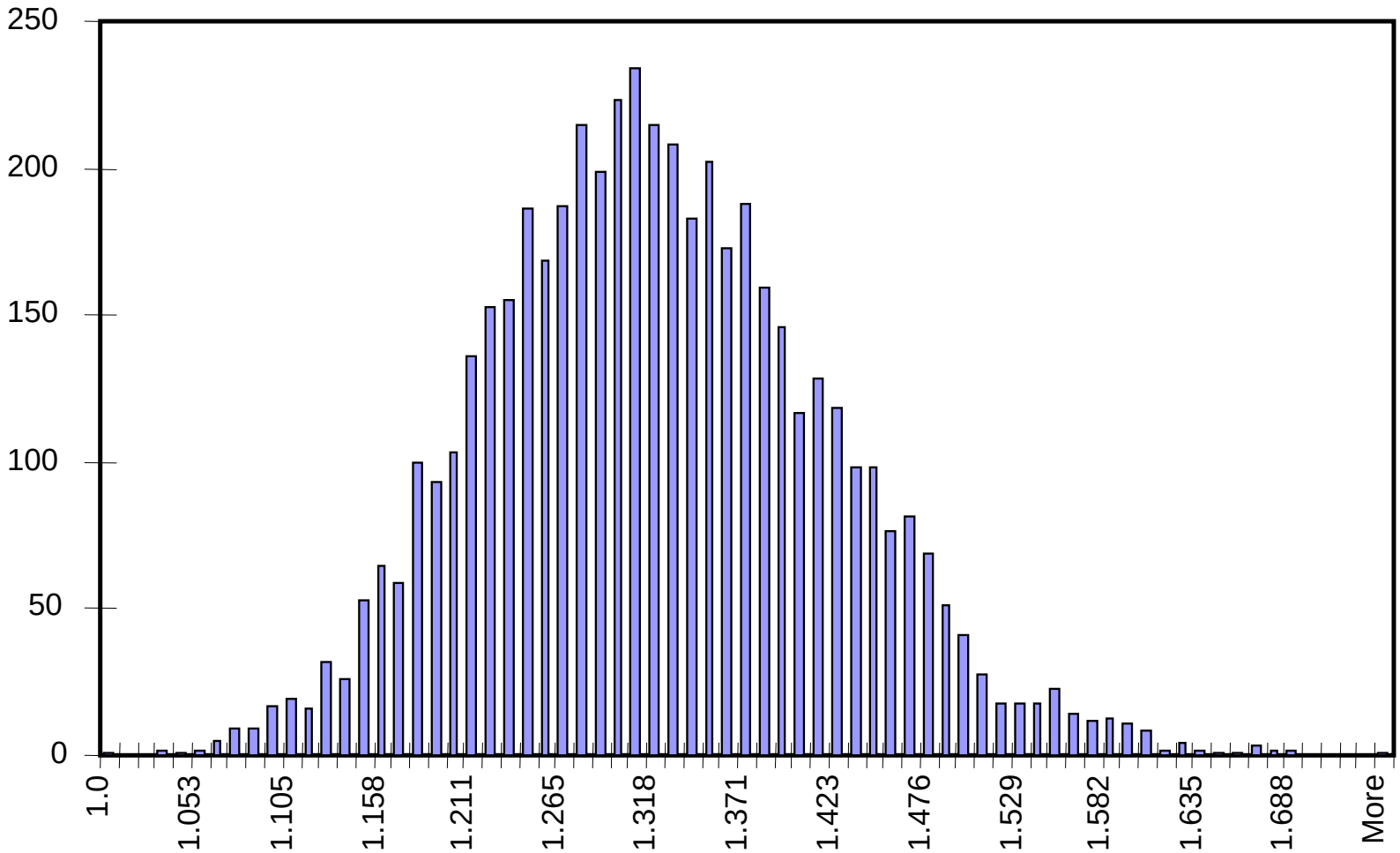


Normalized metal resistance across manufacturing lines





Normalized single-level capacitance distribution



Across-chip BEOL variation causes

- Lithography ACV, just like PC level of similar dimension
- Density-dependent thickness
  - polish, RIE
  - pattern density is a strong function of metal level
  - dummy fill reduces the variation
- OPC distance-dependent bias… more about this later
- Density on M-1 level causes thickness and width changes
  - layer thickness variations in Mx-1 transfer into Mx causing metal thickness variation
  - on large wafers, Cu reflection impacts lithography

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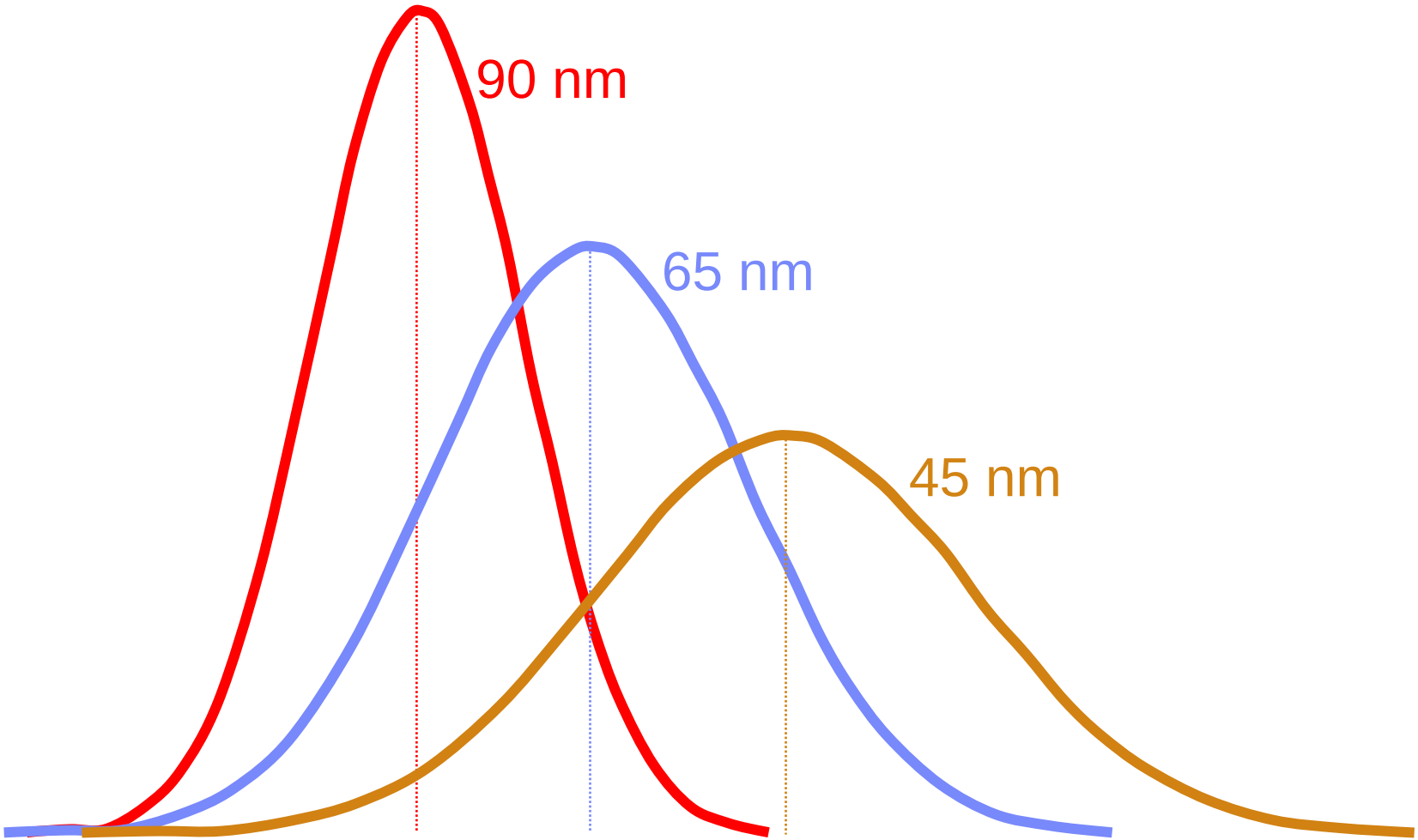
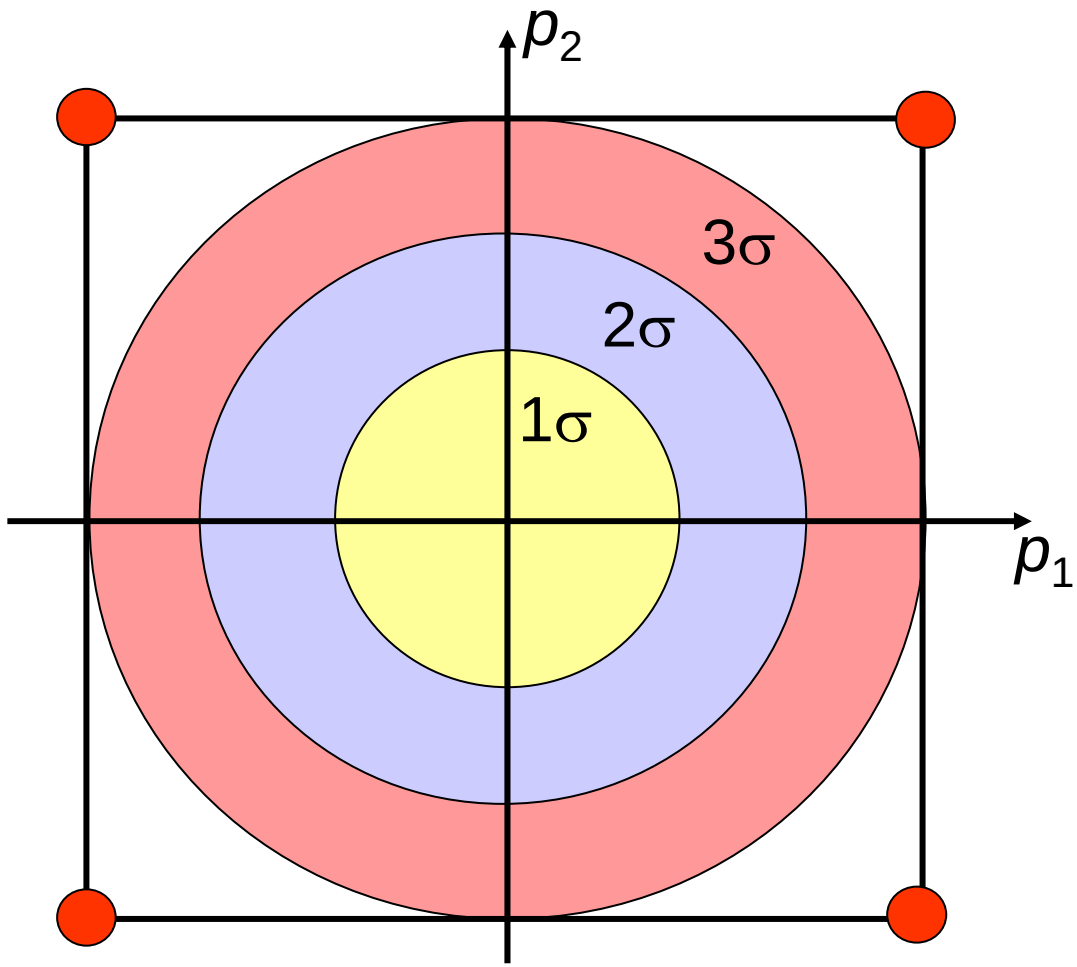
Any performance left in worst-case design?



Worst-case vs. 3σ design



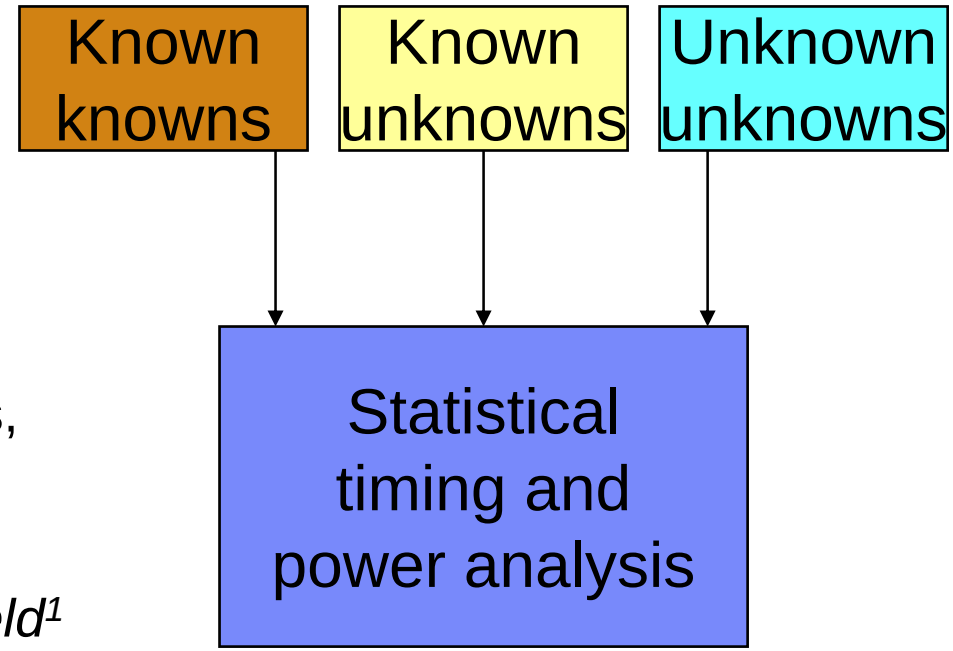
What do we do with all this variability?

As we know,
There are known knowns.
There are things we know we know.

We also know
There are known unknowns.
That is to say
We know there are some things
We do not know.

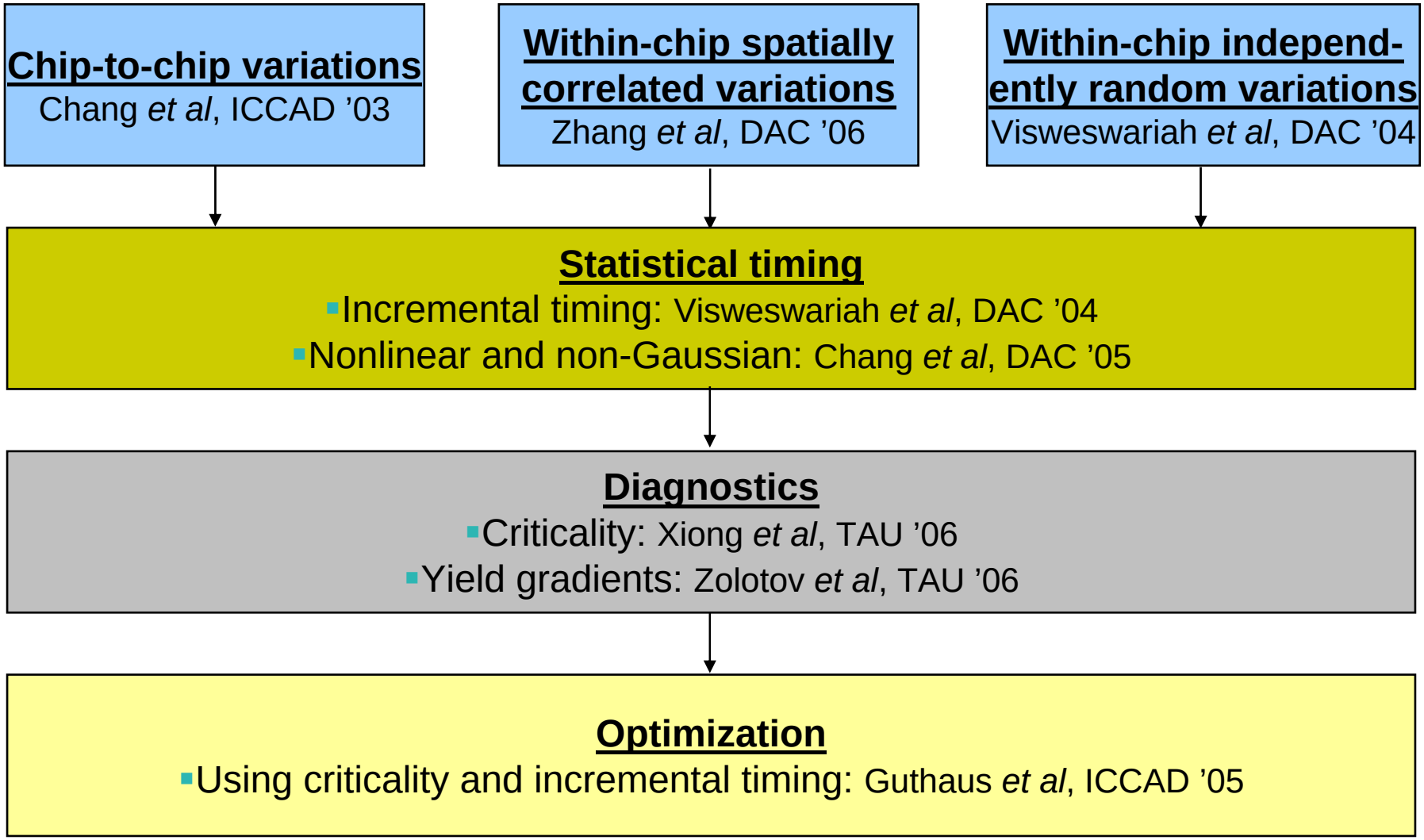
But there are also unknown unknowns,
The ones we don't know
We don't know.

Donald H. Rumsfeld[1]

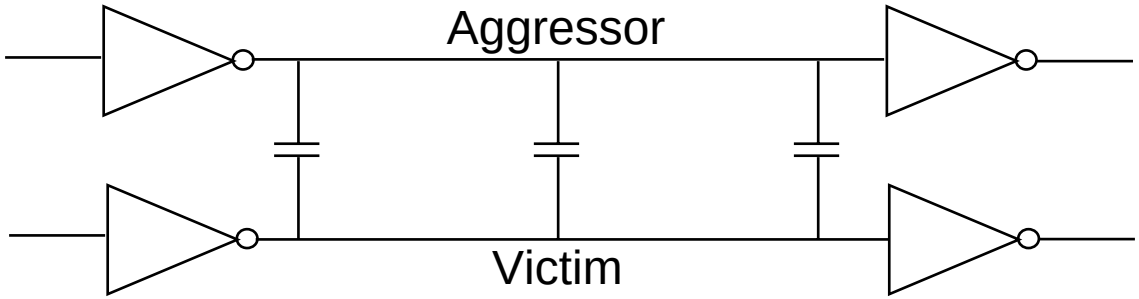


[1]Dept. of Defense news briefing, 2/12/02, linebreaks mine

Statistical timing



Coupling noise



- Driver strengths are functions of process
- Overlap window is a function of process
- Coupling capacitance is a function of process
- Slews are functions of process
- Hence Δdelay is a function of process
  - by taking advantage of these correlations, pessimism can be reduced
- However, logic patterns/correlations cannot be treated statistically
  - a single reproducible vector that causes a deterministic timing problem due to coupling noise is enough to make the chip unusable

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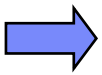
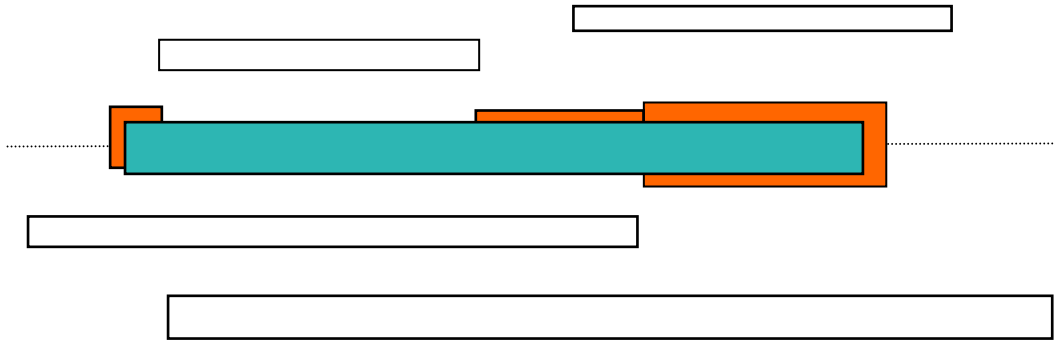


Extraction

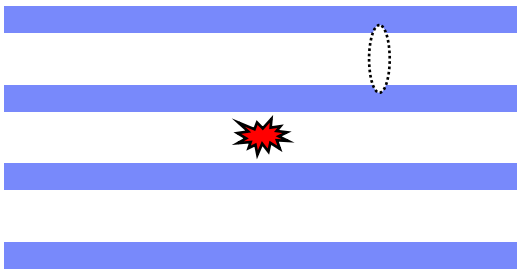
- How many random variables per metal level?
  - 1, 2 or 3?
- Variational extraction (transform geometry distributions to correlated R, C distributions)
- Pattern-density-aware extraction (known unknown!)
  - tile-based thickness model, followed by thickness-aware extraction
- Should extraction anticipate OPC and other data prep. manipulations?
- Spreading for critical area reduction vs. bunching for dummy fill insertion

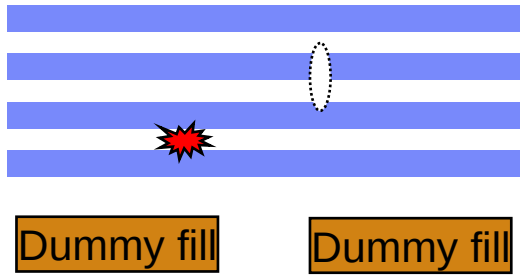
Metal blooming: anticipate OPC?

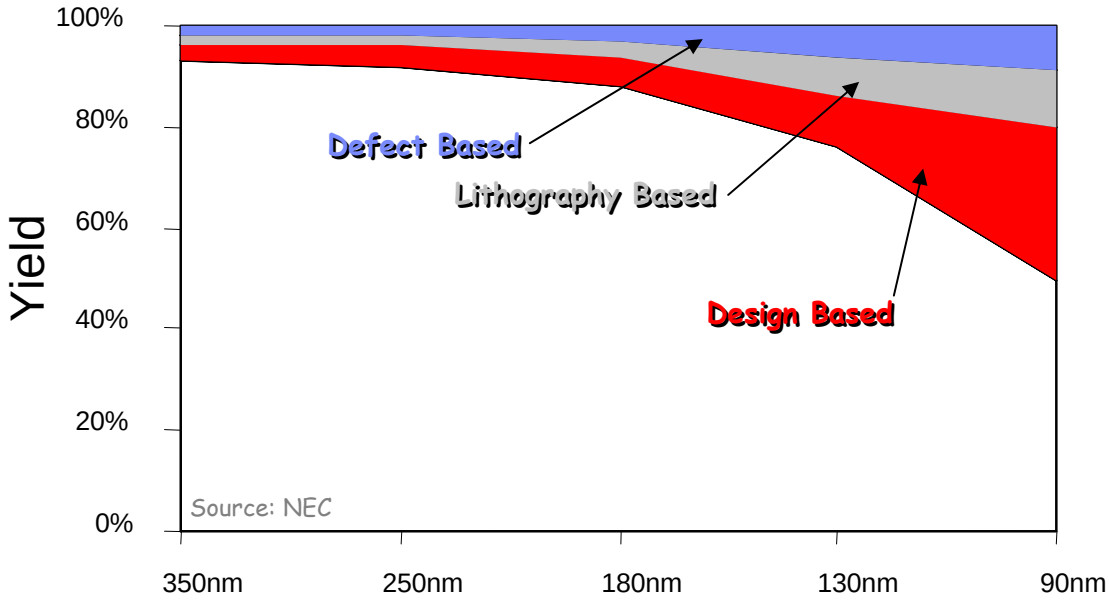


- Anticipation helps reduce resistance
- Increases extraction complexity

Spreading vs. dummy fill insertion







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Robust circuit design

First order model →

$$P(x,y) = mean + \frac{\partial p}{\partial x}\Delta x + \frac{\partial^2 p}{\partial x^2}\Delta x^2 + \cdots + \frac{\partial p}{\partial y}\Delta y + \frac{\partial^2 p}{\partial y^2}\Delta y^2 + \cdots$$

- Its the sensitivities, stupid!

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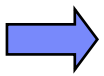
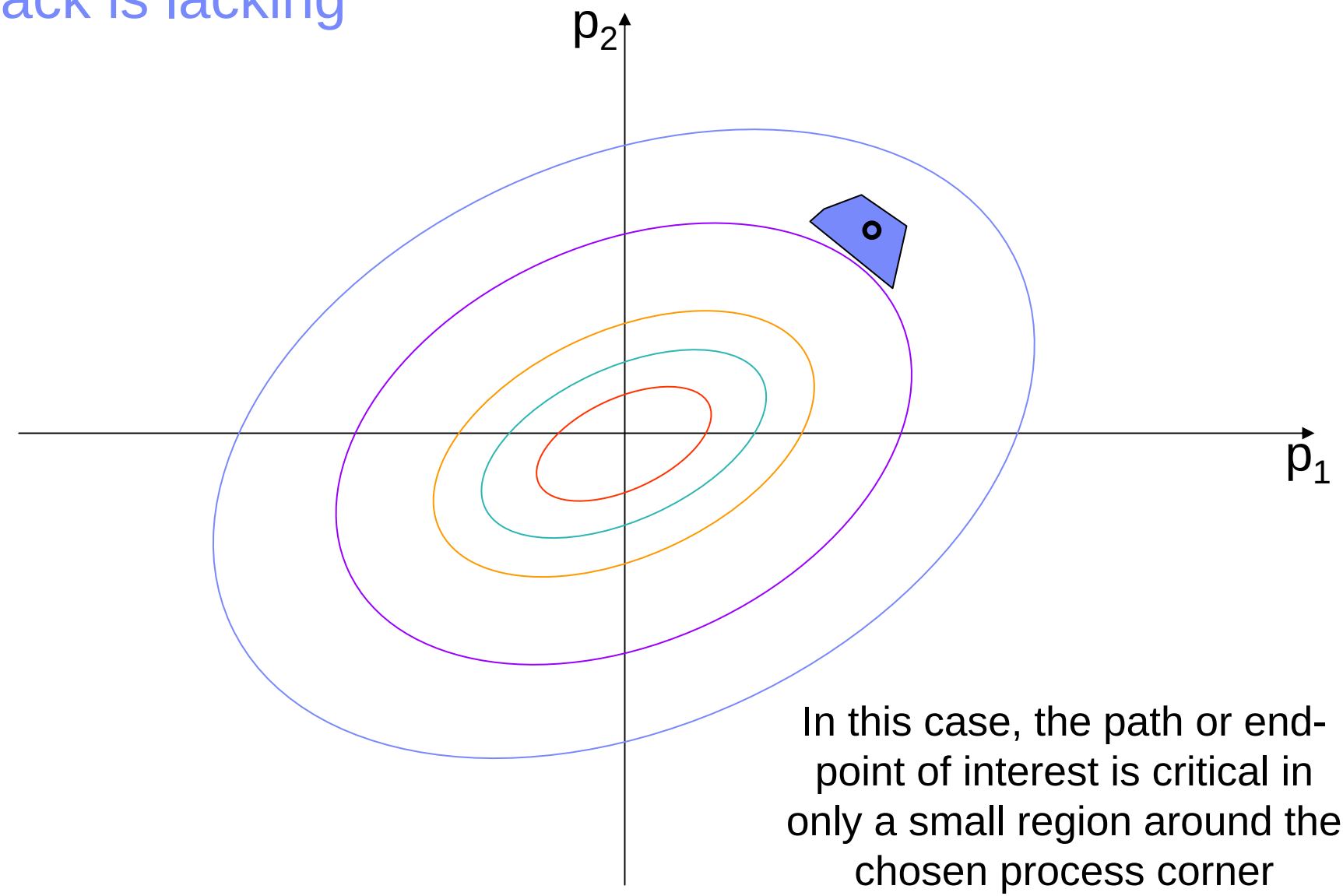


Deterministic vs. statistical optimization

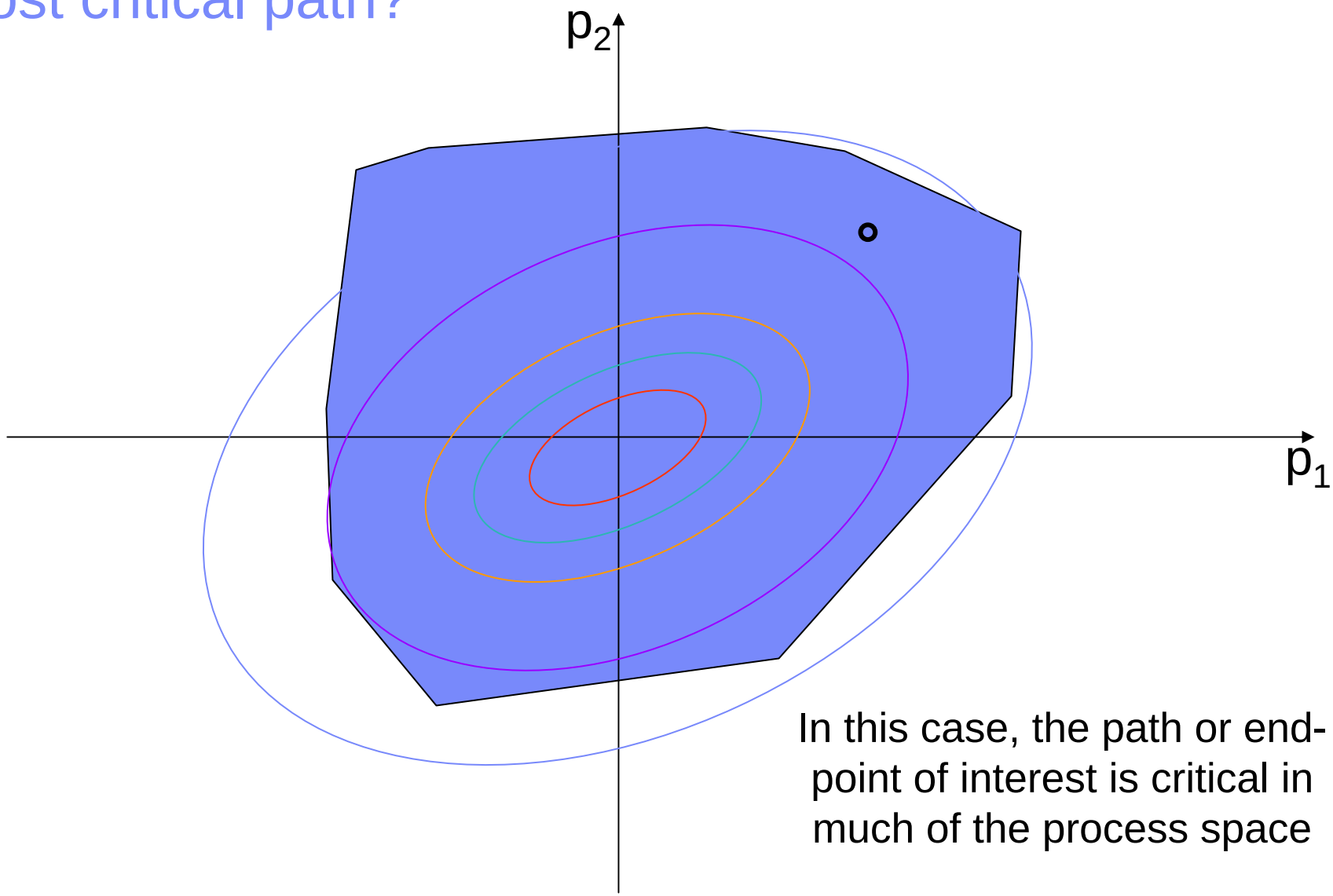
Deterministic	Statistical
Metrics are single numbers	Metrics are correlated distributions
No easy way to cover “all corners” or entire process space	Implicitly covers entire process space
Critical path is unique	Critical path is different at each point in the process space
Difficult to consider parametric yield explicitly; hard to incorporate robustness	Parametric yield can be optimized or constrained; robustness is a natural metric
“Max” operation is not differentiable	“Max” operation is differentiable

Slack is lacking



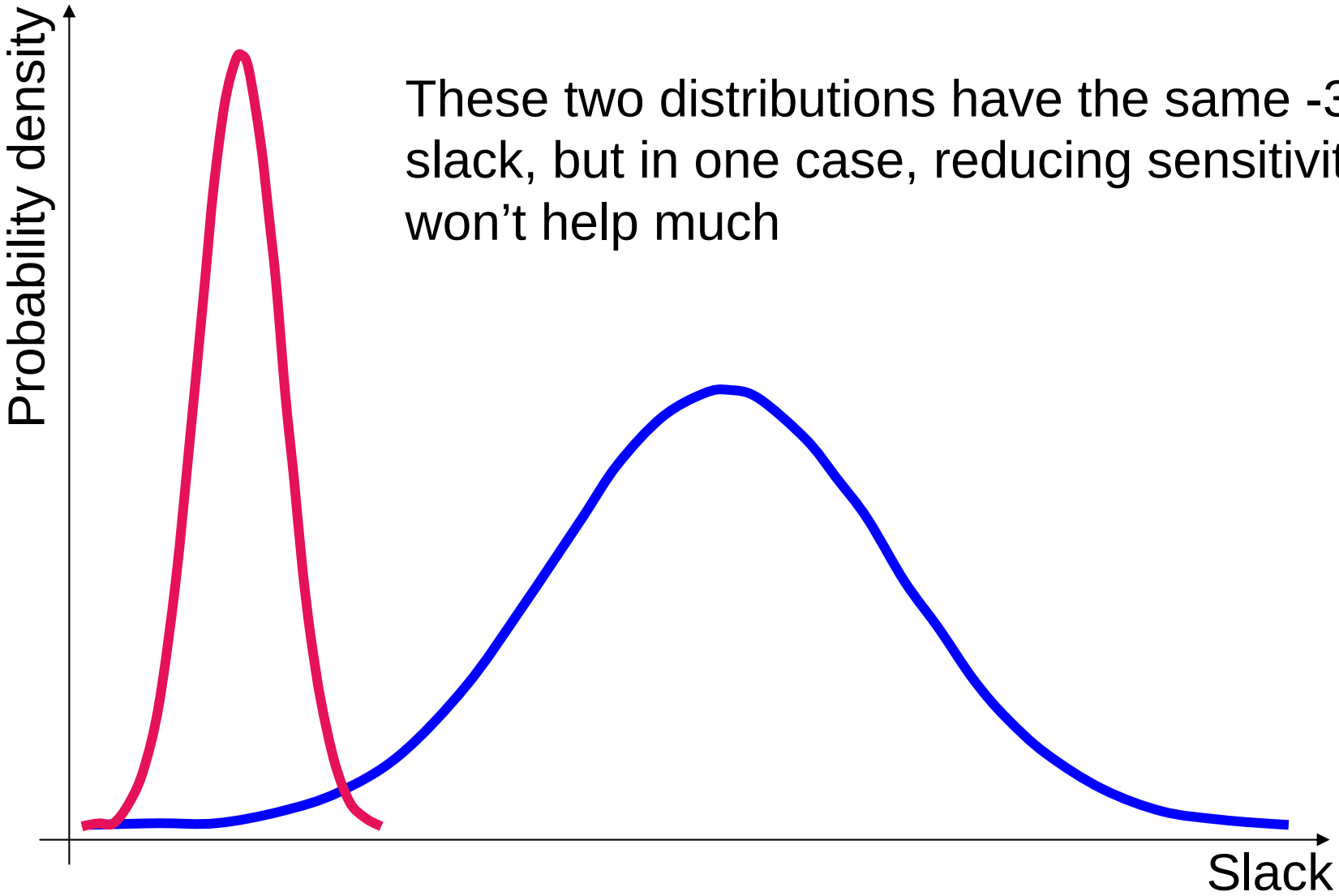
In this case, the path or end-point of interest is critical in only a small region around the chosen process corner

Most critical path?



In this case, the path or end-point of interest is critical in much of the process space

What about -3σ slack?



These two distributions have the same -3σ slack, but in one case, reducing sensitivities won't help much

Relative ordering of paths/end-points

- If path A has a slack of -60 ps and path B has a slack of -50 ps
  - if the two paths are tightly correlated, fixing A is sufficient till it reaches -50 ps since B will hardly dominate anywhere in the process space
  - if the two paths are uncorrelated, fixing A is not enough since B has something to say in large parts of the process space
  - in either case, optimizing mean slack as well as the sensitivity signature simultaneously is more powerful than just optimizing nominal slack

The solution

- Use criticality as a measure
  - simple scalar between 0 and 1
  - defined as the probability of a {node, edge, path} being on the critical path of a manufactured chip
  - covers the entire process space
  - can give guidance to optimization, test pattern generation
  - can exploit conditional criticalities

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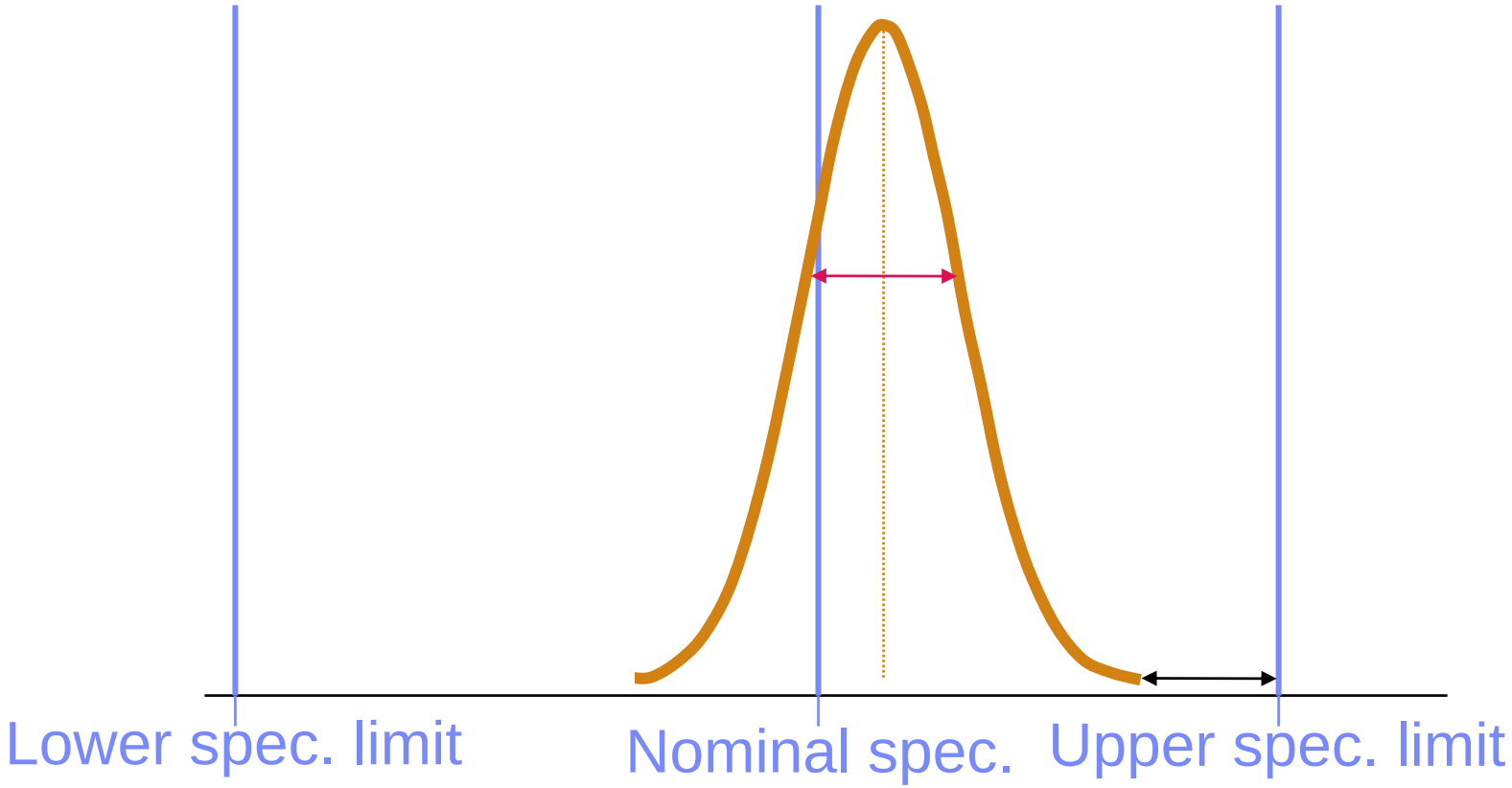
Manufacturing for predictable performance



- Cp and Cpk (Process Capability Indices) measure manufacturing predictability
- Manufacturing typically outperforms spec. limits

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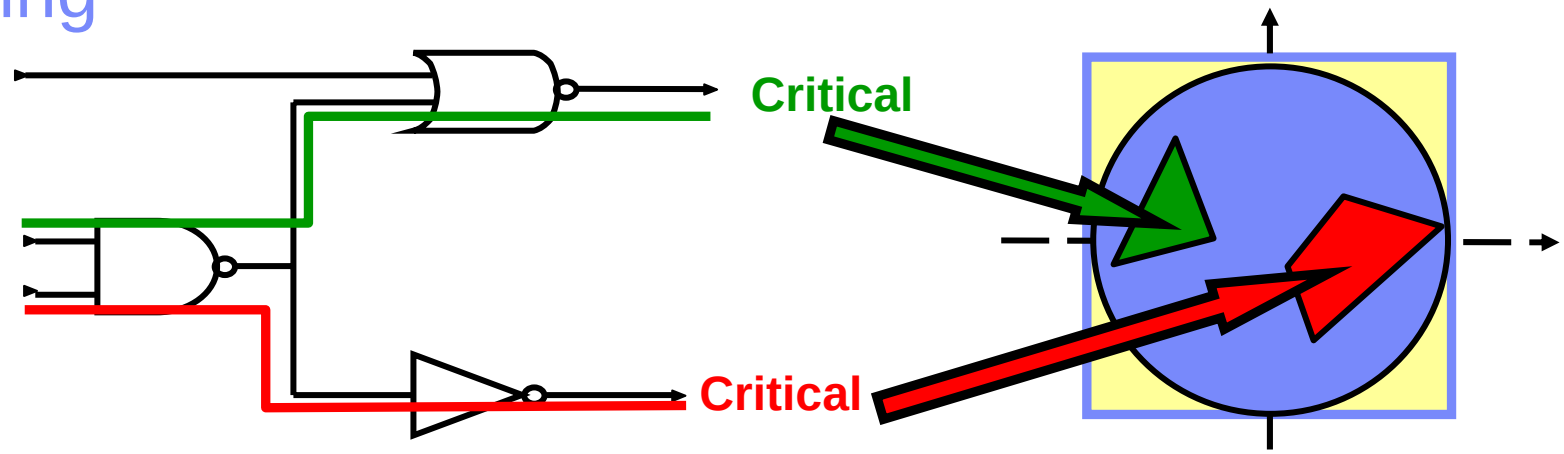
Testing



- Each point in the process space can have a unique critical path
- How to come up with a set of test vectors that tests for parametric variations in all parts of the process space?
- How to measure coverage thereof?
- How to test against workload-related defects?
- How to test against fatigue-related defects?

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