Impact of Interconnect Resistance Increase on the Performance of High-Speed and Low-Power Designs

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Outline

- Interconnect Technology Description
  - Interconnect Resistivity Increase
  - Resistivity and Capacitance Modeling
- Impact of Resistance Increase on Chip-performance
  - State of the art in Literature
  - Case Study for 65nm technology Node
- Conclusions

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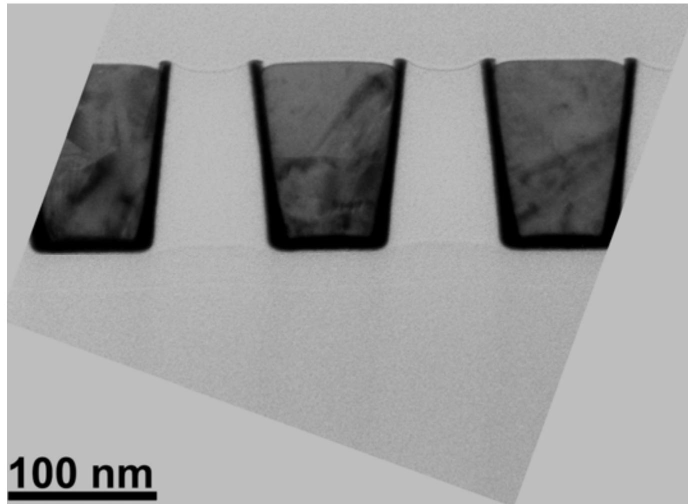
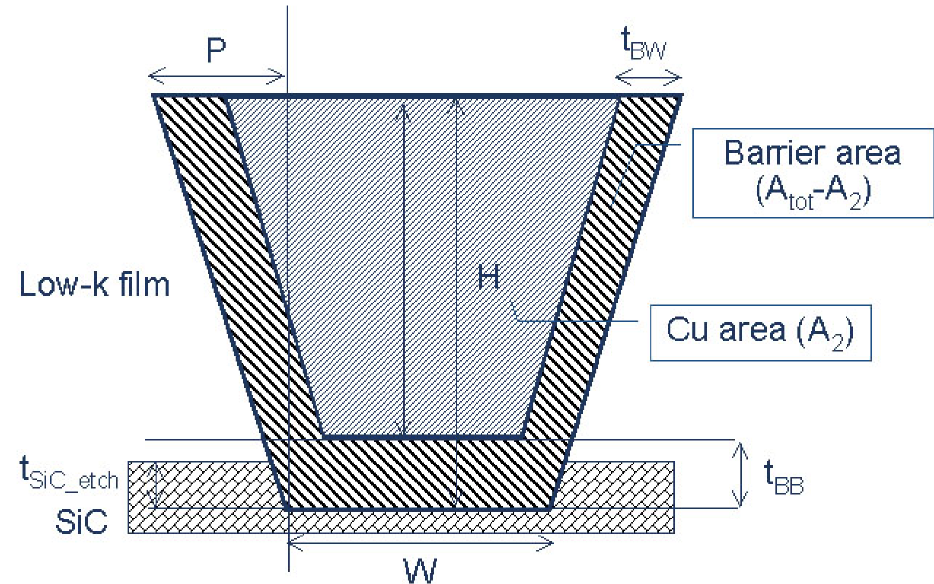
Interconnects are Complex Structures



TEM cross-section of SD-Cu / low-k structures



Process	Input parameter
CD	W
Trench profile	P, W
Etch stop opening	H
Barrier step coverage	t_{BB}, t_{BW}
Height	H

Interconnect Resistivity: Measured Data*

1 / Cross Sectional Area (μm^{-2}) (approx.)	Effective Resistivity ($\mu\Omega$-cm) (approx.)

* Y. Travaly, M. Bamal et al, MAM 2006

Resistivity is increasing linearly with the inverse of cross-sectional Cu area

resistivity vs. 1/Cu area for a trench height ~130 nm

Factors causing the increase in resistivity

- Increase in resistivity in due to:
  - Size-dependent effects (i.e. grain-boundary and interface scattering) [1],[2],[3]
  - Increasing percentage of high resistivity barrier area in the total wire area

[1] K. Fuchs, Proc. Cambridge Philos. Soc. 34,100, 1938
[2] E.H. Sondheimer, Adv. Phys. 1, 1, 1952
[3] F. Mayadas & M. Shatzkes, Phys. Rev. B, 1, 1382, 1970

Measurement Based Modeling of Resistivity

Line conductance increase for a sample with arbitary shape can be expressed as [4]:

$$\frac{\sigma_{Cu}}{\sigma_0} = 1 - \frac{P_{Cu}}{S_{Cu}}.\lambda.\Sigma_{sc}$$

Resistivity is modeled from measurement (verified up to 65nm design rules) as:

$$\rho_{eff} = \beta + \frac{\alpha}{S_{Cu}}$$

Where α and β are empirical constants determined from measurements and S_{cu} is the cross-sectional area of Cu interconnect in um^2

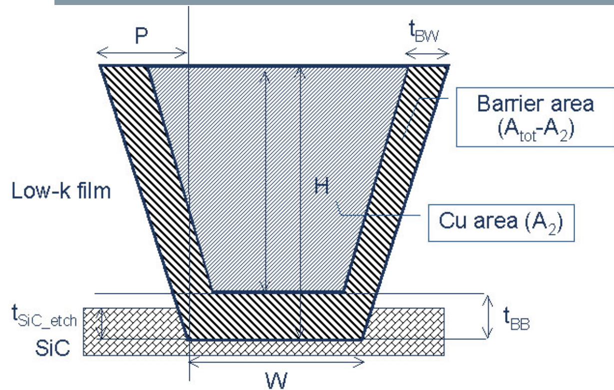
Estimation of α and β

* Y. Travaly, M. Bamal et al, MAM 2006

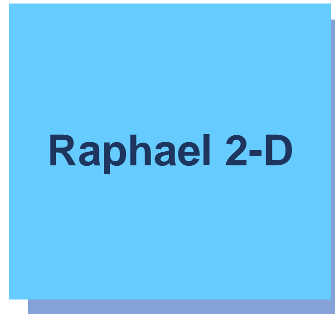
Obtain R vs. Temp. data from measurements. → Obtain ρ vs. A^{-1} data for different interconnect thickness → Calculate the values of α and β

[4] R. B. Dingle, Proc. Roy. Soc., 62, 77 (1949).

Capacitance and Resistance Modeling



Interconnect geometry and material description



Solver

C (pF/mm)

Capacitance Estimation

$$R(\Omega / mm) = \frac{\rho_{eff}}{S_{Cu+barrier}}$$

Resistance Estimation

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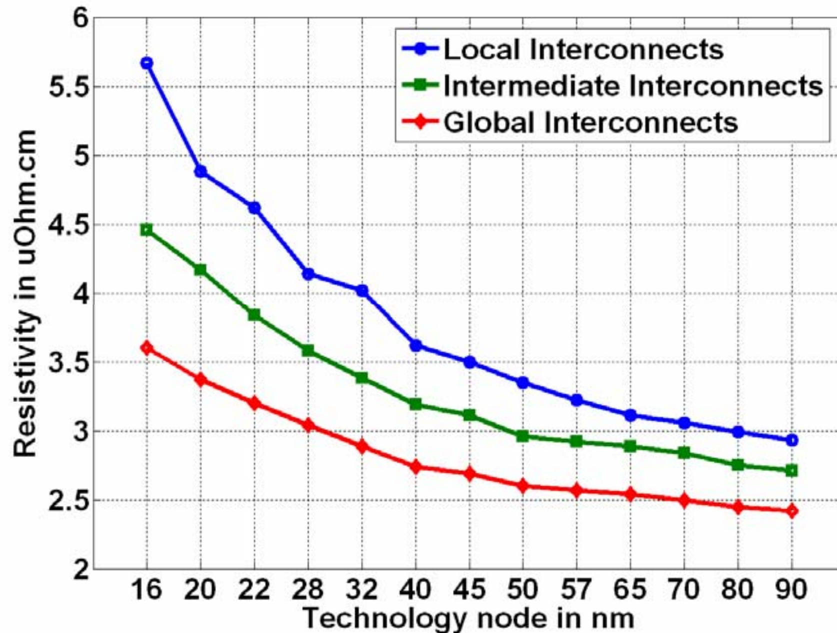
ITRS Trends on Resistivity



Effective Resistivity (ρ_{eff}) vs. Technology node

Observation: The effective interconnect resistivity is increasing with scaling

Consequences: How does this impact the performance of circuits and systems ?

State of the Art in Literature

1) R. Sarvari et. al at IITC 2005 (Georgia Tech.).
   - ➔ Impact of Size Effects on the Resistivity of Copper Wires and Consequently the Design and Performance of Metal Interconnect Networks.

2) V.H. Nguyen et. al. at IITC 2005 (Philips).
   - ➔ An Analysis of the Effect of Wire Resistance on Circuit Level Performance at the 45-nm Technology Node.

3) K. Maex et. al. at ICICDT 2005 (IMEC).
   - ➔ Technology aware design and design aware technology.

Observations

Paper #	Technology Node	Targeted Application	Conclusions
1. R. Sarvari (Georgia Tech.)	100nm and 18nm	High Performance	Resistivity increase has no impact on performance
2. V.H. Nguyen (Philips)	45nm	Low Power and High Performance	Resistance become important for 360(180) um long local interconnects for LP (HP) applications
3. K. Maex (IMEC)	45 and 32nm	Low Power and High Performance	Resistance becomes important for 386um long interconnects for 45nm technology node

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    - Tile Model
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Impact on System Level performance

- The case study is done for 65nm technology node.
  - The choice is made because of the availability of process data to calibrate the **resistivity model** and to enable a more **realistic evaluation of different interconnect options**.

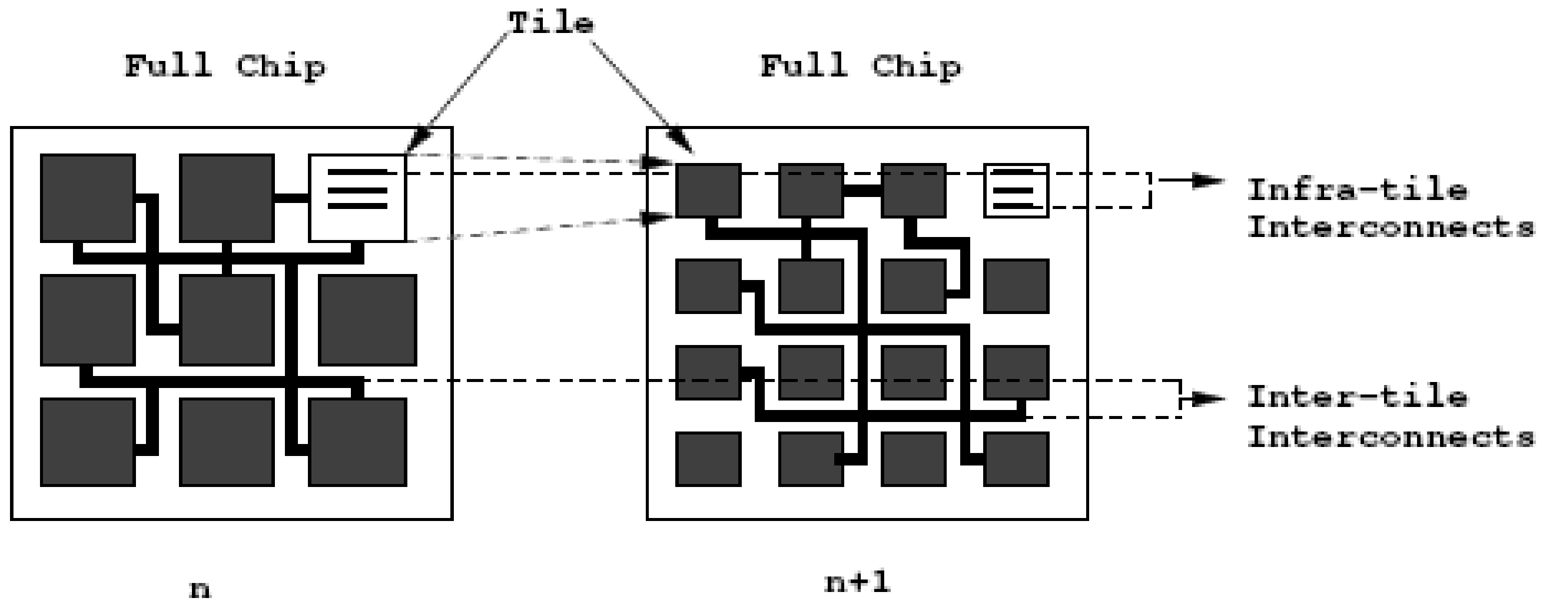
- The analysis is performed on a **standard cell based** design representing a medium sized tile.

- Various high resistance and low resistance interconnect options are evaluated to **understand the various trade-offs involved.**

- The analysis is performed for **high performance** and **low power applications.**

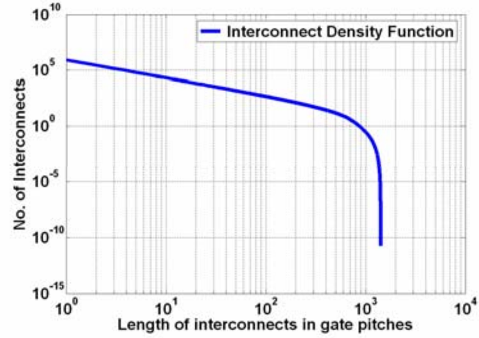
Why Tile?

Difference between scaling behavior of local (intra-tile)

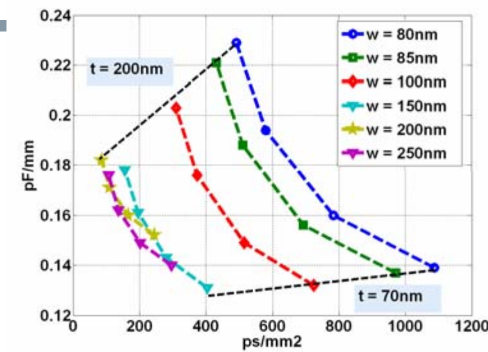


The intra-tile interconnects are scaling in length with the process technology scaling and are routed through local layers of metal, hence the impact of resistivity increase should be studied in context of intra-tile interconnects

Overall Methodology



PHYSICAL PARAMETER	VALUE
Number of Gates,N	500000
Rent's Exponent, p	0.7
Rent's Coefficient, k	4.0
Minimum Feature Size, F	0.08 μm
Supply Voltage, Vdd	1.1 V
No. of Metal Levels, n	4
Routing Efficiency, e_w	0.4



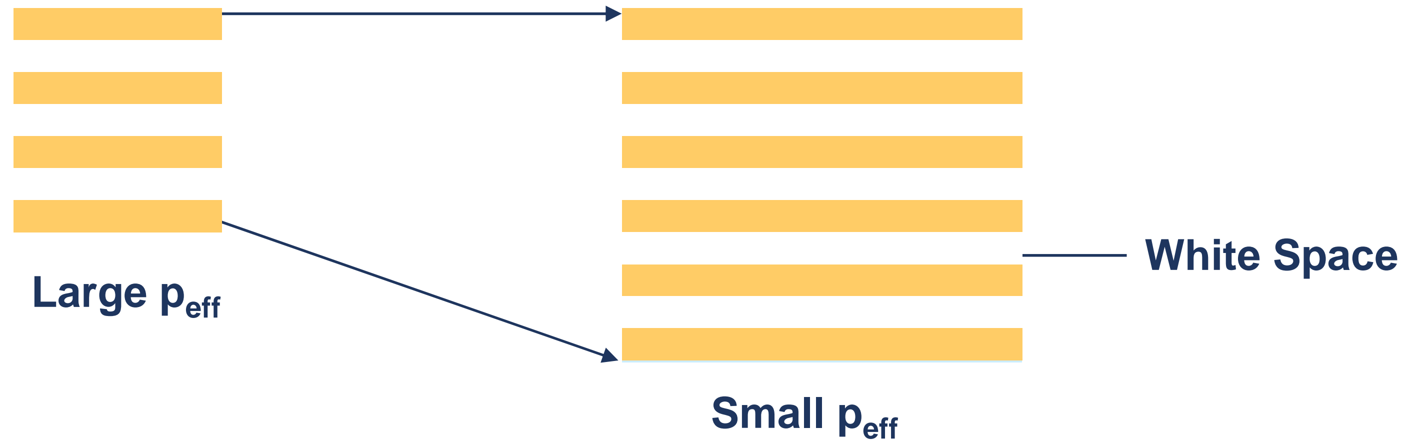
Length distribution for the Tile → Wiring Demand

System Level parameters for the Tile → Wiring Supply

Wiring Demand = Wiring Supply → Calculate the placement efficiency → Calculate Area, average interconnect length in each layer → Calculate F_{clock}, Energy and Power

Interconnect Technology Options → Calculate F_{clock}, Energy and Power

Placement Efficiency Calculations



Wire Supply = Wire Demand ➔ Chip is wirable

$$\frac{A_g N}{p_{eff}} \sum_{1}^{n} \frac{e_w}{pitch(n)} = \chi \sqrt{\frac{A_g}{p_{eff}}} \int_{1}^{2\sqrt{N}} i(l) l dl$$

[5] J. A. Davis et. al. “A stochastic wire-length distribution for gigascale integration (GSI)-parts I and II”, IEEE TED, 1998

[6] P. Christie et. al. “The interpretation and application of Rent's rule”, IEEE Trans. VLSI sys., 2000

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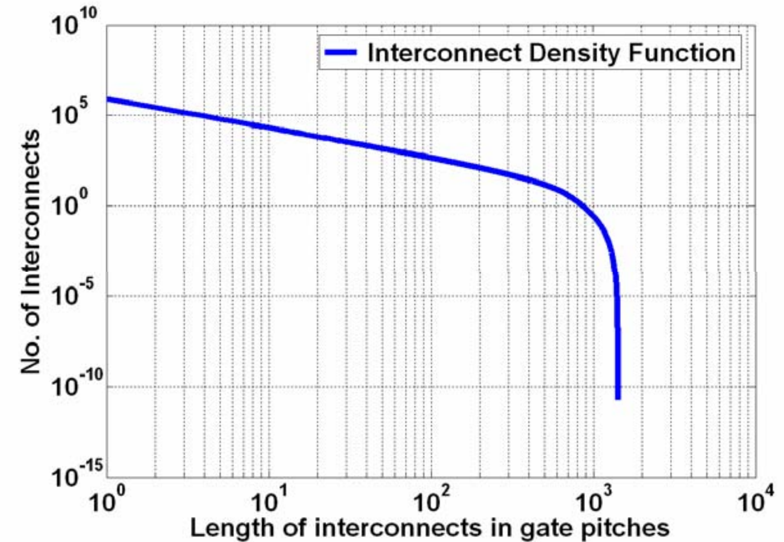
System Level Model of a Tile

Physical Parameter	Value
No. of Gates, N	500000
Rent's Exponent, p	0.7
Rent's Coefficient, k	4
Minimum Feature Size, F	0.08μm
Supply Voltage, V_{dd}	1.1 V
No. of Metal Levels, n	4
Wiring Efficiency, e_w	0.4



The predictive length information can be derived by stochastic length distribution models based on Rent's rule. ["Davis Model"].

- **This length information gives the wiring requirements of the tile. This wiring requirement has to be met by the metal layers available for routing.**
- **In the contemporary high performance designs the interconnect requirements decide the tile area, performance and energy dissipation.**

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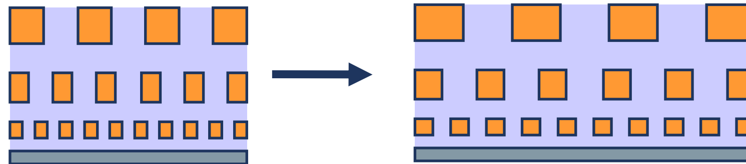
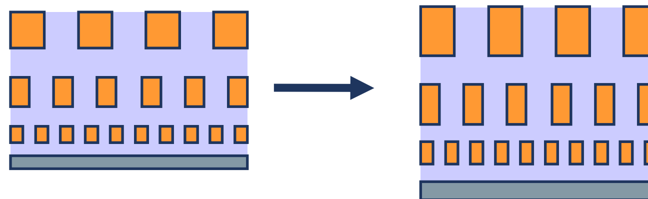
Interconnect Technology Options

- Interconnect Options can be generated by
  - Variable pitch at constant height
    - Trading off density with Improved RC and C

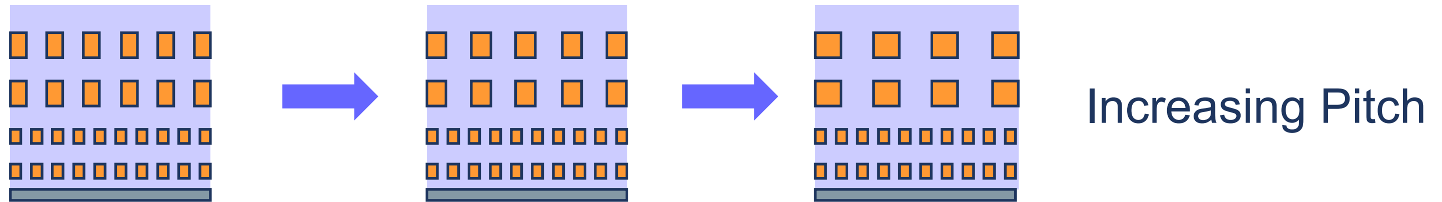


  - Variable interconnect height for constant pitch
    - Trade off between C and RC



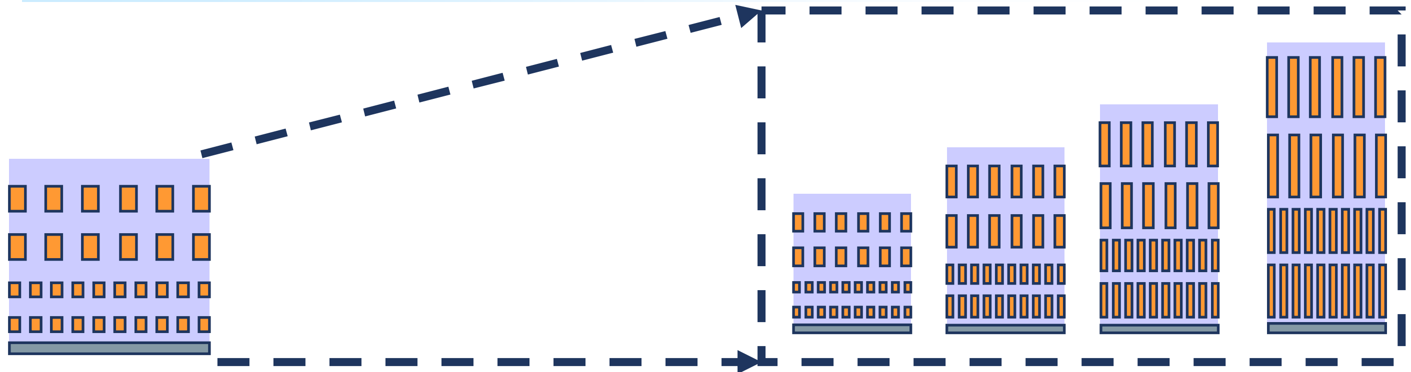
  - Variable width for constant pitch
    - Trade off between C and RC
    - Theoretical option at this stage
  - Variable spacing for constant width
    - Trade off between density and performance
    - Theoretical option

Options used in this case study



Increasing Pitch

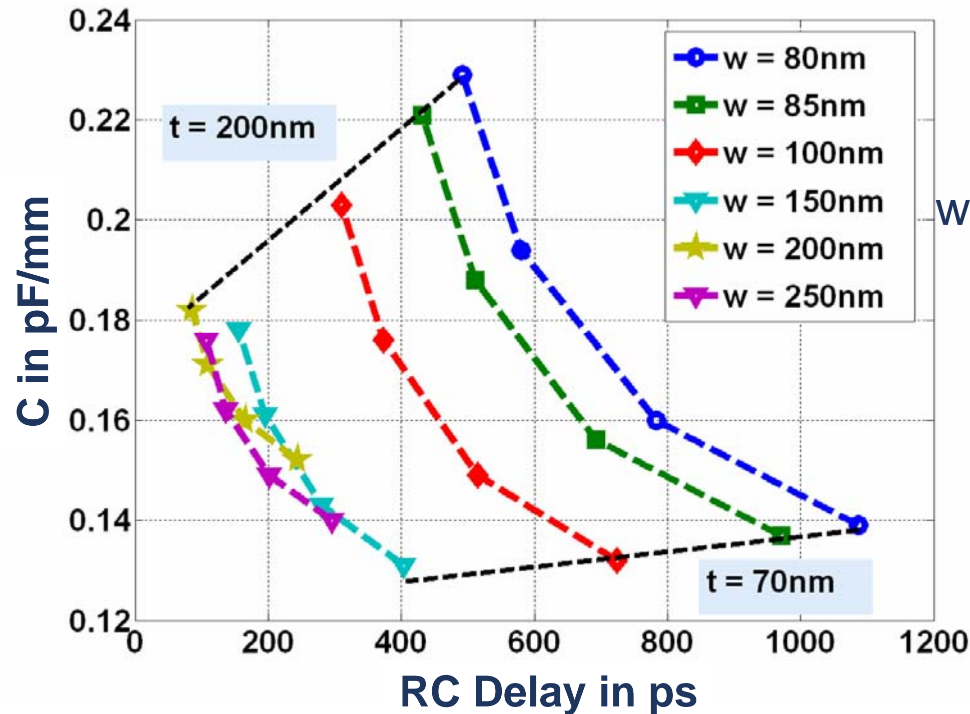
- Decrease in Resistivity/Resistance and Capacitance
- Decrease in wiring density



- Exploring different interconnect thickness for same pitch
- Decrease in resistance/resistivity and increase in capacitance

Various high resistivity/resistance and low resistance options can be generated using this methodology

Range in Interconnect RC Delay and C



width=spacing=pitch/2

- Using the available technology options a 2X range in capacitance and 3X range in RC delay is possible
  - Low thickness options have high RC delay and lower capacitance
  - The wide pitch options have lower RC delay and lower Capacitance at the expense of decreased wiring density

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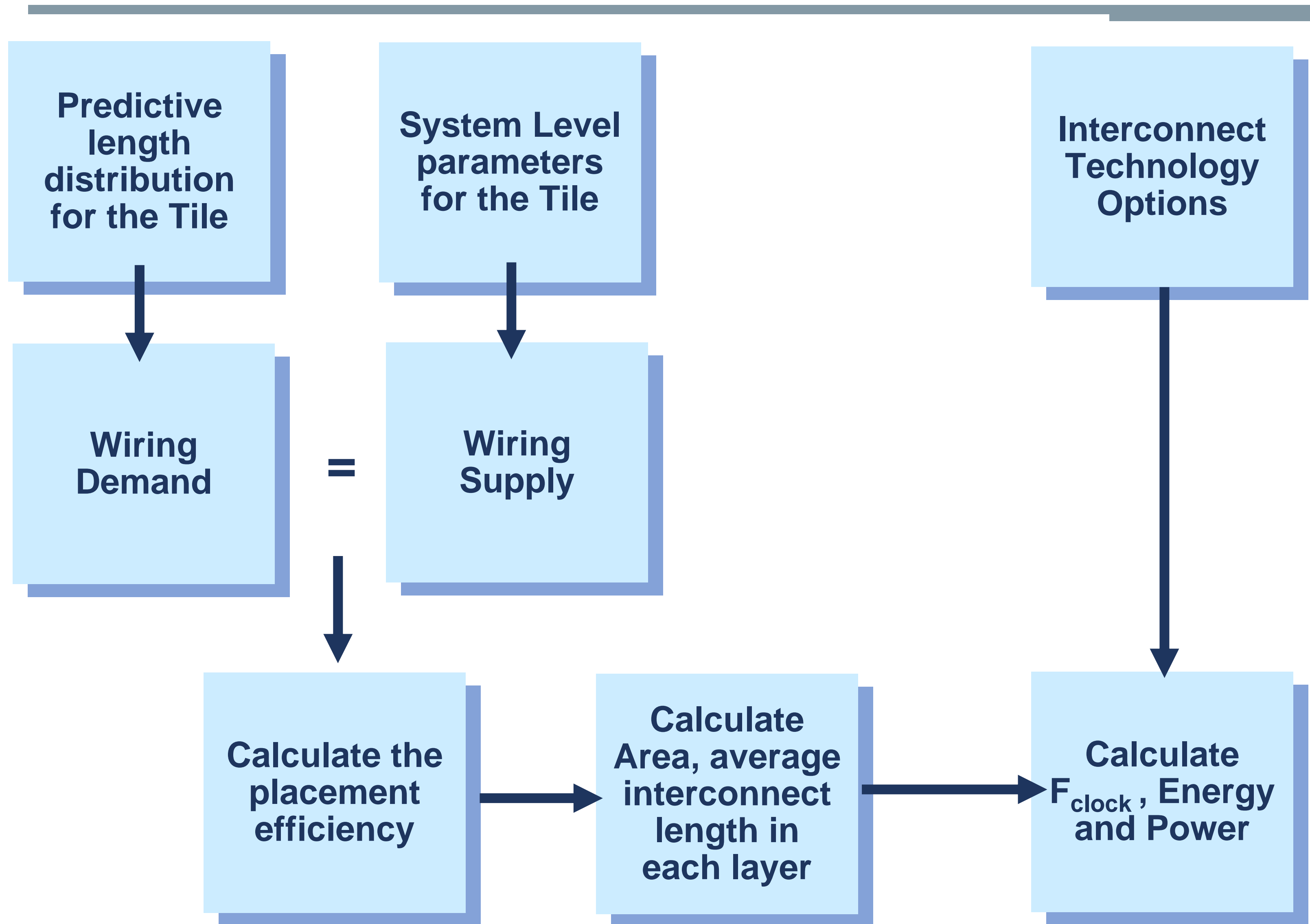
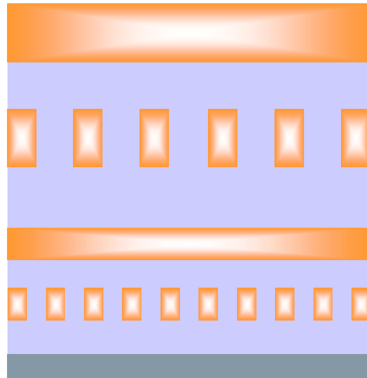


Simulation Setup



- A two tier interconnect stack is chosen for the analysis
- Tier-1 uses minimum pitch since it is utilized for short interconnects
- Different interconnect pitches for Tier-2 are used to understand the impact of resistance and the trade offs involved

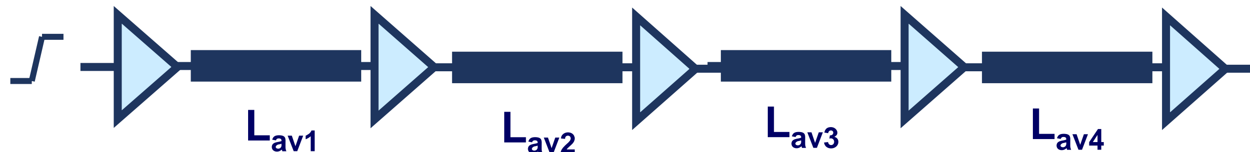
An Interconnect Stack with 2 Tiers

Exp#	Tier-1 Pitch (nm)	Tier-2 Pitch (nm)	P_{eff}	Area (mm^2)	Total Wire length (Tier-1) m	Total Wire length (Tier-2) m
P170	160	170	0.39	1.61	8.06	7.58
P200	160	200	0.34	1.87	9.37	7.5
P300	160	300	0.24	2.58	12.9	6.89
P400	160	400	0.20	3.10	15.5	6.2
P500	160	500	0.18	3.49	17.4	5.58

Average Lengths in Different Experiments

Exp #	L_{av1} (μm)	L_{av2} (μm)	L_{av3} (μm)	L_{av4} (μm)
P170	5.8032	75.032	258.38	701.04
P200	6.621	94.071	316.4	793.47
P300	8.7695	152.99	494.07	1043.2
P400	10.429	207.92	658.53	1248.6
P500	11.626	252.58	797.61	1409.6

Critical Path Model



- Critical path model is chosen to reflect the average interconnect lengths
- The gates are minimum sized gates for low power design
- The gates are maximum sized allowed by free silicon area for HP design

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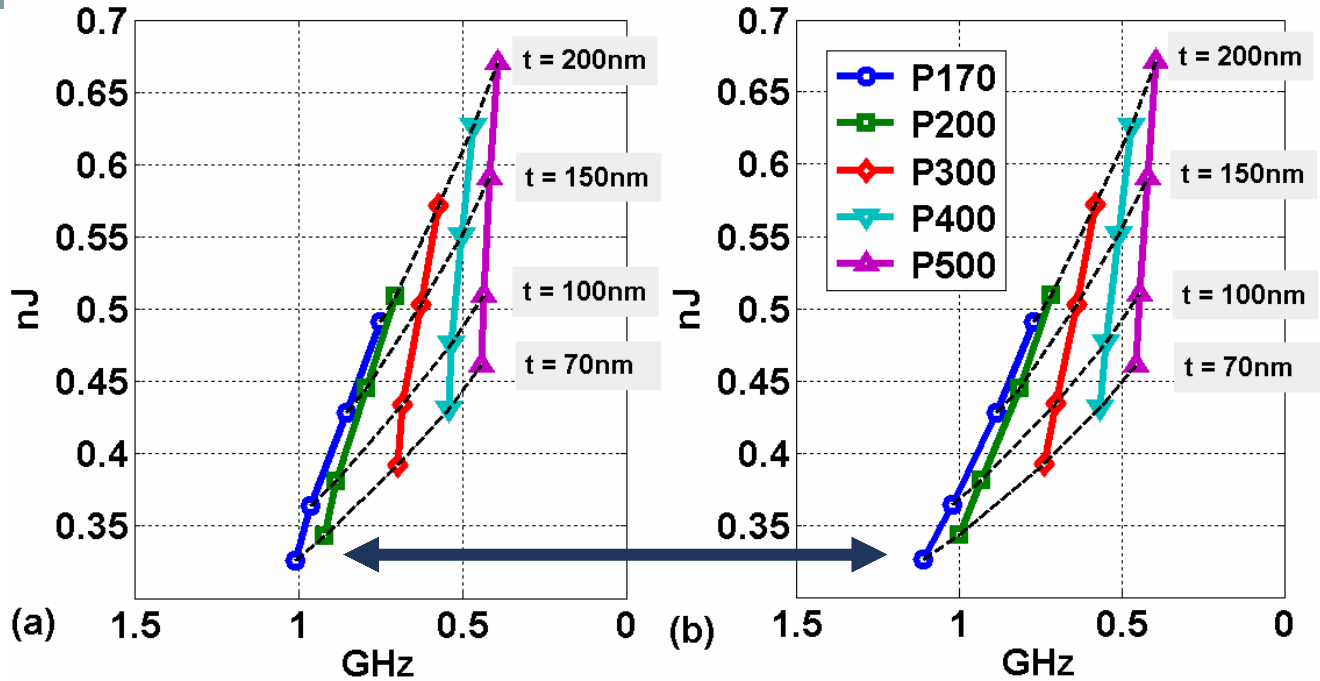
Low Power IC

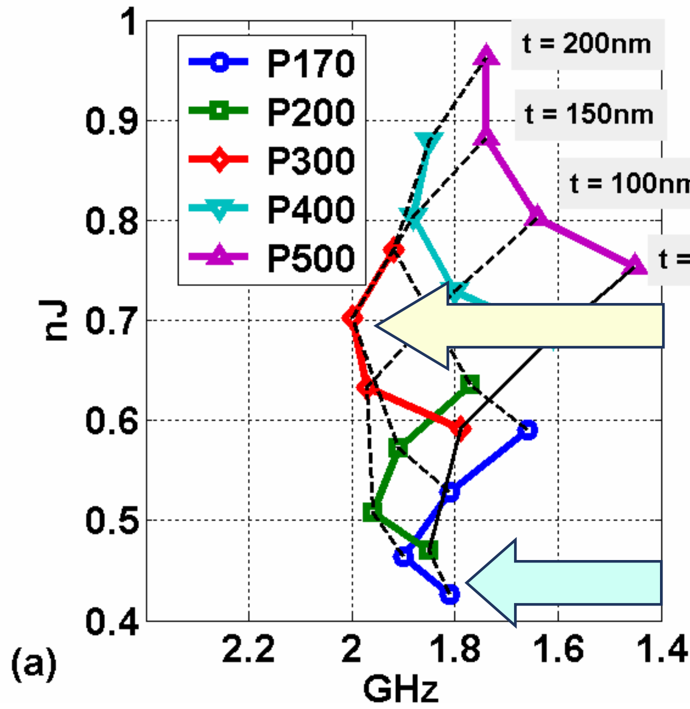


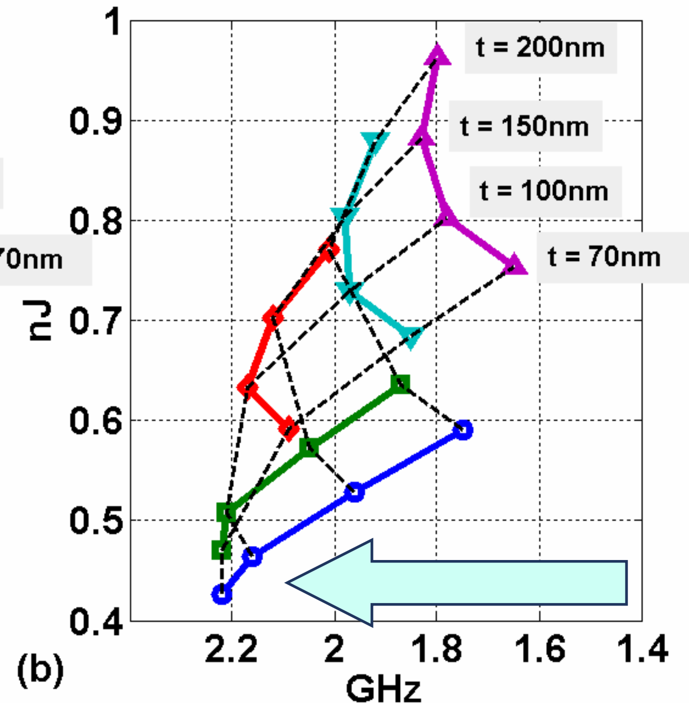
With resistivity increase

Without resistivity increase

- ❑ The resistivity increase is not affecting the performance scaling
- ❑ The low power devices have much higher impedance than the interconnect resistance
- ❑ Delay is contributed by interconnect capacitive loading on the driving gates and not by its intrinsic RC propagation delay.

High Performance IC (Larger Gate Sizes)





With resistivity increase

Without resistivity increase

- Resistivity increase impacts the performance of high-speed applications.
- Performance can be enhanced by optimal interconnect sizing.
- A trade off between various metrics of interest can be made depending on the targeted application.

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Summary

Optimal interconnect technology options for Tier-2

	pitch(nm)	thickness(nm)		pitch(nm)	thickness(nm)
Energy	170	70	Energy	170	70
GHz	300	150	GHz	170	70
Area	170	Any	Area	170	Any

High Performance Applications

Low Power Applications

- To minimize both energy and area, minimum pitch (170nm) should be chosen.
- To maximize the speed (GHz), a wider pitch of 300nm is suitable with a thickness of 150nm.
- For low power applications, the minimum pitch (170nm) and minimum thickness (70nm) provides the minimum area, minimum energy and maximum performance.

Conclusions

- Interconnect resistivity does not have significant impact on the performance of low power IC's.
- Interconnect resistivity can decrease the performance of high performance IC's if resistivity is not handled early in design phase through optimum interconnect sizing.
- The analysis was carried out for standard cell based designs. This analysis will be extended to cover more realistic designs reflecting the contemporary memory dominated applications.

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Questions??

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