Constant Impedance Scaling Paradigm for Interconnect Synthesis

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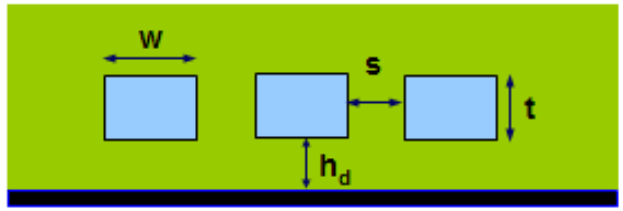
Introduction

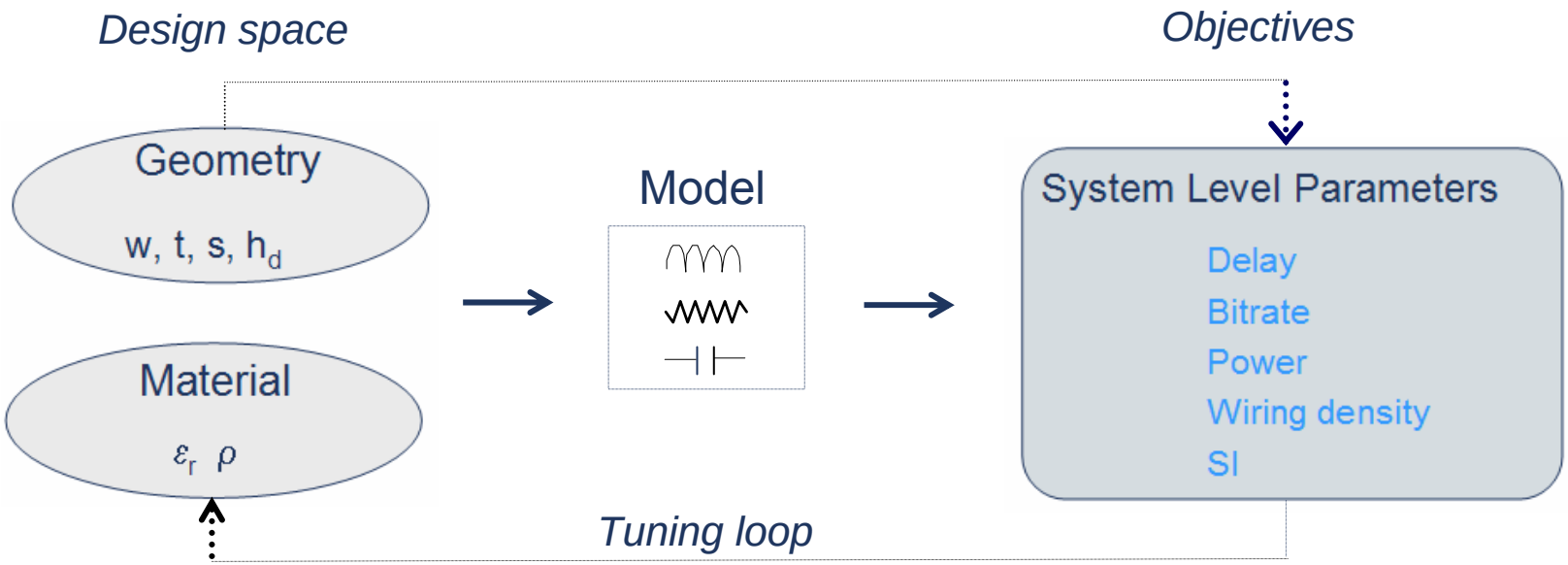
- Global interconnects are *performance limiters* in nano-CMOS regimes
  - Billion transistor + Integration densities
  - GHz range clock frequencies

- "Computer Architecture is all about Interconnects"
  - Bill Dally, Stanford

- Need for proper (global) interconnect design and optimization
  - Application Independent
  - Interconnect stack technology development

Interconnect Design Loop





- Numerous possibilities in the design space
- Systematic Design ?

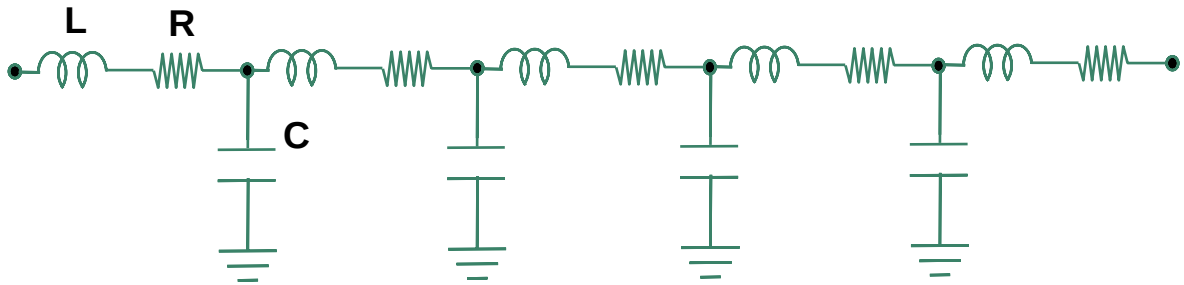
  → Constant Impedance Scaling

Outline

- Introduction
- Concept
- Methodology
- Design strategies
- Conclusion

Interconnect Design Space Abstraction

Interconnect Electrical Model



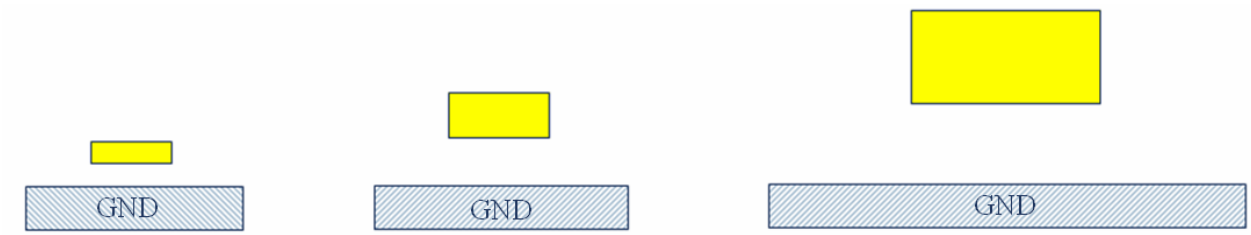
- R depends on the cross-sectional area (A)
  - Absolute quantity
  - Scaling variable

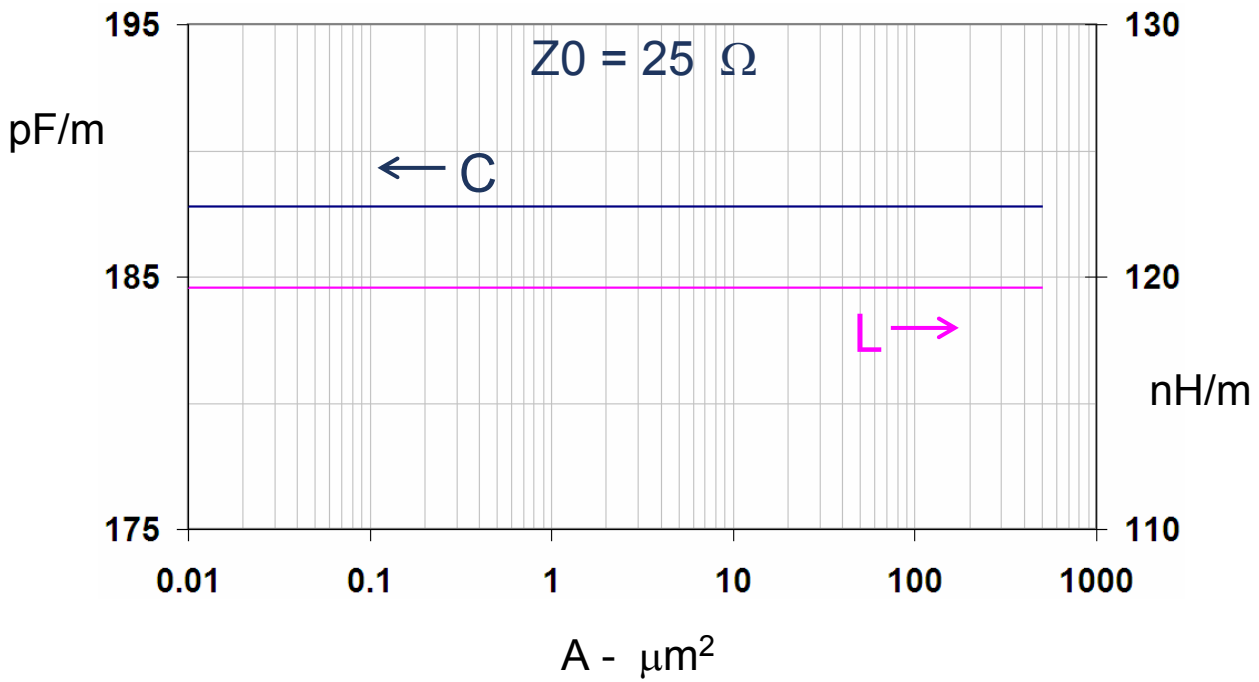
- L and C depends on spacing between adjacent lines
  - Relative quantity
  - Impedance Abstraction

$$Z0 = \sqrt{\frac{L}{C}}$$

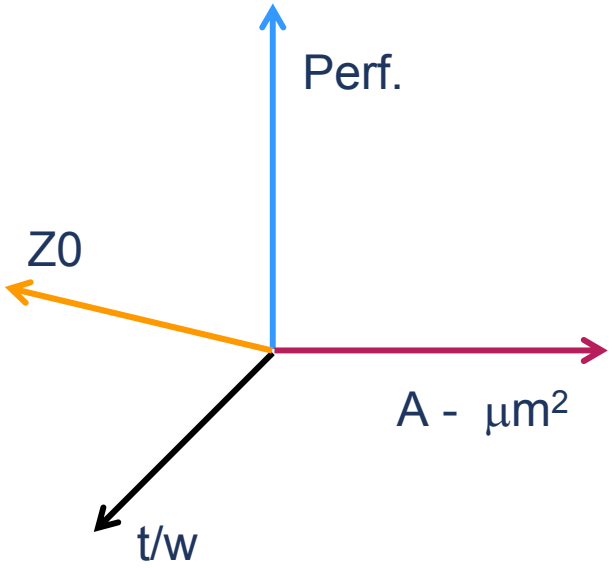
L and C can be fixed independent of A

Different A yet same Z0 !





Interconnect Design Space Abstraction



Complete Geometry

⇒ w, t, h_d, s

$$Z0 = \sqrt{L/C}$$

$A = w * t$

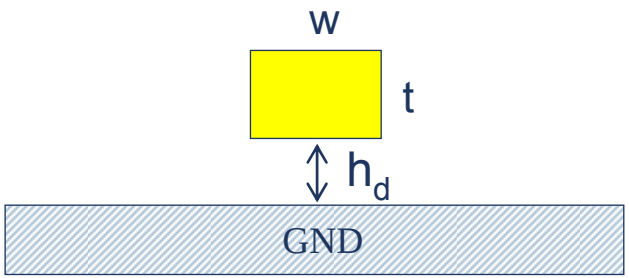
Power, Noise → Z0

Delay, Bitrate → A

Wiring density

Design Methodology – Fix Design Ratios

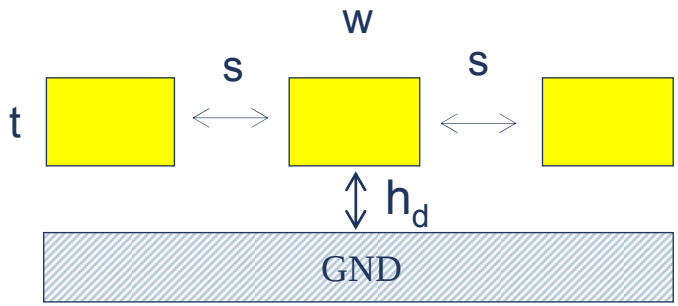
1. Find w/h_d, t/h_d



$$Z0 = f(w/h_d, t/h_d, \varepsilon_r)$$

Given t/w

2. Find s/h_d

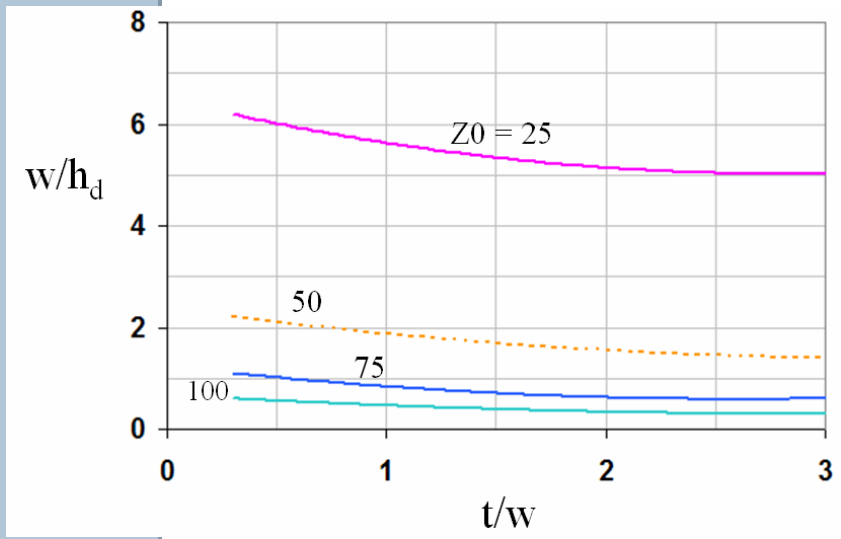


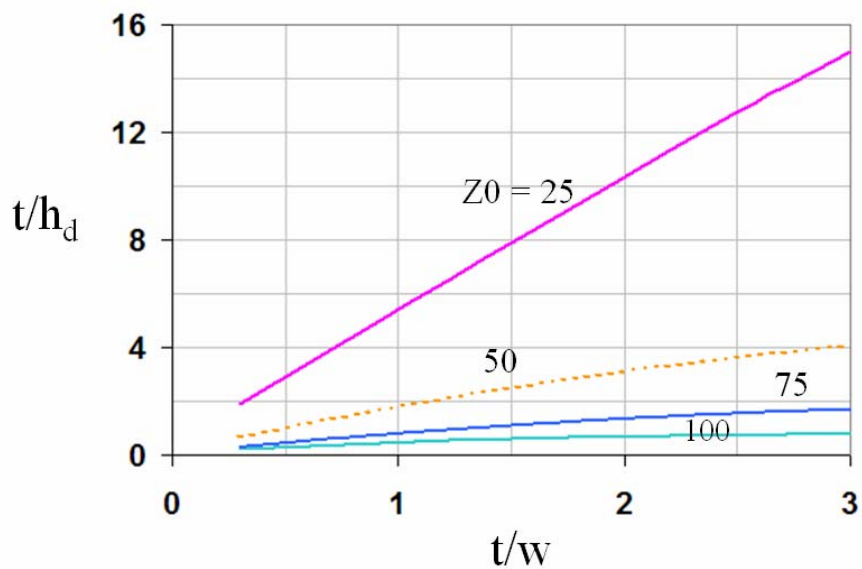
Xtalk <= 20% VDD

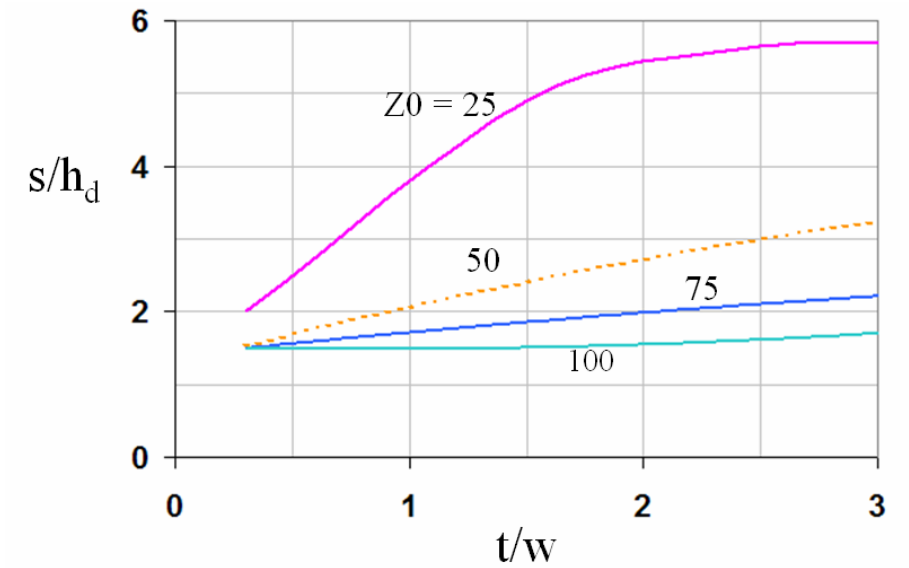
Impedance unchanged

Weak coupling

Design Ratios for different impedances







$\varepsilon_r = 2.7$

Given Z0 and A Wire Geometry is fixed

Given t/w

$$Z0 = f(w/h_d, t/h_d, s/h_d, \varepsilon_r)$$

$$ar_1 = w/h_d$$

$$ar_2 = t/h_d$$

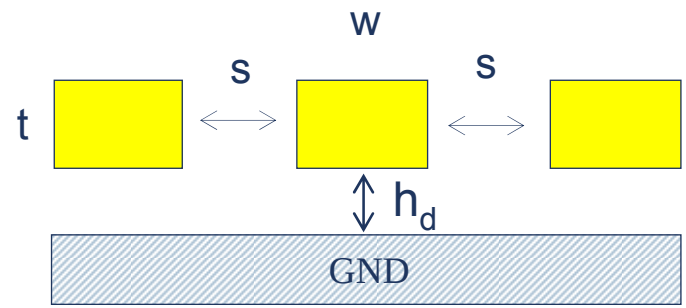
$$ar_3 = s/h_d$$

$$w = \sqrt{CD \times ar_1 / ar_2}$$

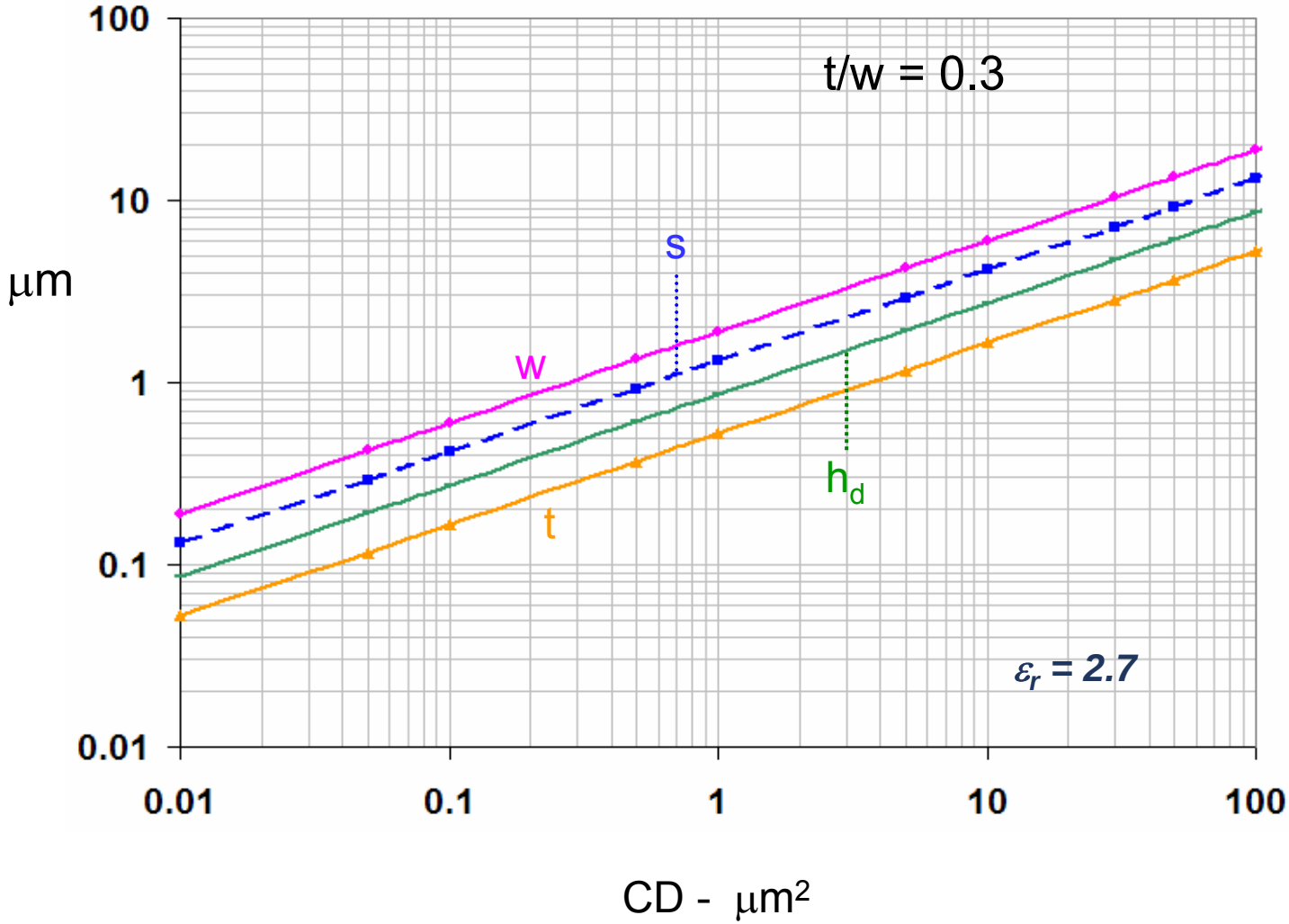
$$t = CD/w$$

$$h_d = w/ar_1$$

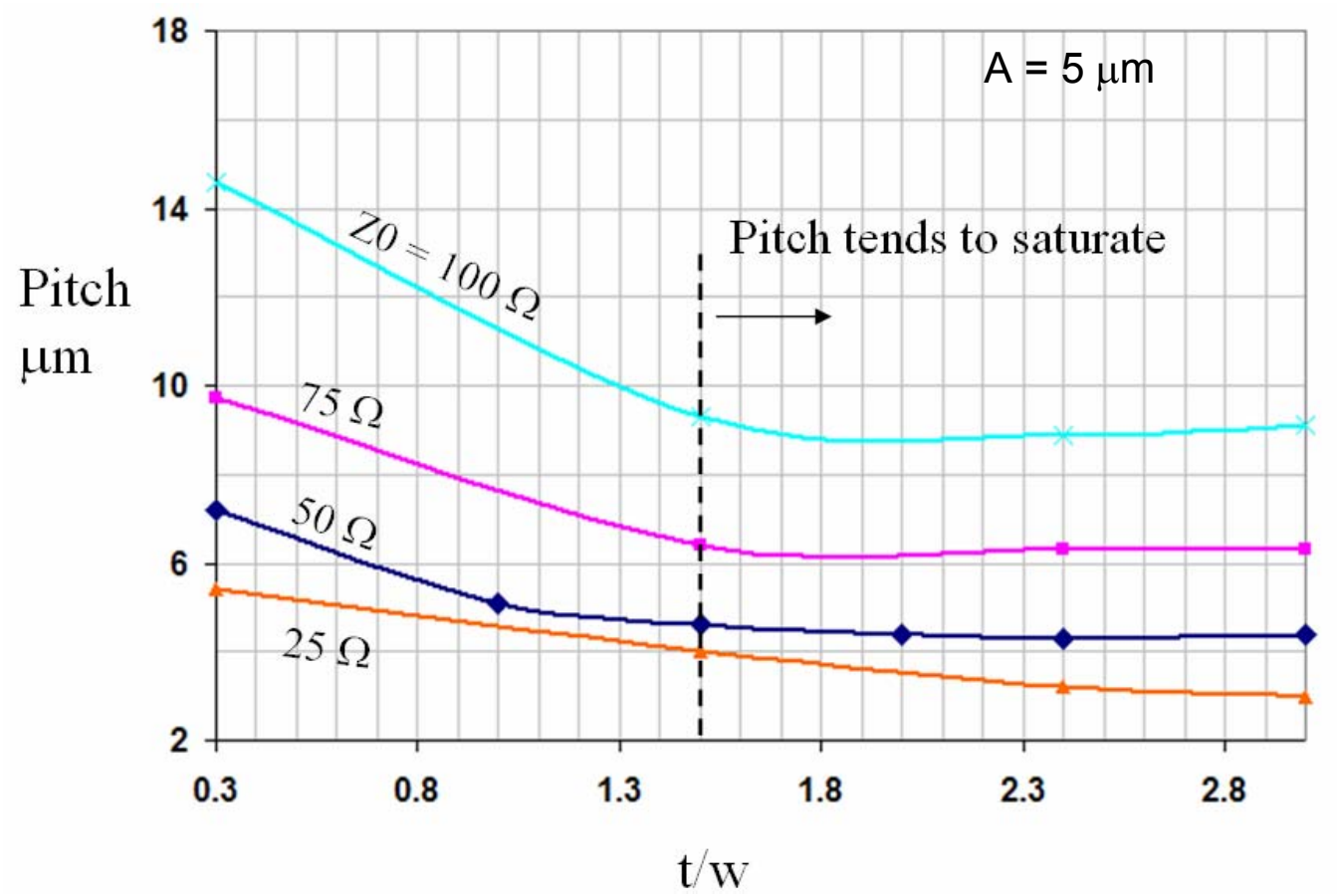
$$s = w \times ar_3$$



Wire Geometry Example: 50 Ω



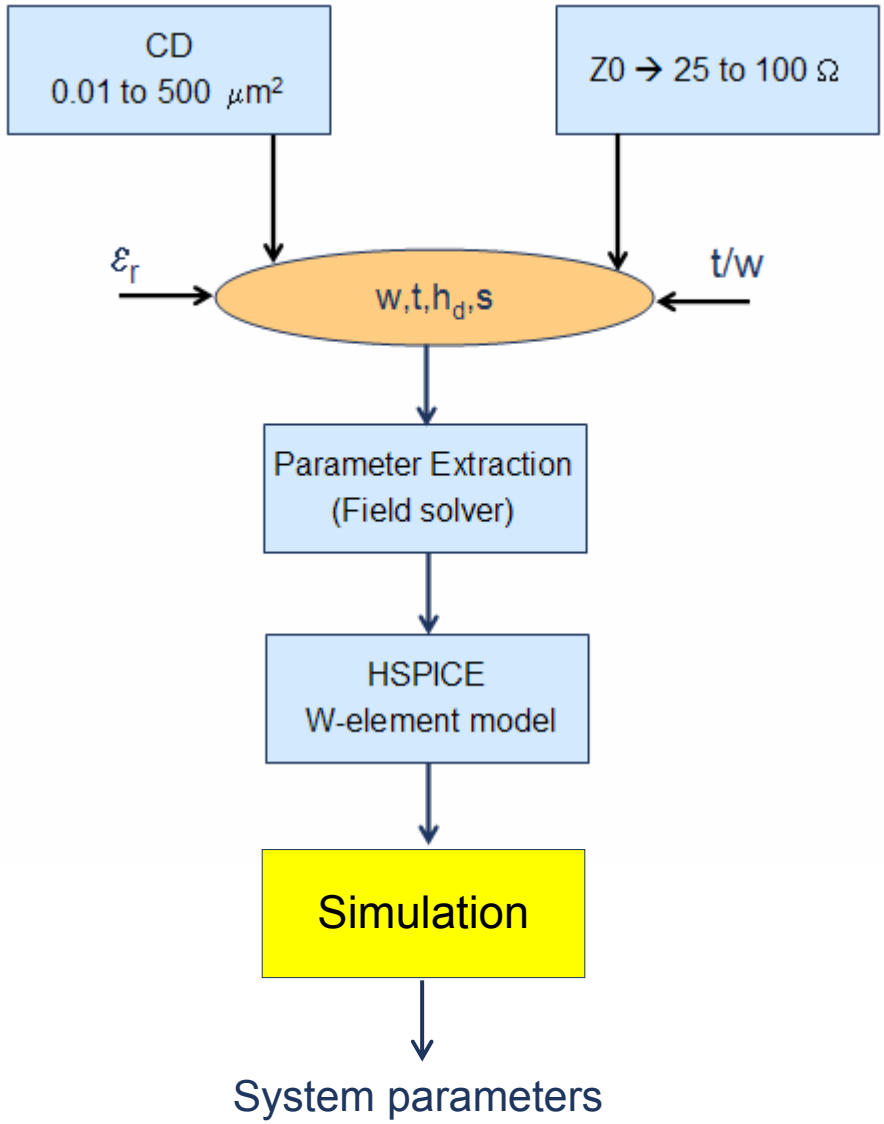
t/w is chosen to minimize pitch



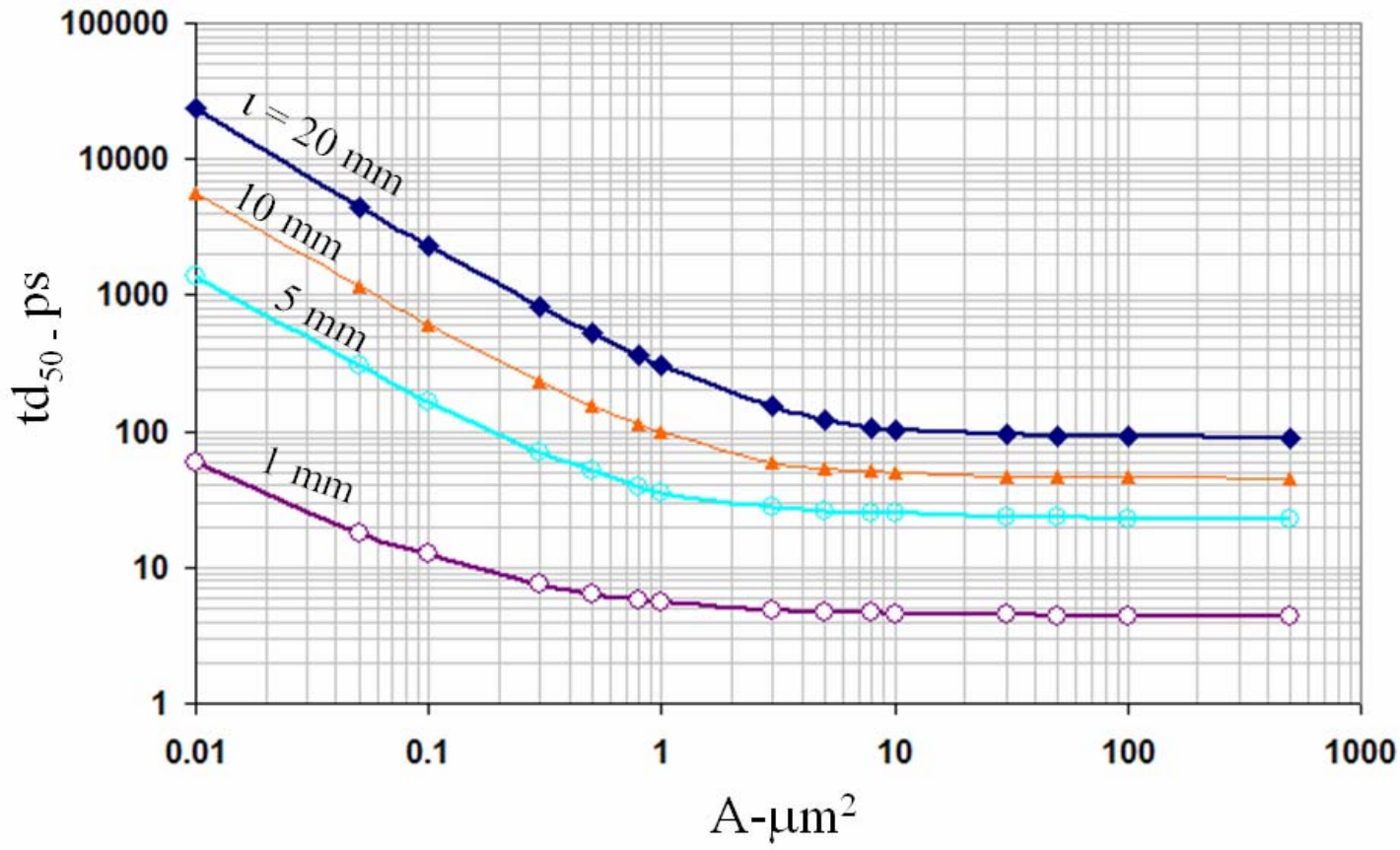
Pitch = w+s

- Same trends for all As
- t/w of *2.4* is considered

Interconnect Design Methodology

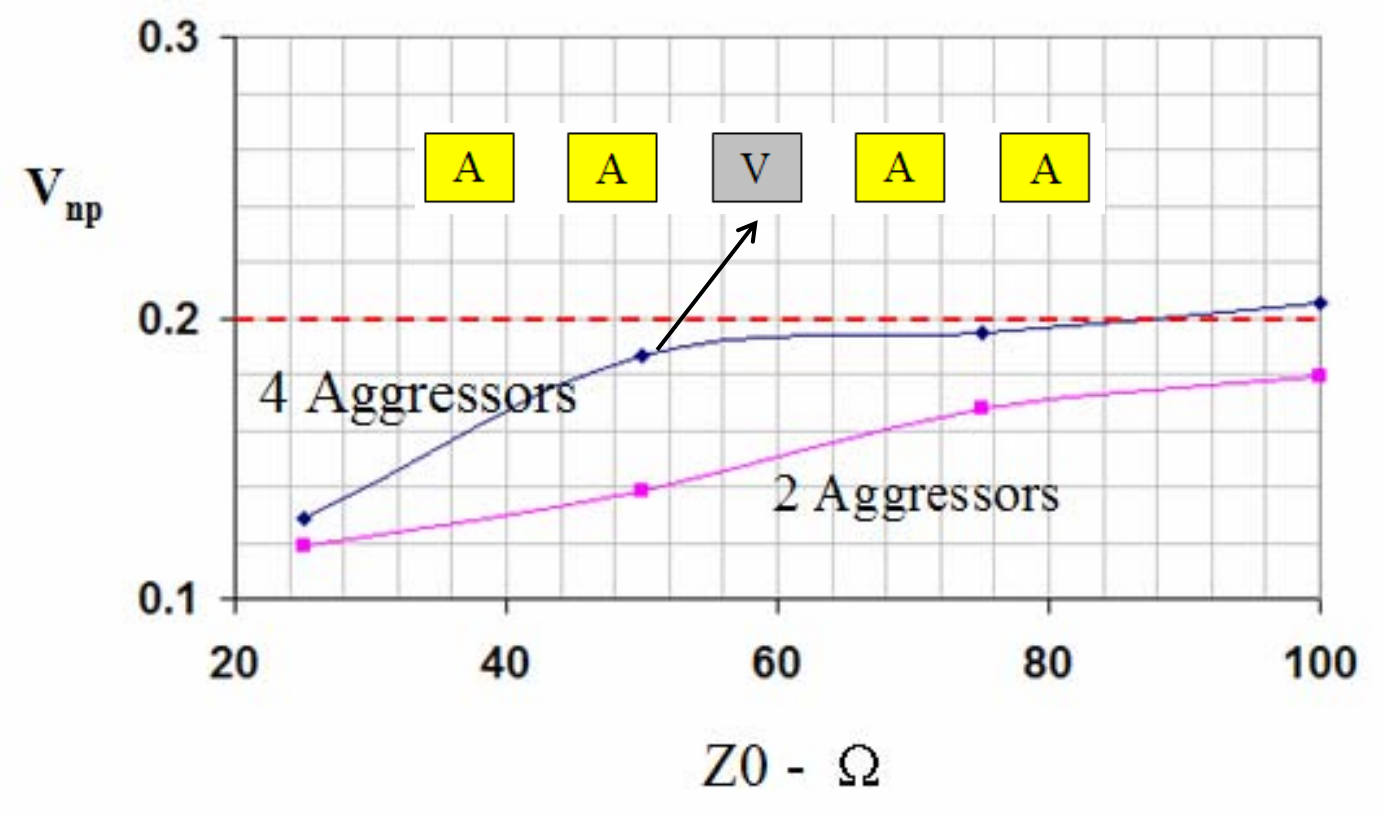


Delay Characteristics of 50 Ω line



- Rich data set linking geometry and system parameter - delay

Xtalk Validation



-Tolerable xtalk up to 4 Aggressors

- Lower Z0 ; lesser Xtalk

- Vnp fairly independent of A

Outline

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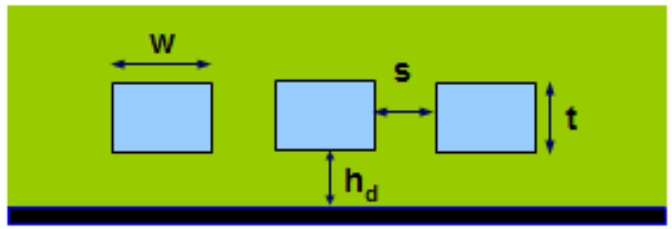
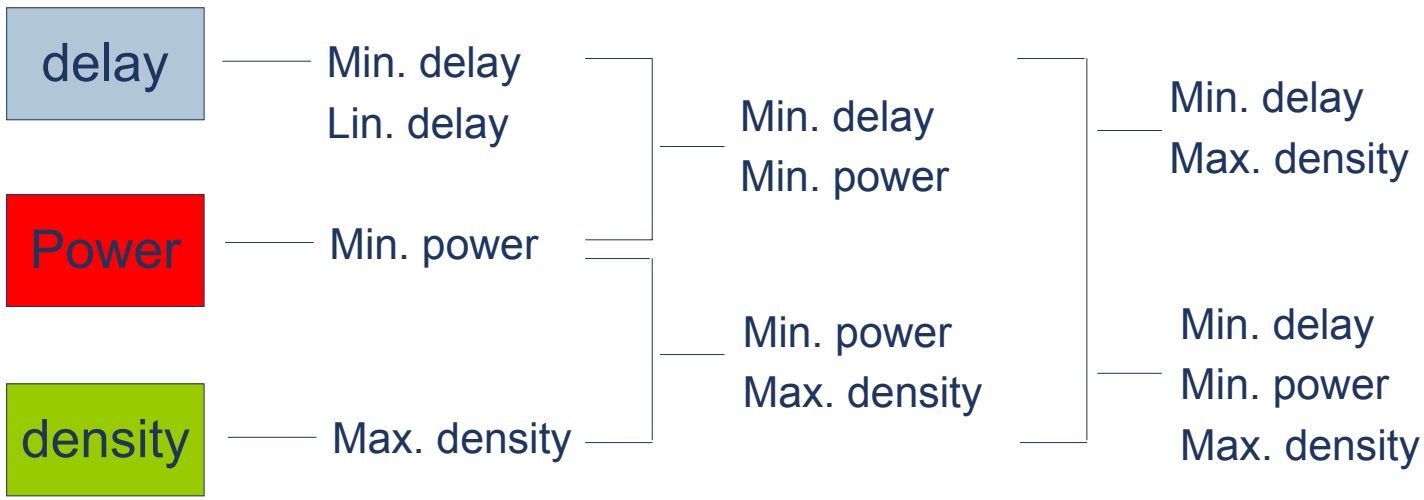
- Methodology
  - **Results**
- Design strategies
- Conclusion

Interconnect design Strategies

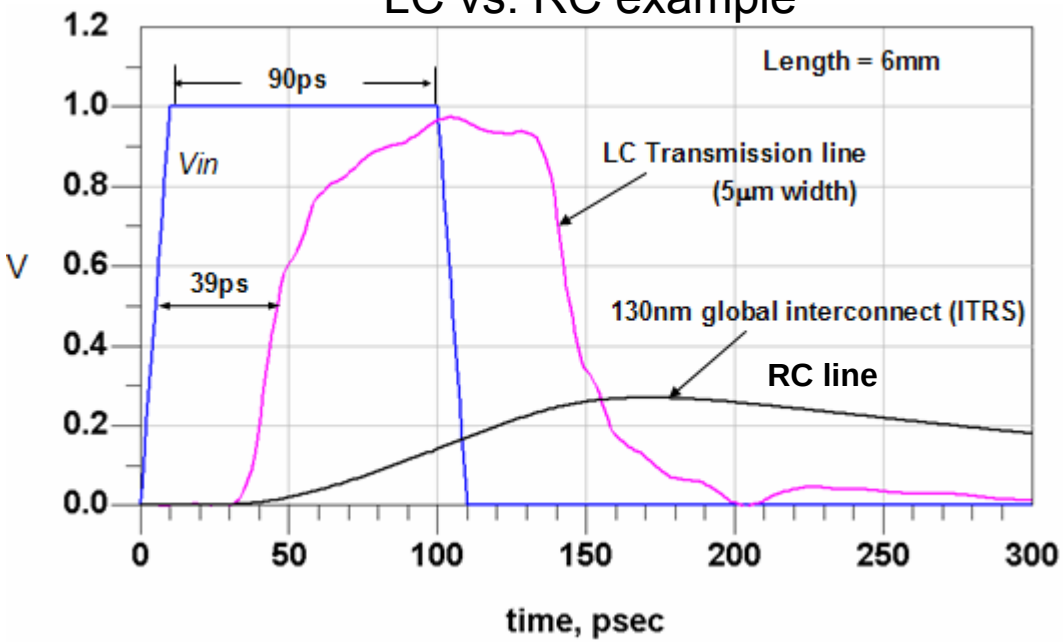




Strategy: Min. delay

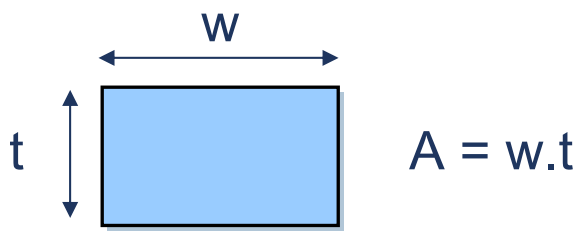
- Min. delay → LC Transmission lines
  - $\sqrt{\varepsilon_r}/c_0 = \sqrt{LC}$
  - Limited only by ε_r
  - Near speed of light propagation
  - *Large A*; delay independent of R

LC vs. RC example



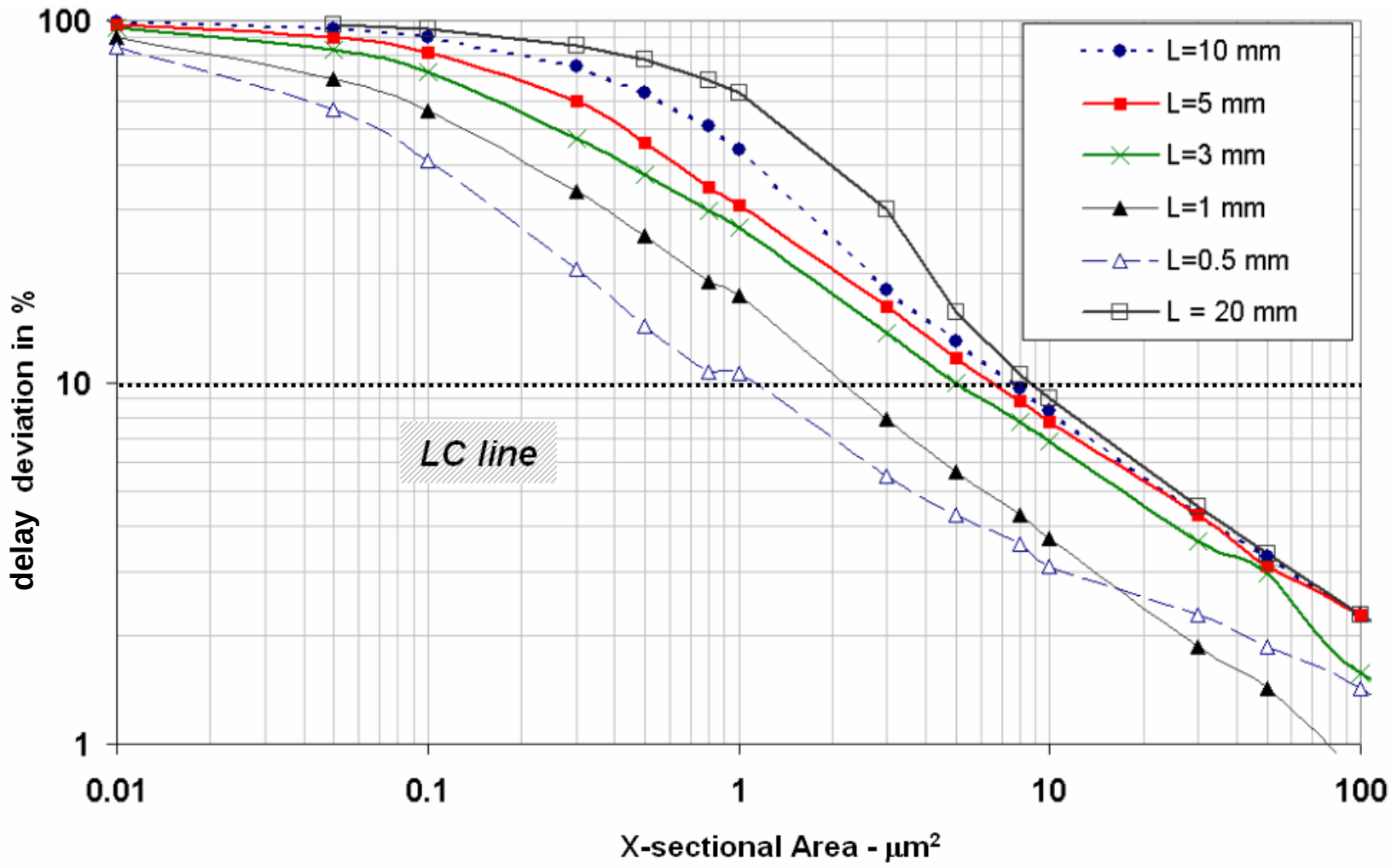
Min. delay - Problem Statement

- Find the minimum interconnect
  X-sectional area (Amin) required to achieve
  LC mode propagation
  for a given length ?

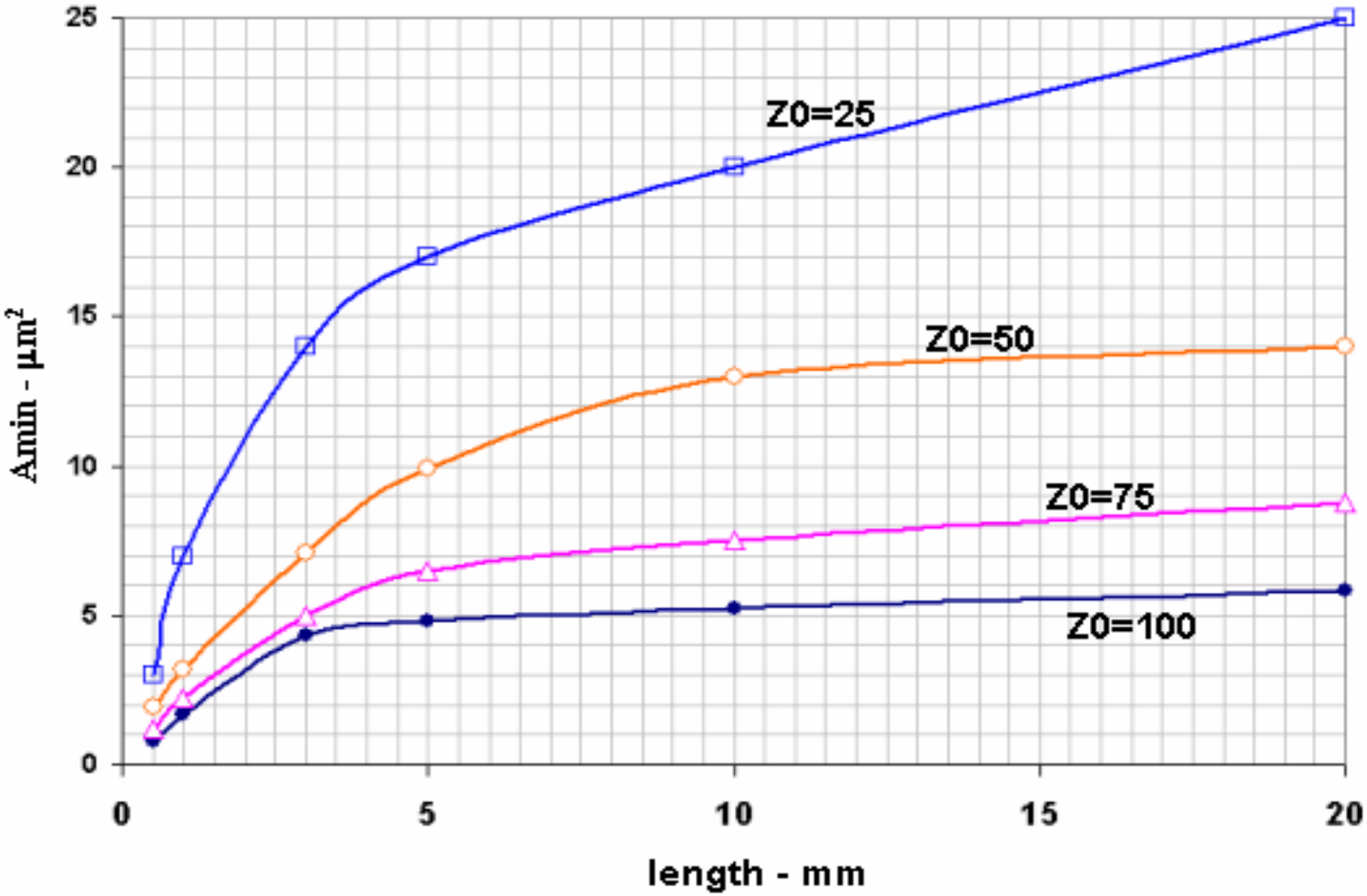


- LC mode propagation defined as delay with in *10% of Speed of light delay*

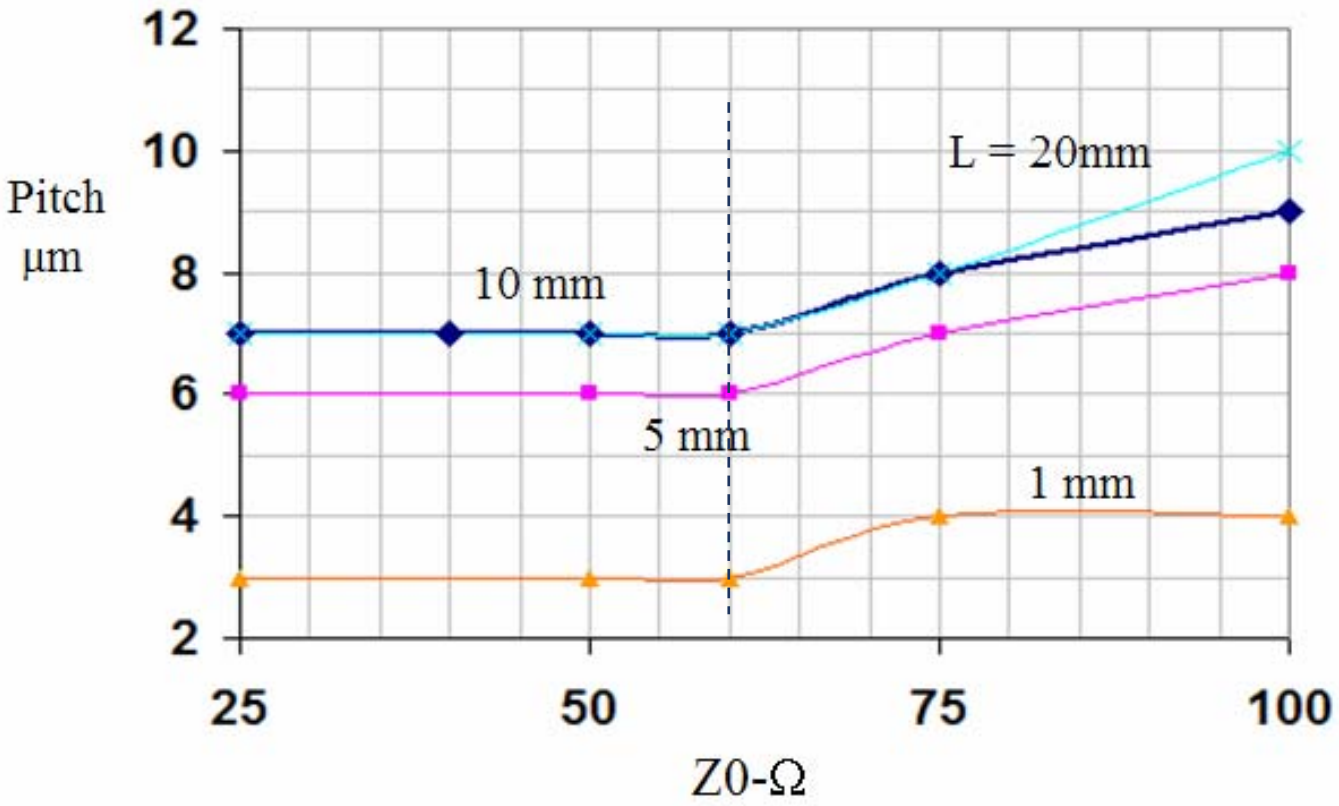
Amin = 7.6um² for 10mm long 75 ohm line for min. delay



Amin decreases for increasing Z0

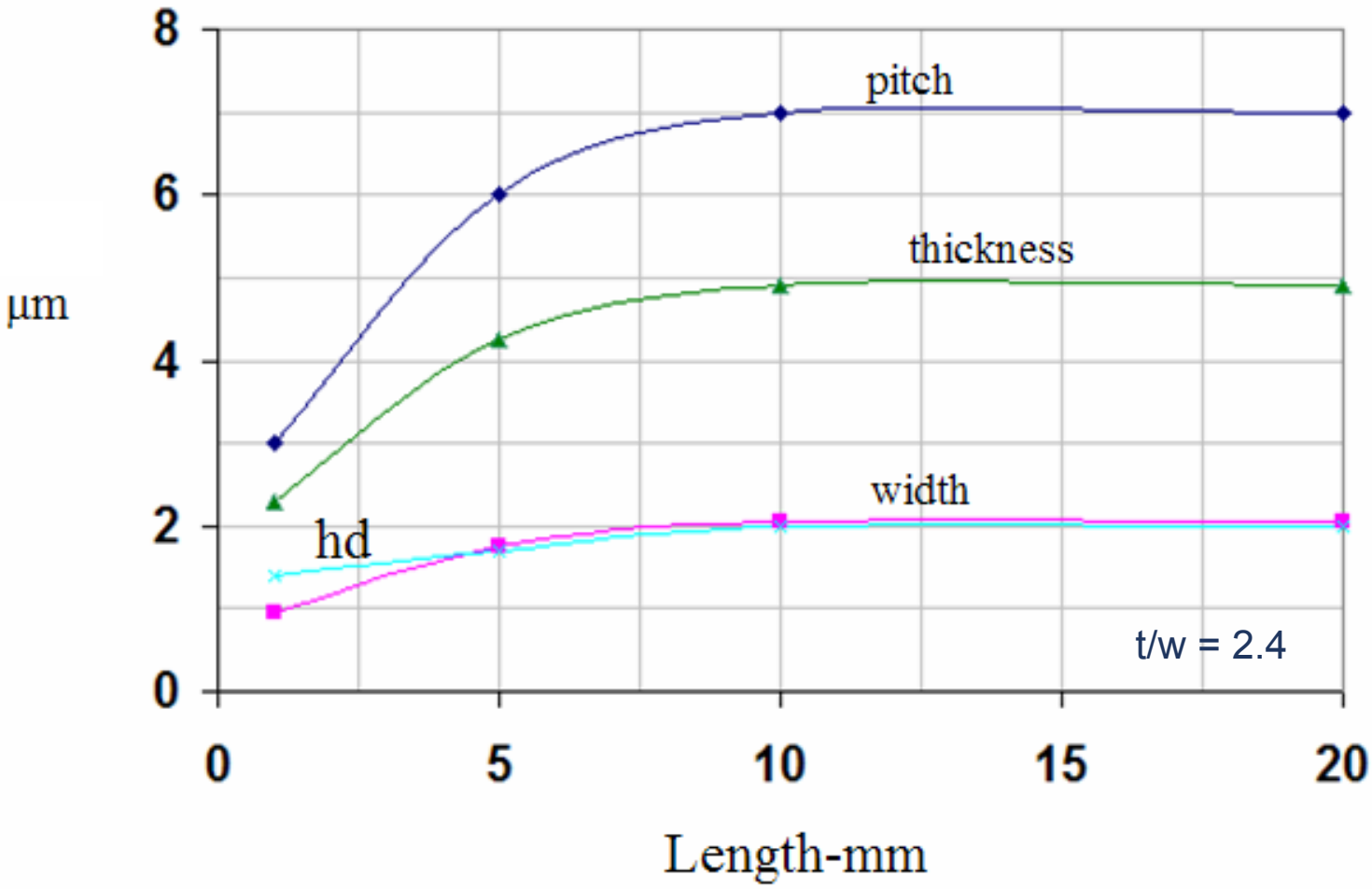


Pitch vs. Length under X-talk constraint



60 Ω - Optimal Z0 for Min. delay

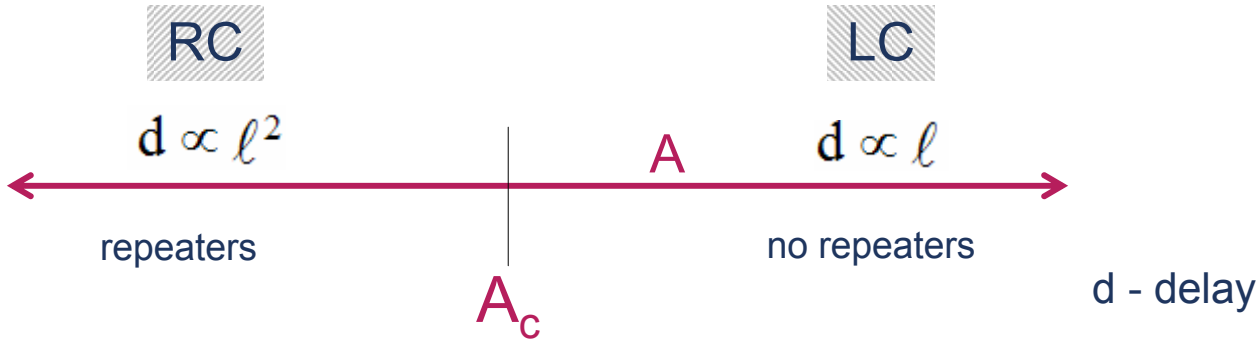
Optimal Geometry for LC Transmission lines



Design Strategy

Repeater Less Line

Repeater less line

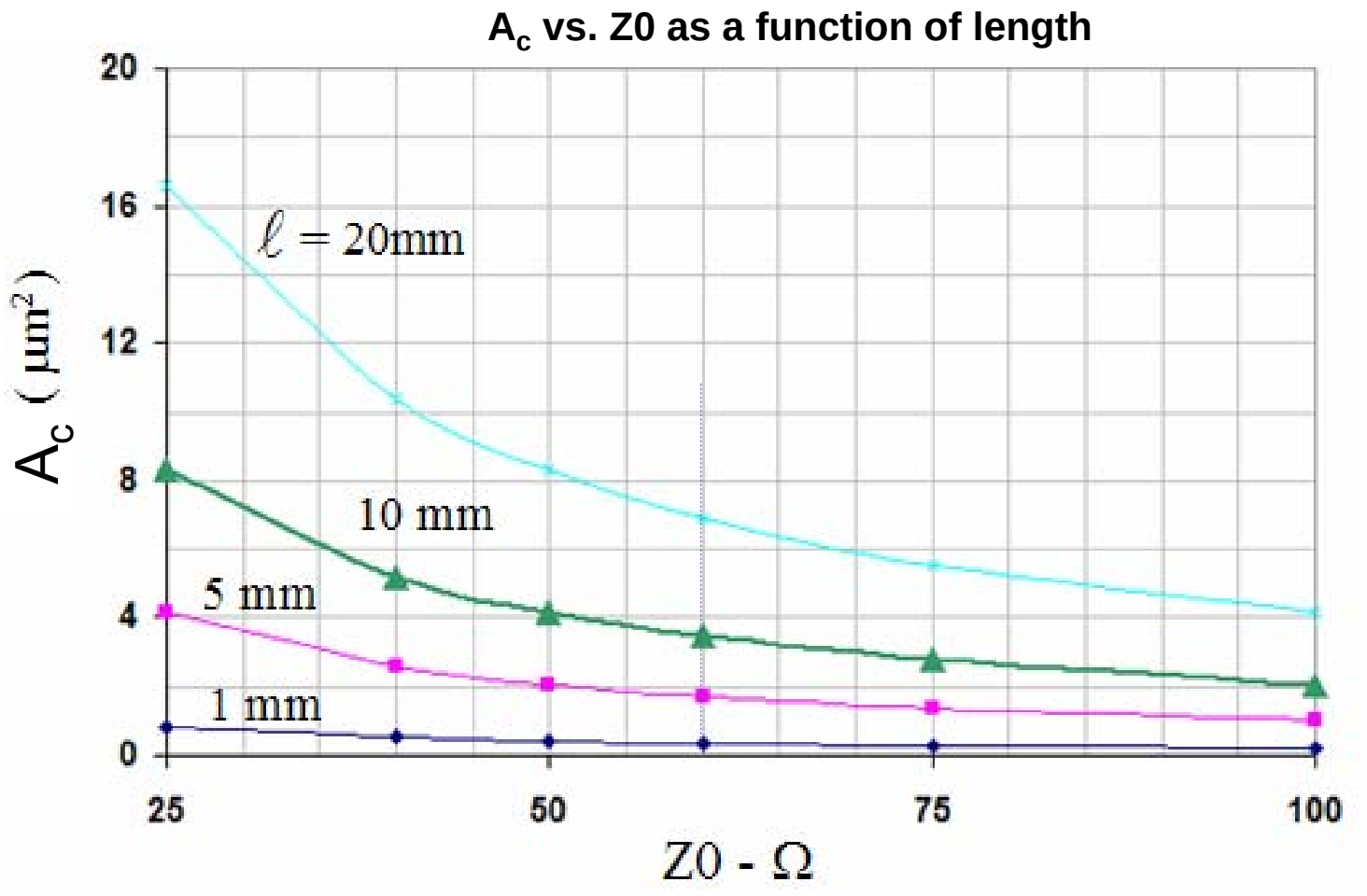


What is the RC-LC cutoff point (A_c) ?

Equating RC and LC delays

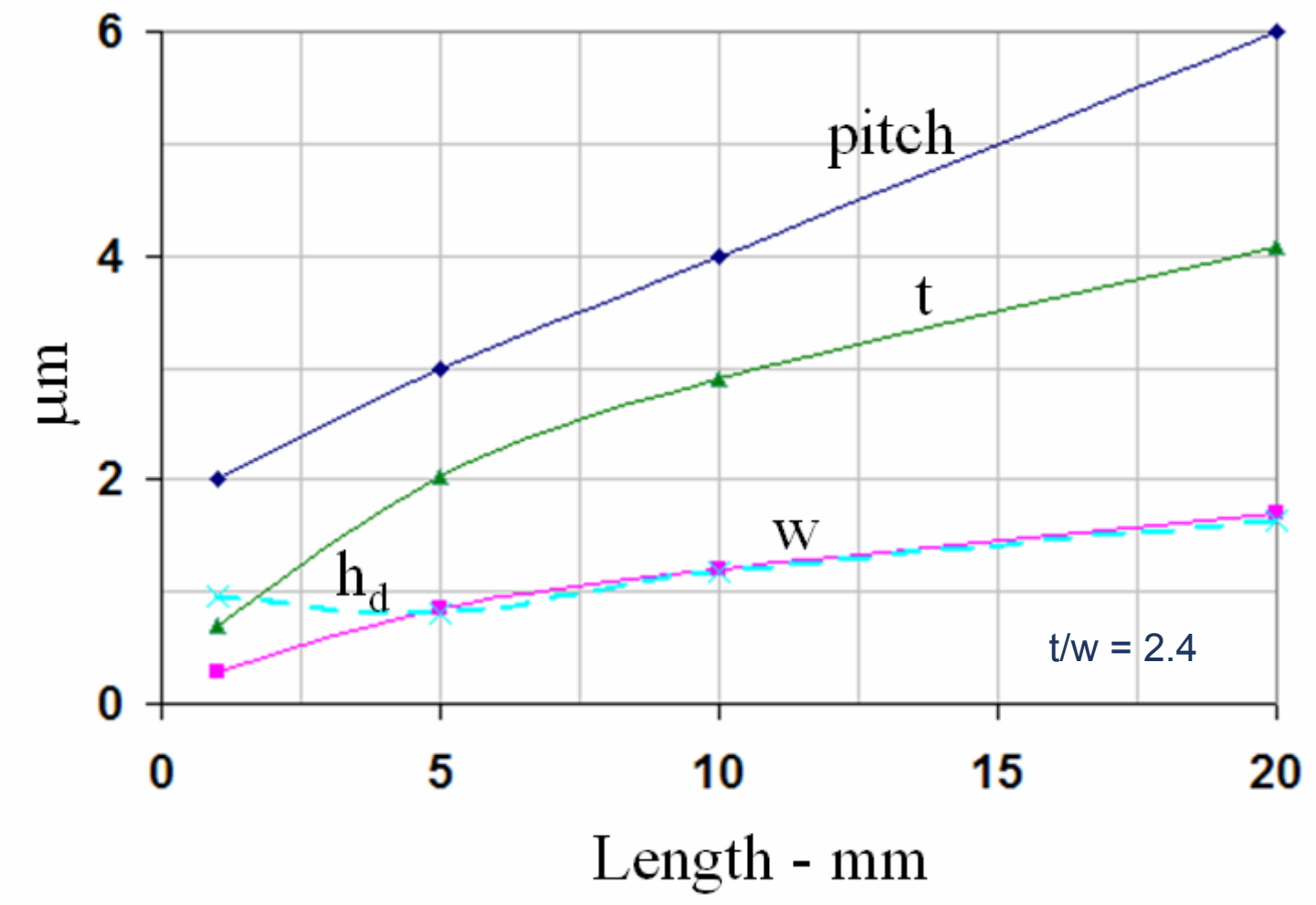
$$\Rightarrow \quad A_c = \frac{1.2\rho\ell}{Z0}$$

Ac decreases with Z0



- Optimal Z0 = 60 Ω

Optimal Geometry for Repeater less line



Design Strategy

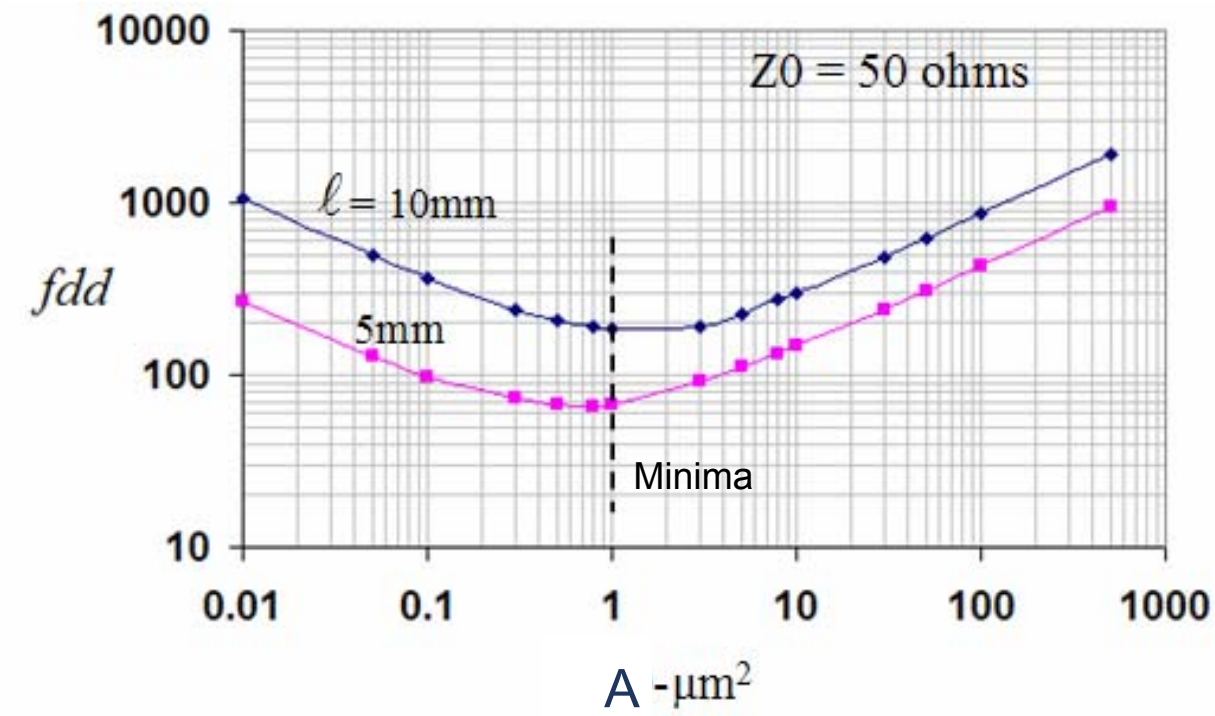
Min. Delay

Max. Wiring density

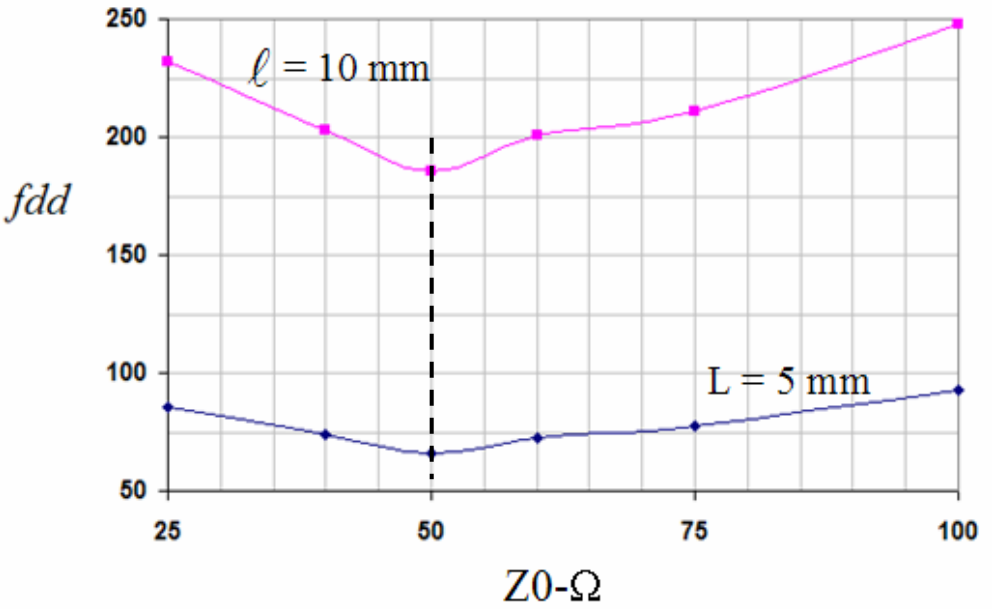
Strategy: Min. delay, Max. Wiring density

Define figure of merit

$$fdd = \min\left(\frac{delay}{density}\right) = \min(delay.pitch)$$



Strategy: Min. delay, Max. Wiring density



Optimal Z0 = 50Ω

Optimal Geometry for L = 10 mm

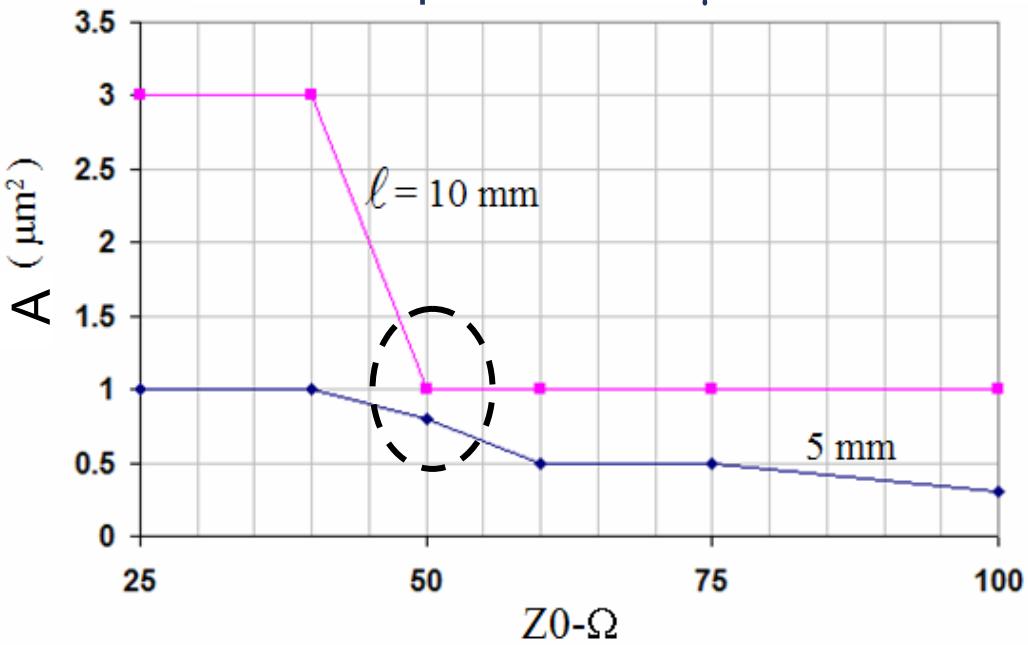
W = 0.65 μm

t = 1.55 μm

h_d = 0.44 μm

P = 2 μm

Optimal A = 1μm²



Design Strategy

Min. Delay

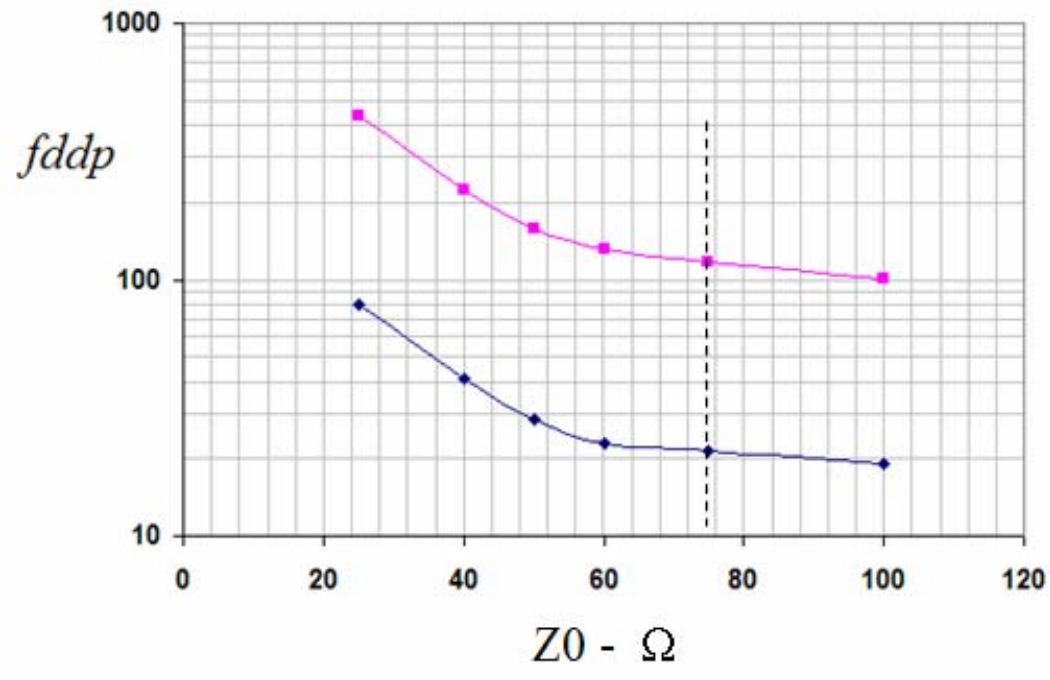
Min. Power

Max. Wiring density

Strategy: Min. delay, power and Max. density

Define figure of merit

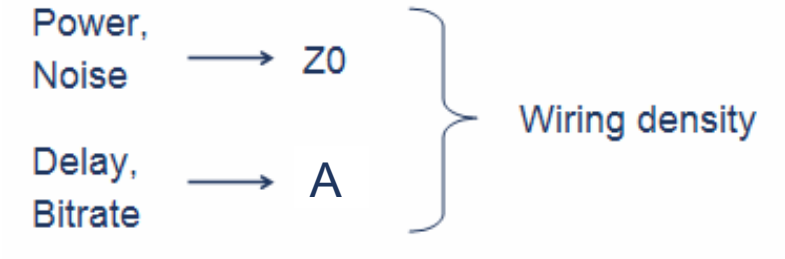
$$fddp = \min\left(\frac{delay \times C}{density}\right) = \min\left(delay \times pitch \times C\right)$$



- Optimal Z0 = **75 Ω**
- Optimal A = **1μm²** for line lengths of 10mm

Conclusion

- Constant impedance Scaling
  - Systematic Approach to interconnect design



- Design strategies

- Applications
  - Interconnect stack technology development
  - On-chip global interconnects
  - Package level interconnects

Thank you

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Backup Slides

Interconnect Simulation Model