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Interconnection Lengths and Delays Estimation for Communication Links in FPGAs

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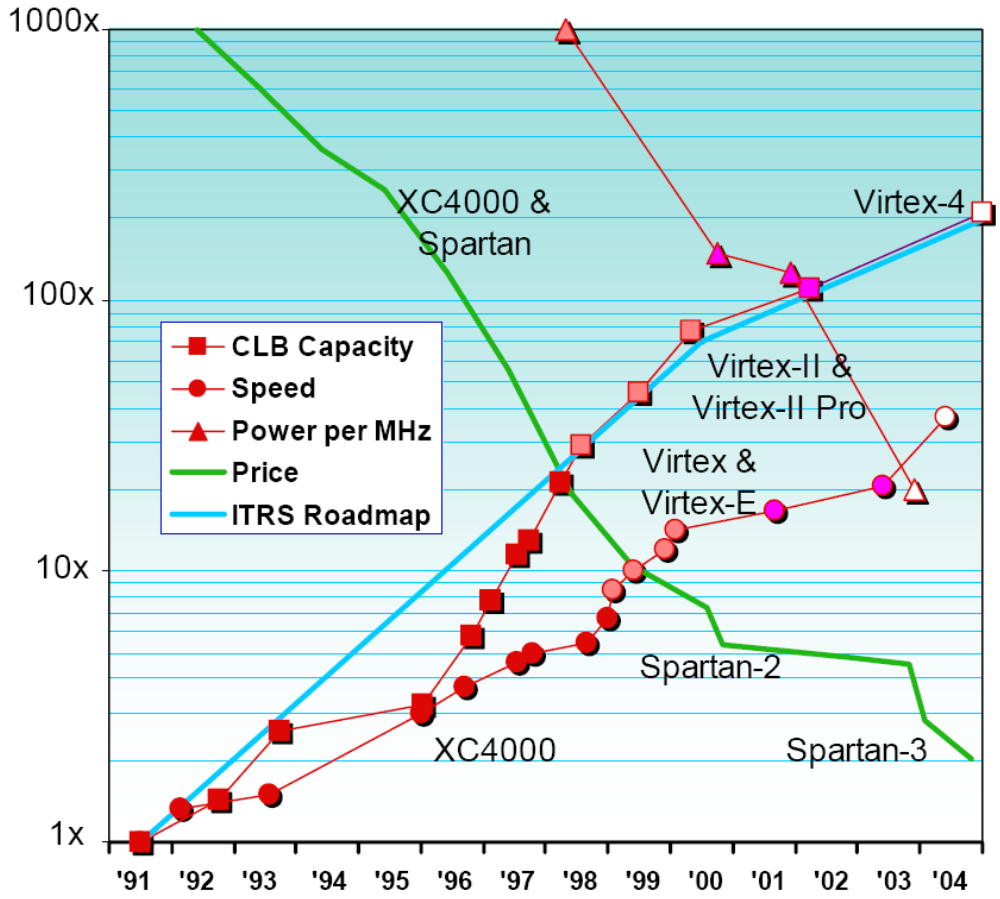
Outline

- Introduction
  - Inter-Module Communication in FPGAs
- Background
  - Communication link and FPGA routing architecture
- Interconnection Length Estimation
  - A stochastic approach
  - Number of interconnections and length at each channel
- Comparison with Experiments
- Delay Estimation
  - Based on the length estimates
- Potential Applications and Future Work

The Ever-Increasing Capacity

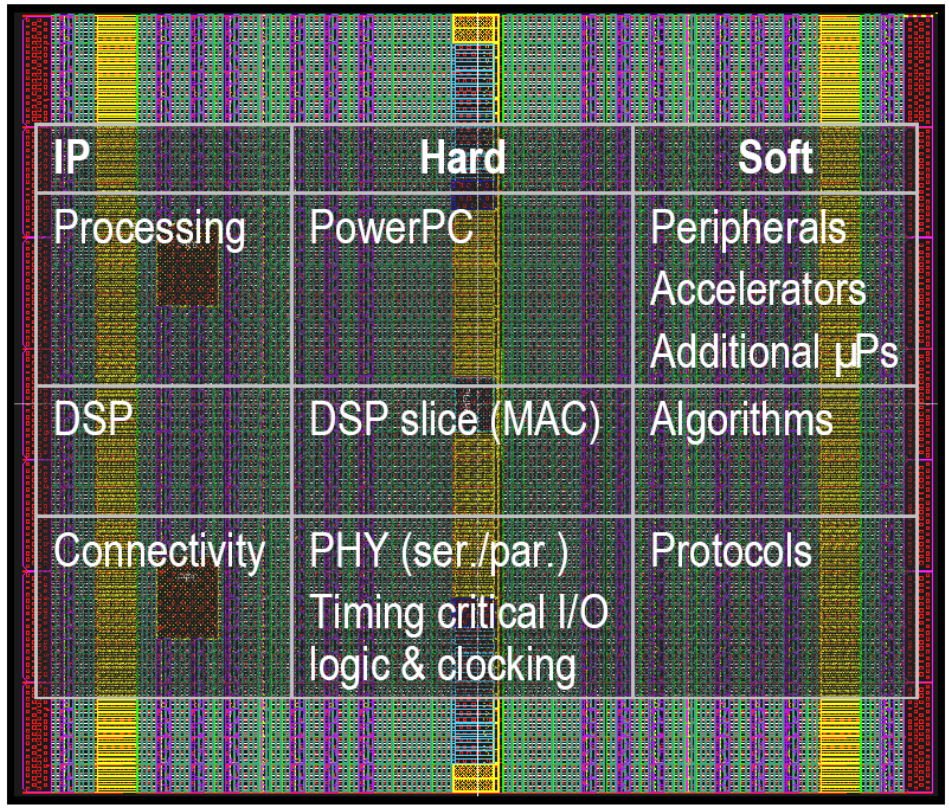
- The FPGAs capacity grows exponentially
- Complex system can be implemented in a single-FPGA
- Towards a module-based design



Source: Xilinx, 2005

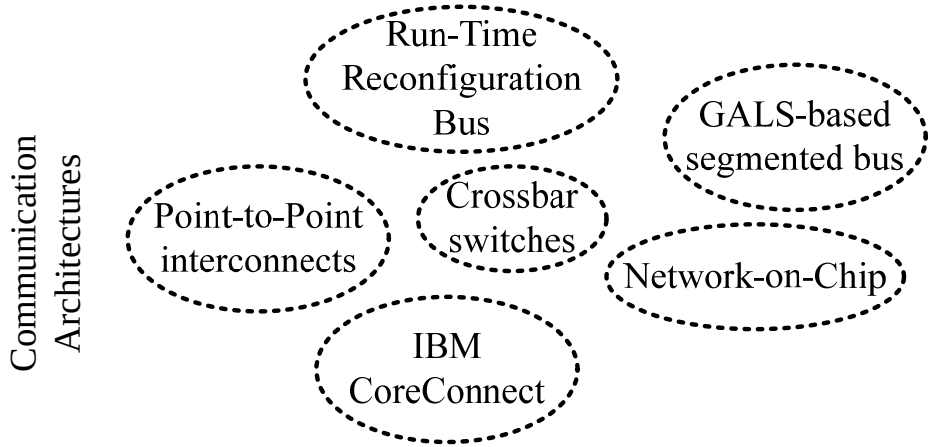
Modules on FPGAs

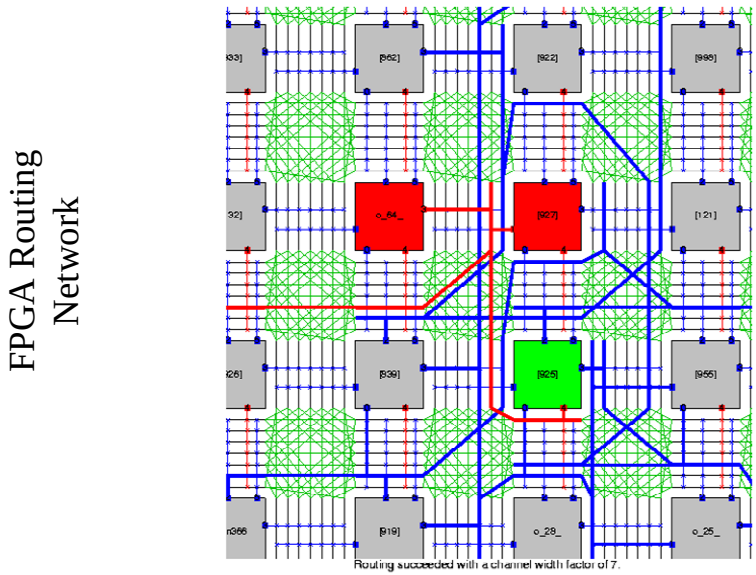
- Embedded blocks and Soft-IPs are available
- System design by connecting these modules
- Required efficient interconnection architecture
- What does the communication architecture look like?



Communication Architectures and FPGA Routing Network

- Various on-FPGA communication architectures have been proposed
- A survey can found in (Mak *at el.*, FPL'07)
- How to predict interconnections lengths and delays for communication architectures in FPGAs?

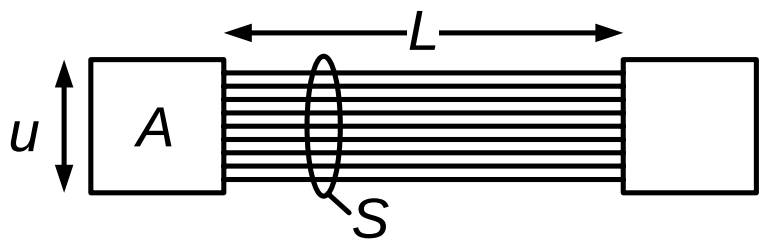




Related Work

- Analytical approach
  - Rent's Rule (Donath, Stroobandt)
  - Stochastic method (Davis *et al.*, Brown *et al.*)
- Empirical Approach
  - Heuristic search (Balachandran *et al.*)
  - Statistical analysis (Manohararajah *et al.*)
- A more focus method dedicated for communication link and FPGAs

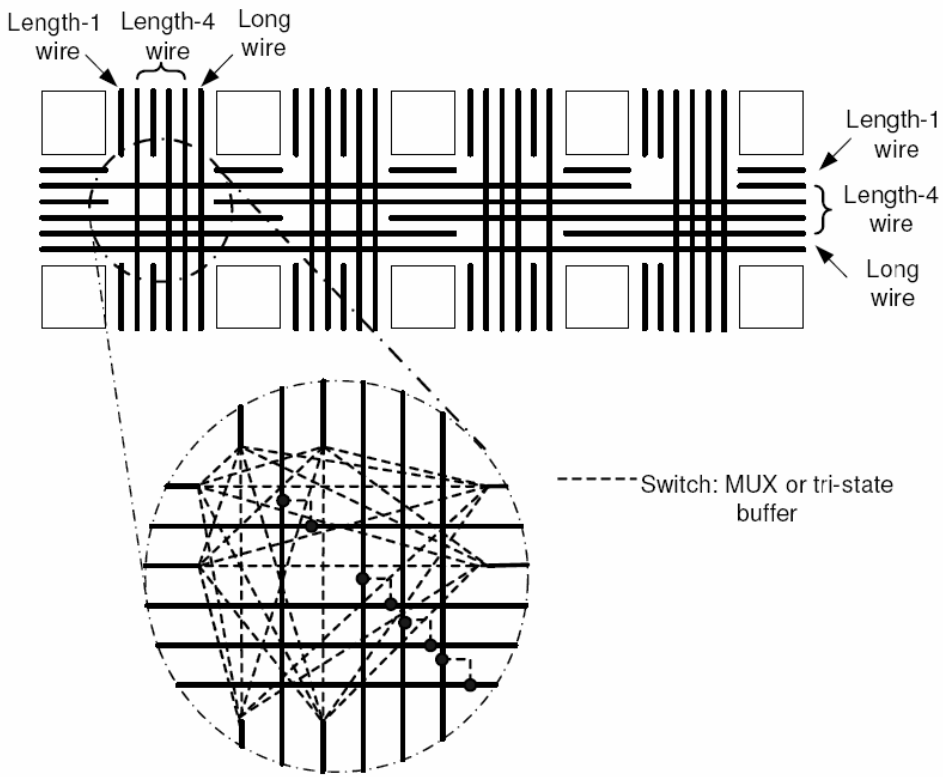
A Simple Link on FPGA



- Physically separated by a long distance (*L*)
- The total number of wires are known (*S*)
- Random placement within the constraint area (*A*)
- Width and length of placement area can be constrained

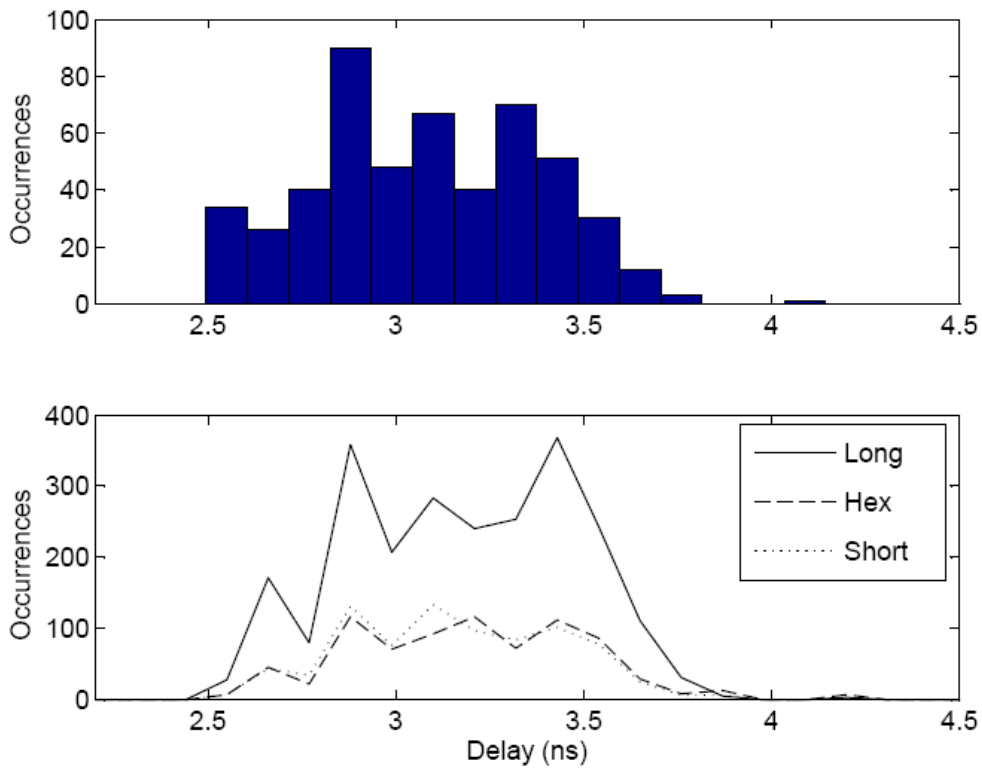
FPGA Routing Architecture

- Wires of different lengths
- Limited number of wires at each channel
- Design of switching fabrics

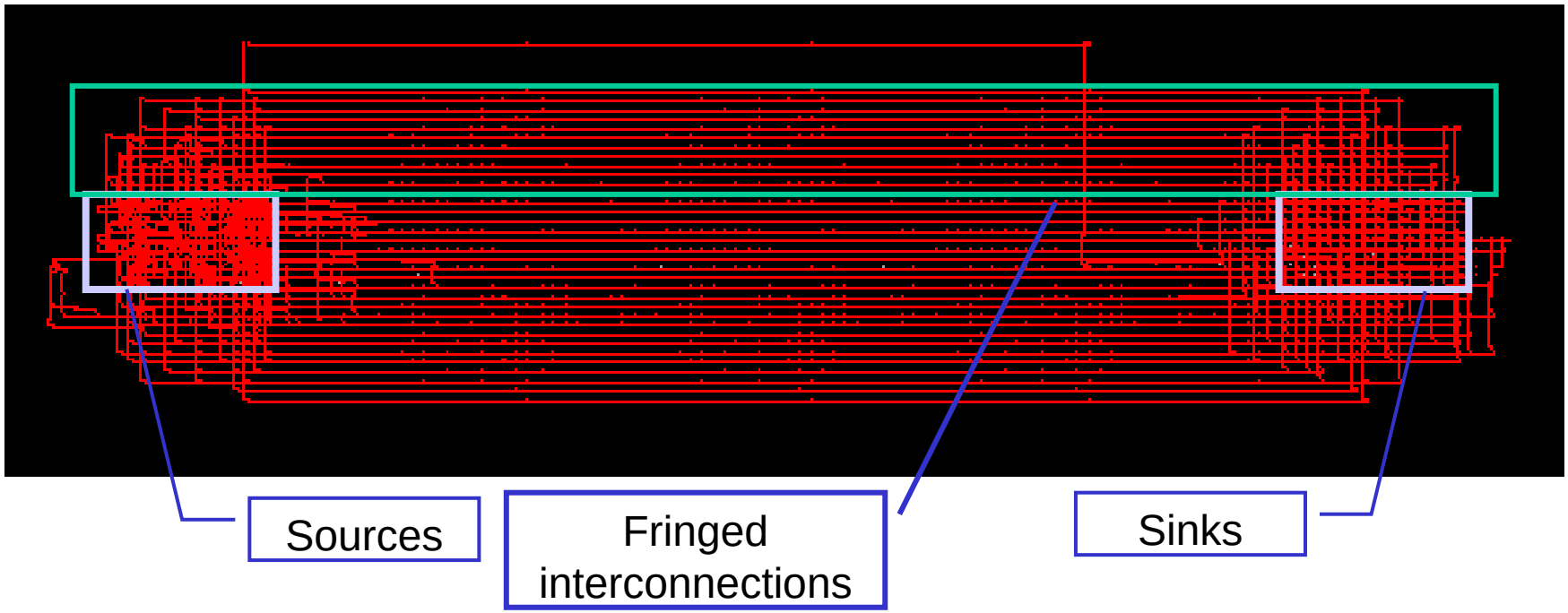


FPGA Routing Architecture (Long links)

- Can be approximated by Gaussian (Average and Worst highly correlated)
- Long wires dominate the delay
- Within the placement area, only short wires will be consumed

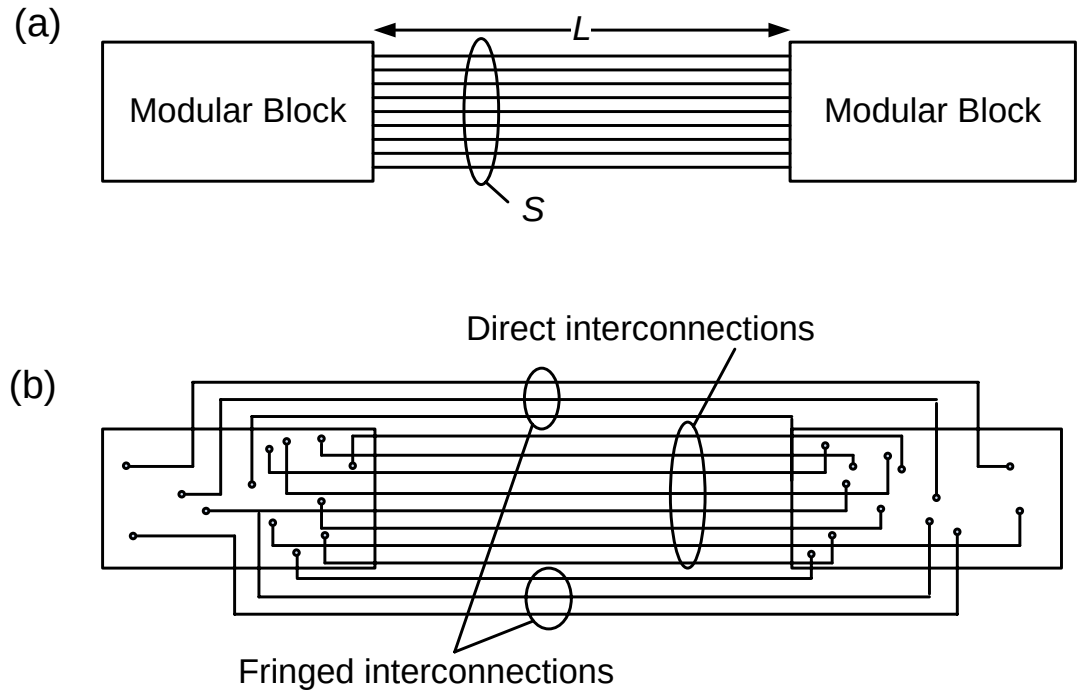


FPGA Routing Architecture (Long links 2)



FPGA Routing Architecture (Long links 3)

- Fringed interconnections tend to be longer
- Aspect ratio of the sources and sinks area
- Number of long wires in the channel is limited
- Random endpoint placement



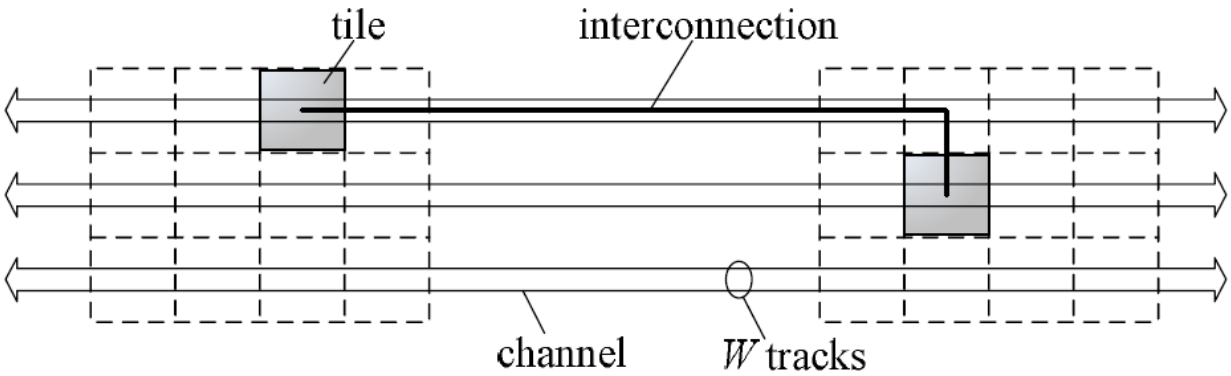
FPGA Routing Architecture - Summary

W: Number of long line wires at each channel

S: Total number of lines

u: Width of the placement area

v: Length of the placement area



- Assumptions
  - Channels are symmetric
  - Random placement of end points
  - Fully routable and always travels shortest path within the placement area
  - Wires are all traversed from one end to the other

Interconnection Length Computation

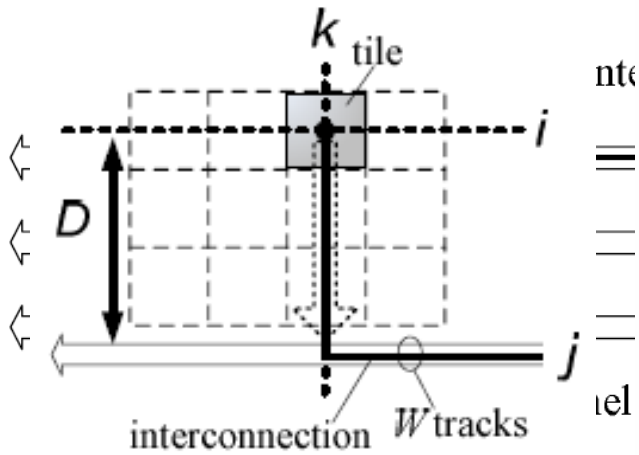
- Average length $R = \sum_{l=1}^{S} \xi_l / S$
- Link the interconnection length to the physical architecture

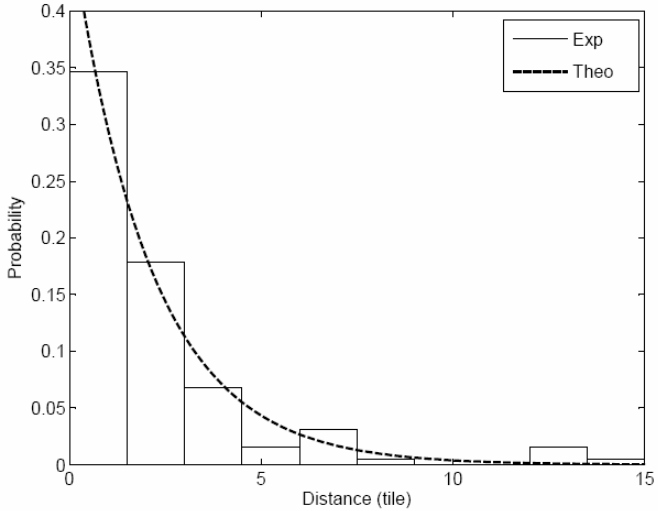
(1) $X_{i,j}$ = length of the i-th interconnection that is going through channel j.
(2) Y_j = total number of interconnections at channel j.

$$\sum_{l}^{S} \xi_l = 2 \sum_{j}^{N} \sum_{i}^{Y_j} X_{i,j}$$

$$E[R] = \frac{2}{S} \sum_{j=1}^{N} \overline{X}(j) \overline{Y}(j)$$

Derivation of $\overline{Y}(j)$





- Probability of an interconnection generated from a tile at row *i* and join channel *j*

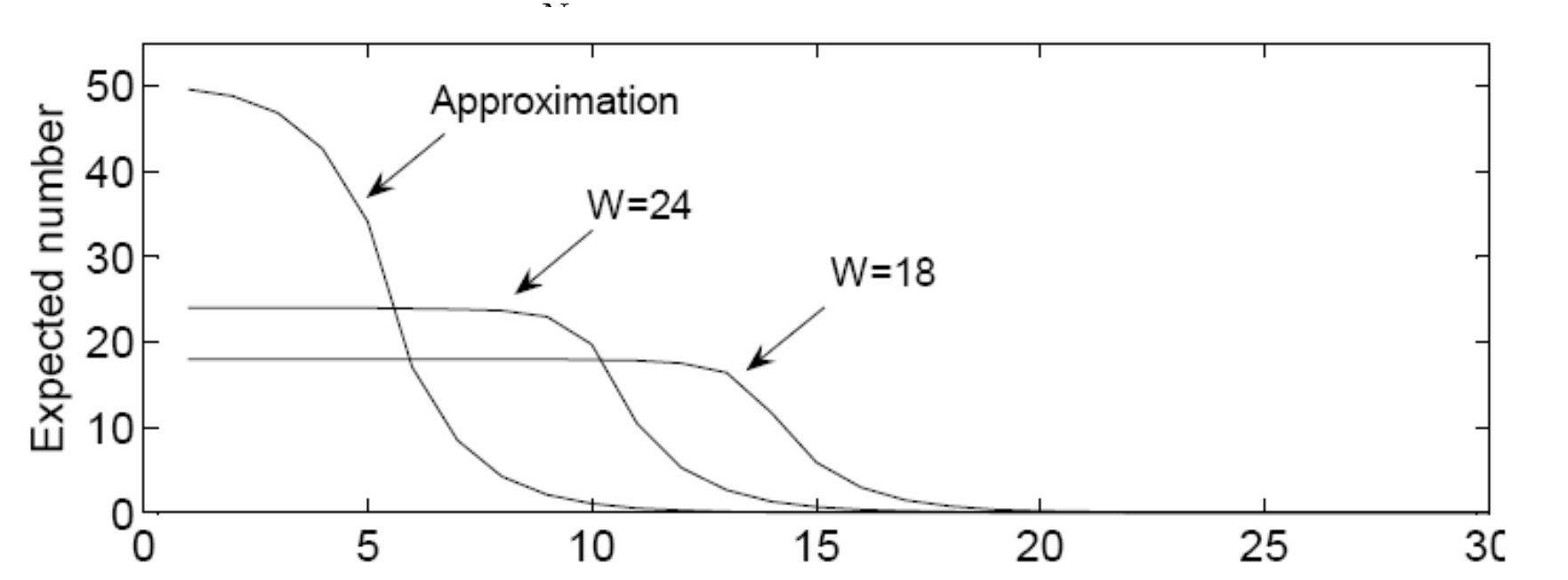
$$z_{ij} = \kappa\theta h_{\lambda_h, d(i,j)} = \kappa\theta(1-\lambda_h)^{d(i,j)}\lambda_h$$

- Probability of channel *j* has *y* interconnections

$$P\{Z_j = y\} = \frac{\lambda_j^y}{y!}\sum_{i=0}^{W}\frac{\lambda_j^i}{i!}, y \le W$$

Derivation of $\overline{Y}(j)$ (continue)

- Number of interconnections at channel *j* conditioned on *S*

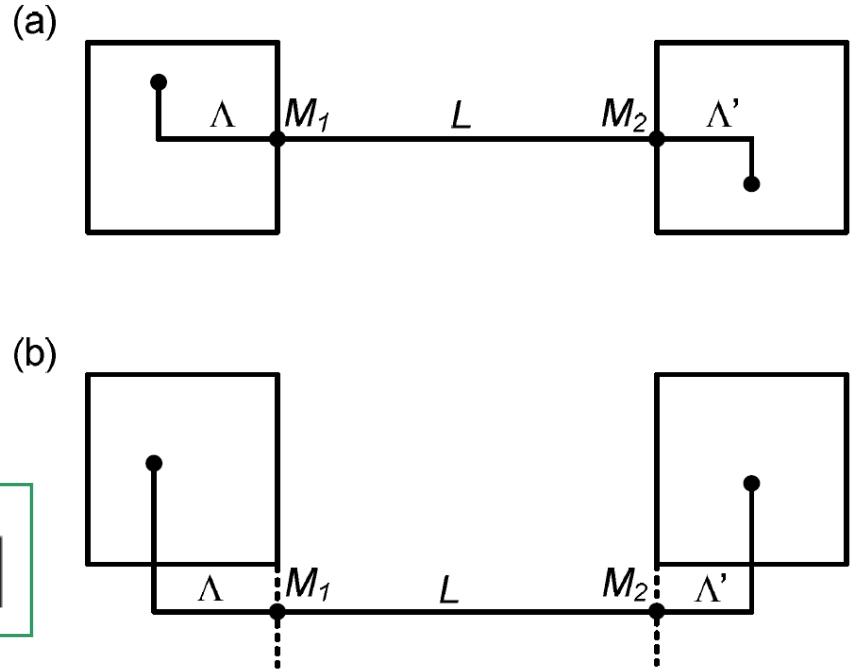


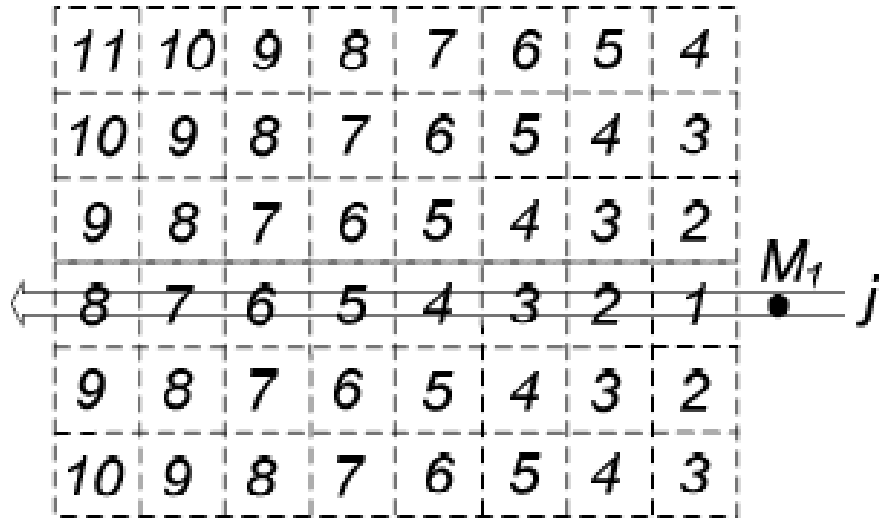
Derivation of $\overline{X}(j)$

- Expected length is sum of three segments

$$\overline{X}(j) = E[X_j] = L + 2E[\Lambda_j]$$

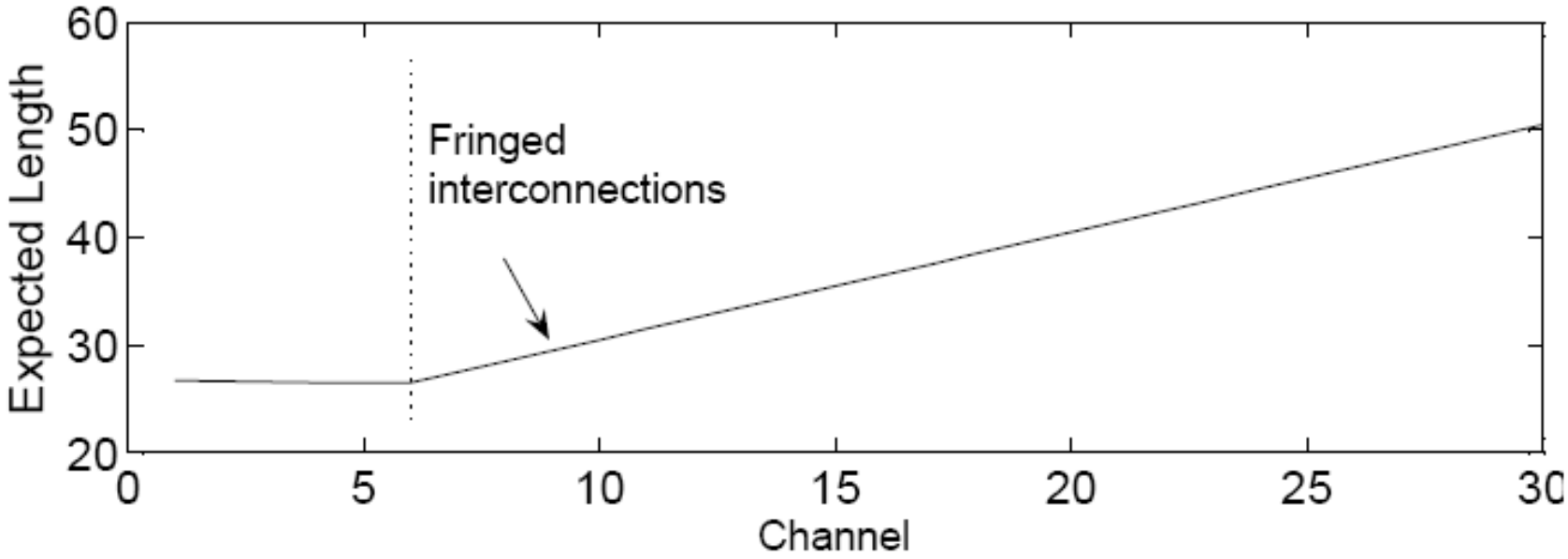
- Manhattan distance



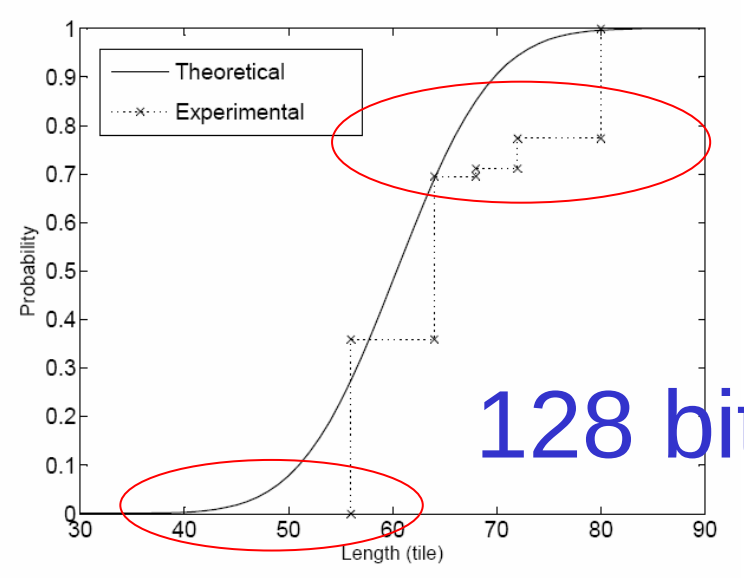


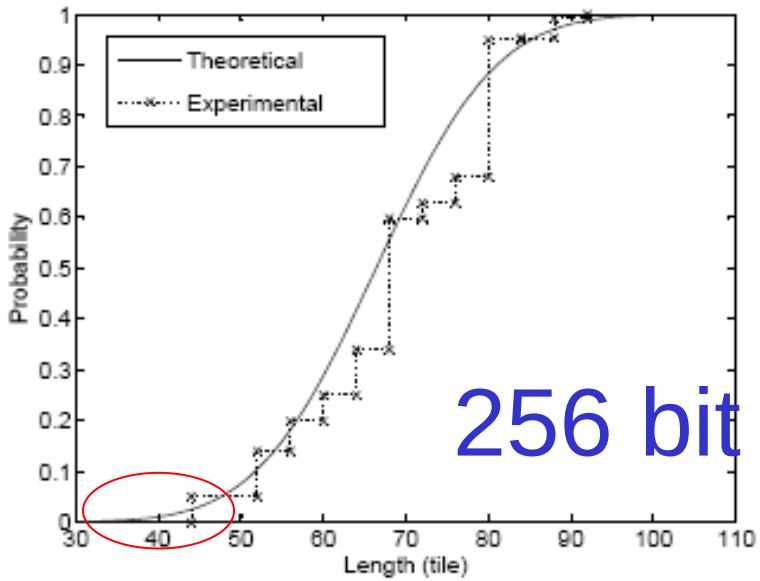
Derivation of $\overline{X}(j)$

- Interconnection length for channel *j*
  - Direct versus fringed interconnections



Comparison with Experimental Results





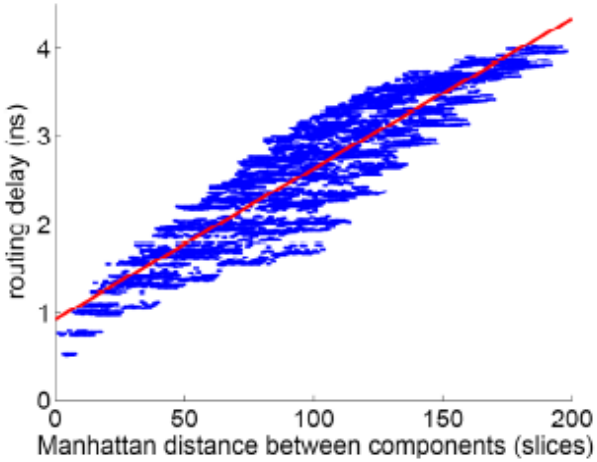
- Measuring interconnection length between two FIFO in a Xilinx Virtex-4 Design Flow
- Extract the placement and routing information in xdl format
- Assuming a Gaussian distribution
- 6.3% error for mean and 24% error for variance

Delay Prediction

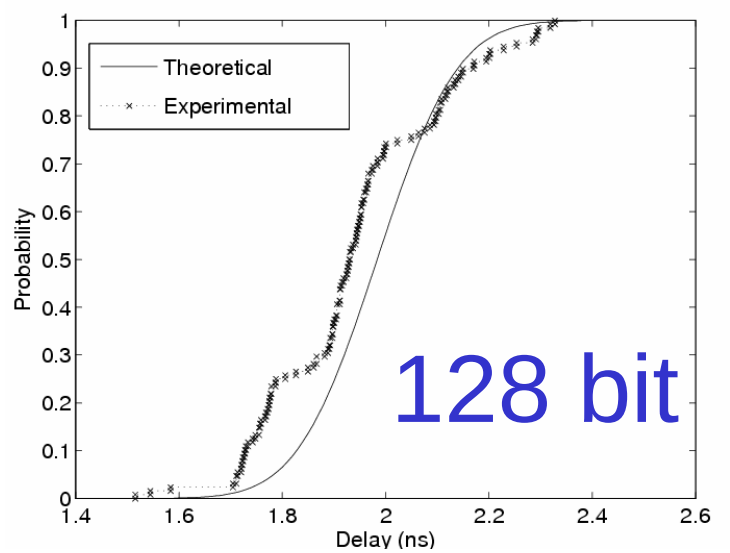
- By assuming a linear relationship between length and delay
  - Buffers along the interconnection
- By applying the length estimate

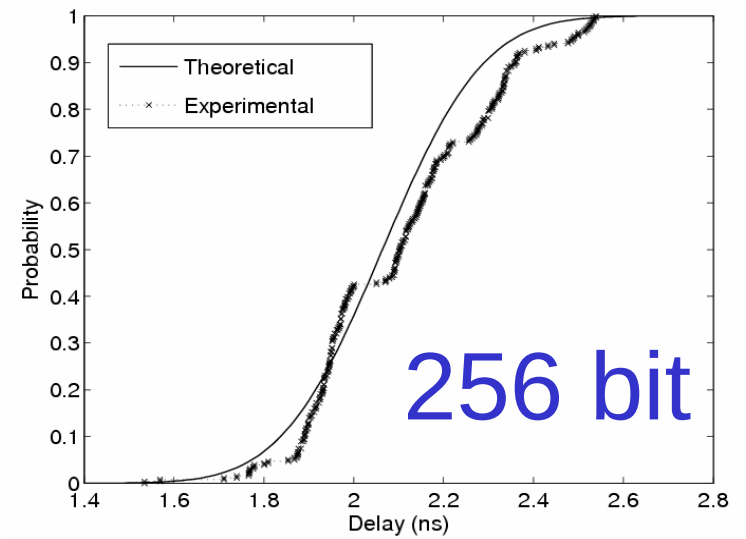
$$\mu_\Delta = \alpha E[\xi] + \beta$$
$$\sigma_\Delta = \alpha^2 \mathrm{VAR}(\xi)$$

- To be modified to introduce more accurate characterization in future

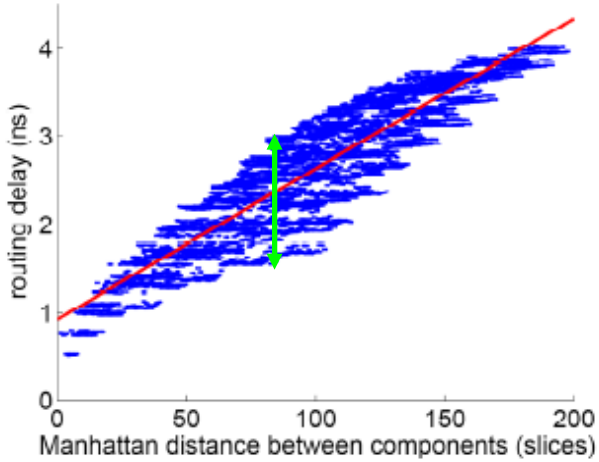


Comparison with Experimental Results





- Extract the α and β from statistics
- A wide spread of non-linear sample points



- 3.9% error for average and 21% error for variance

Conclusion

- Potential Applications
  - Provide an analytical basis for FPGA routing fabric design, especially for high bandwidth link
  - Optimize the aspect ratio and number of pins for modules
- Future Work
  - Local interconnects (within module) are not considered
  - More sophisticated delay models can be introduced