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Global Interconnections in FPGAs: Modeling and Performance Analysis

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- Background
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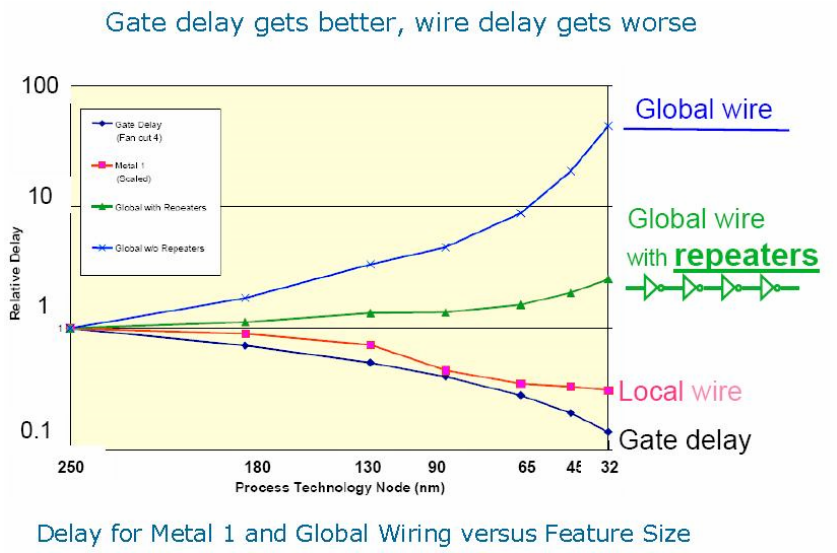
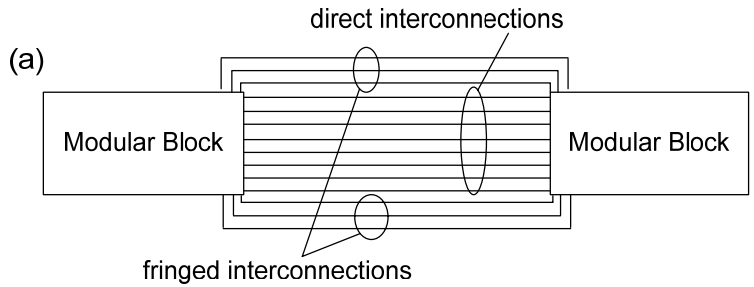
- Conclusion

Global Interconnections Problems in FPGAs

- Technology scaling
  - Long interconnection looks grim in future
  - Worse in FPGAs
- Demand for high bandwidth interconnections
  - Rent's rule predicts that
  - Network-on-Chip architecture
- Interconnect fringing





New Signaling Techniques

- Emerging techniques
  - Interconnect wave-pipelining (Dobkin *et al.*, Deodhar *et al.*, Xu *et al.*)
  - Phase-encoding (D'Alessandro and Yakovlev)
  - LVDS (Lee *et al.*)
- Can these techniques be adapted to FPGAs?
  - (Bad news) Interconnection nightmare
  - (Good news) Buffers were inserted in switching points

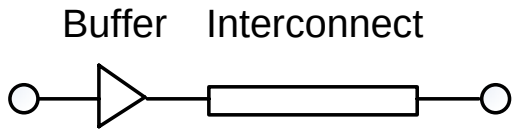
Previous Work (I)

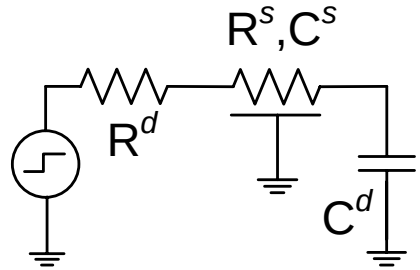
- Sakurai's Closed-Form Approximation

$$v_i = 1 - \sum_{j=1}^{\infty} k_{i,j} e^{-t_{v_i}/\sigma_{i,j}}$$

$$\sigma_i = R_i^d C_i^d + R_i^d C_i^s + R_i^s C_i^d + 0.4 R_i^s C_i^s$$

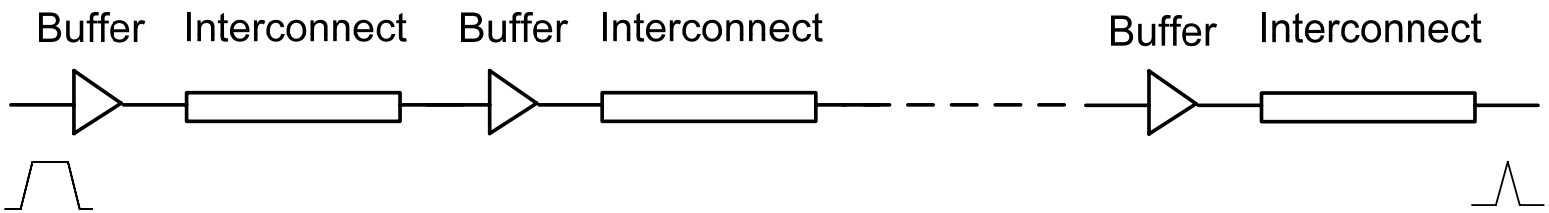
$$k_i = 1.01 \frac{R_i^d C_i^s + R_i^s C_i^d + R_i^s C_i^s}{R_i^d C_i^s + R_i^s C_i^d + \frac{\pi}{4} R_i^s C_i^s}$$





Previous Work (II)

- Deodhar and Davis's Method



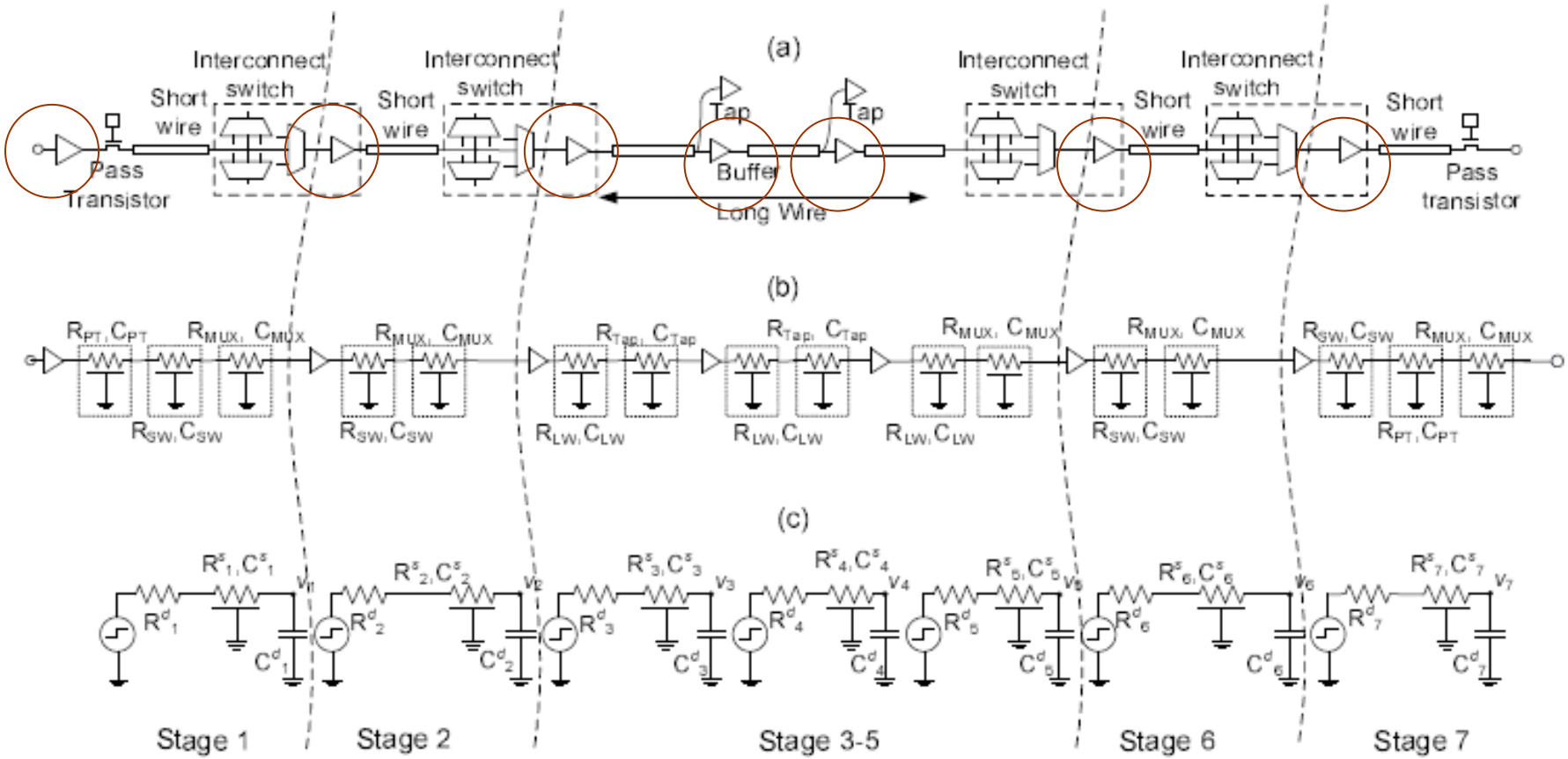
- Given the voltage (*v*) at the sink, we can compute the minimum pulse width (PW)

- Throughput = 1/PW
- Assumption
  - All interconnect segments and buffers are the same

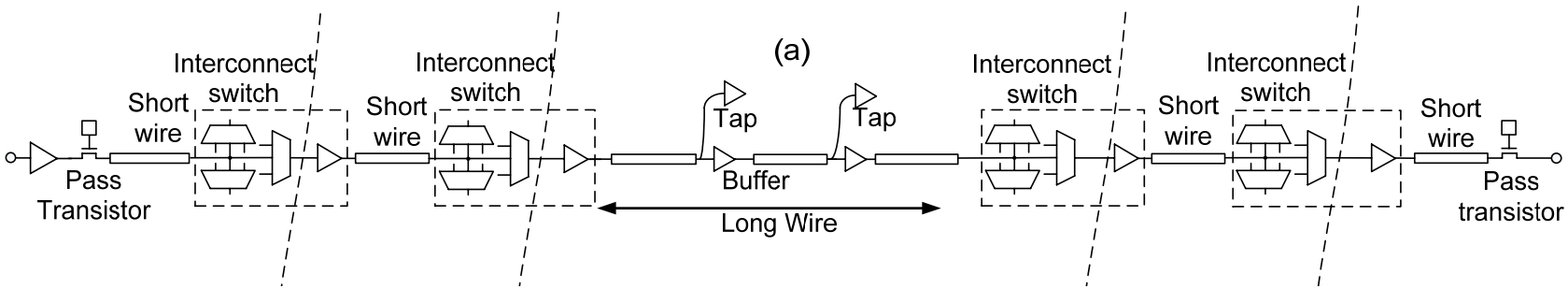
Interconnections in FPGAs

- Highly constrained routing network versus flexible wire design in ASIC
  - Interconnections constructed based on segments of wires
  - Buffered at switching points
  - Interconnections are unknown until a circuit has been downloaded
- A structure model to analyze interconnection performance in FPGAs

FPGA Global Interconnection Modeling



Delay Derivation



- Delay

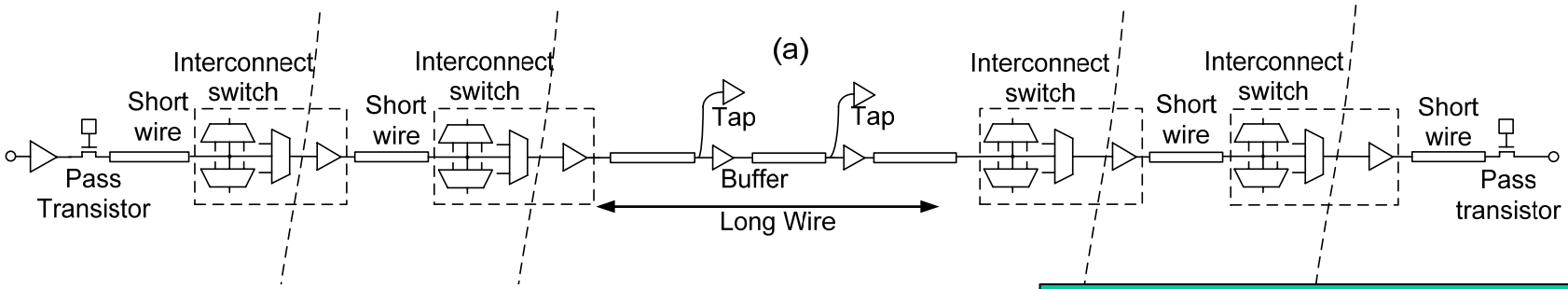
$$T_n^{\text{Delay}} = \sigma_n \ln\left(\frac{\gamma_n k_n}{\gamma_n - v_n}\right) + \sum_{i=1}^{n-1} \sigma_i \ln\left(\frac{\gamma_i k_i}{\gamma_i - 0.5}\right) + \sum_{i=1}^{n} \delta_i$$

Delay of the last segment

Total of delay of the n-1 segments

Delay of the *n* buffers

Throughput Derivation



- Throughput

$$\Gamma_n^{\text{Wave}} = \frac{1}{\sigma_1 \ln\left(\frac{\gamma_1 k_1}{\gamma_1 - v_1}\right) + \delta_1}$$

1. Independent of buffer delay
2. Depends on topological configuration of interconnects
3. Depends on the number of buffers

$$v_{i-1} = \frac{\gamma_{i-1}}{\gamma_{i-1} k_{i-1} (2\gamma_{i-1} - 1) \left(\frac{\gamma_i - v_i}{\gamma_i k_i}\right)^{\frac{\sigma_i}{\sigma_{i-1}}} + 1}$$

A Note About Throughput

- Throughput is function of v_1, which can only be computed backward from v_n

- If all interconnect segments are the same

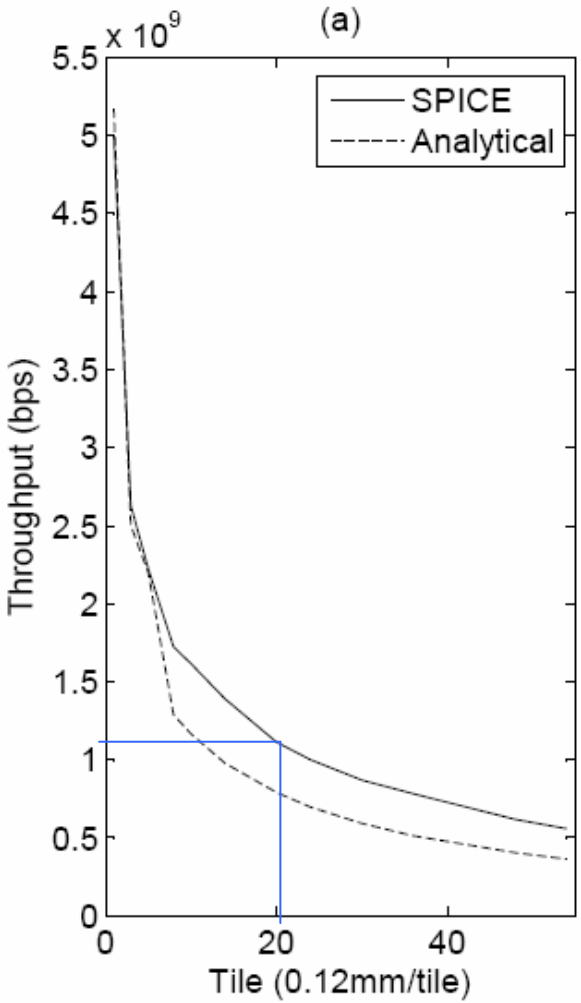
$$v_{n-1} = \frac{1}{2 - v_n}$$

- A more general expression is

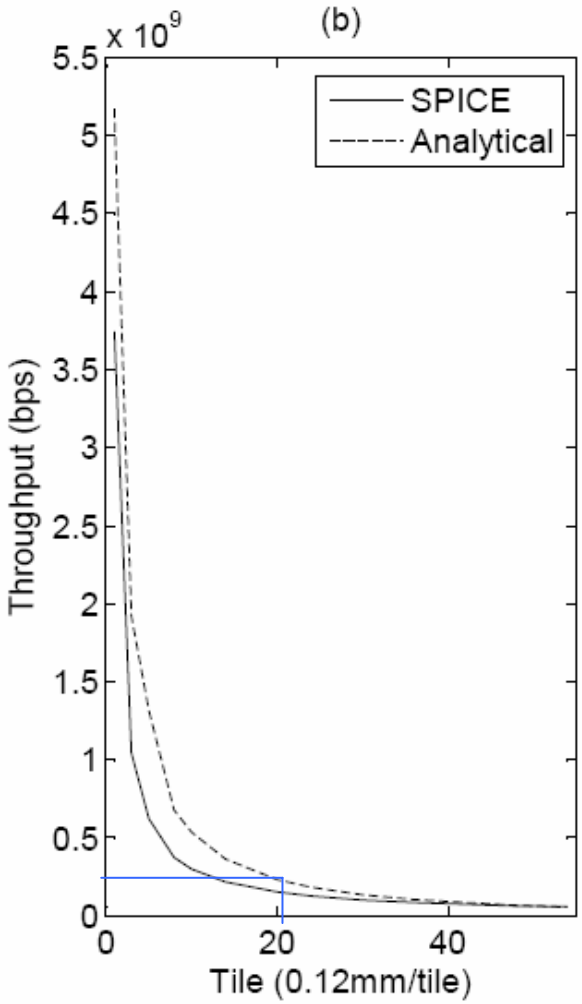
$$v_{i-1} = \frac{\gamma_{i-1}}{\gamma_{i-1} k_{i-1} (2\gamma_{i-1} - 1) \left(\frac{\gamma_i - v_i}{\gamma_i k_i} \right)^{\frac{\sigma_i}{\sigma_{i-1}}} + 1}$$

1. Larger parameter space to explore the interconnect throughput
2. Can be used for FPGA interconnection

Max Throughput versus Min Delay



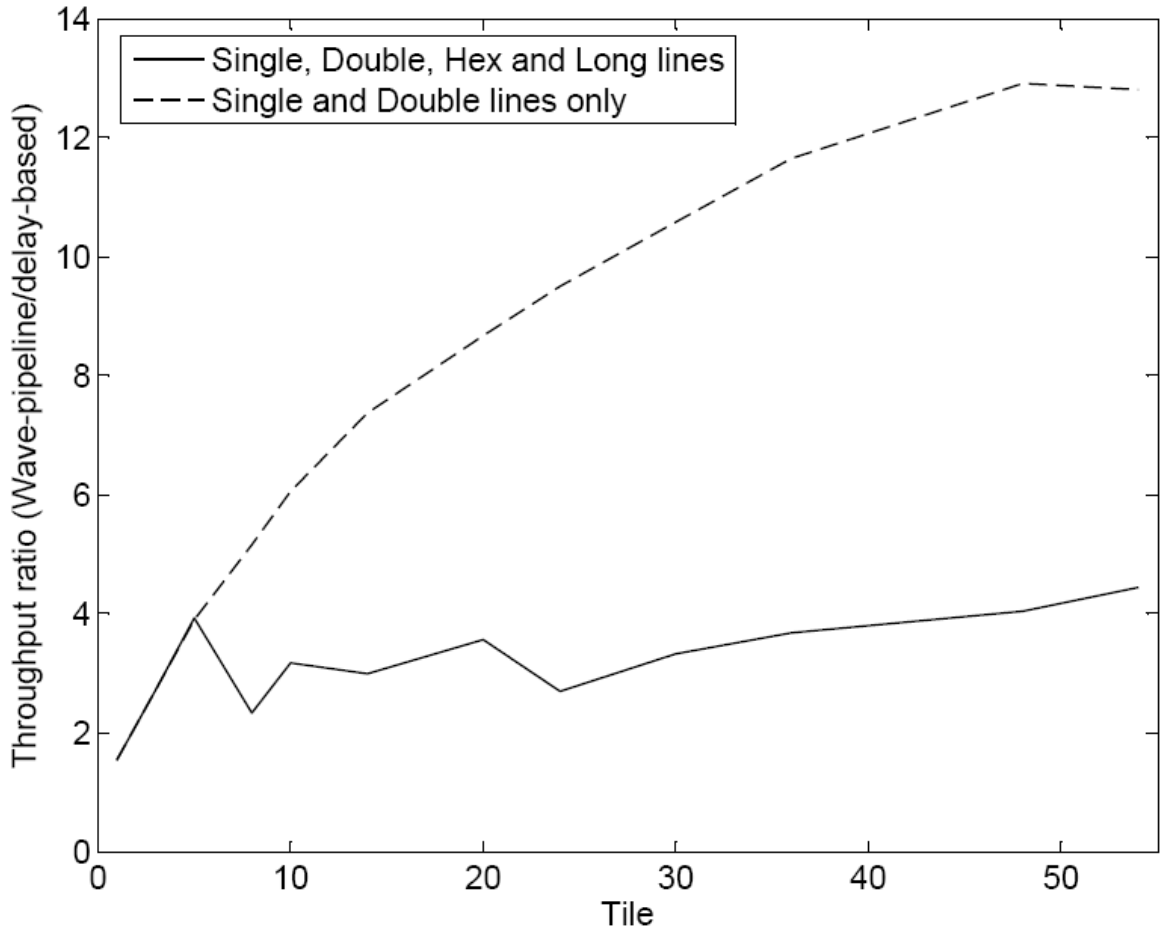
Wave-pipeline Based



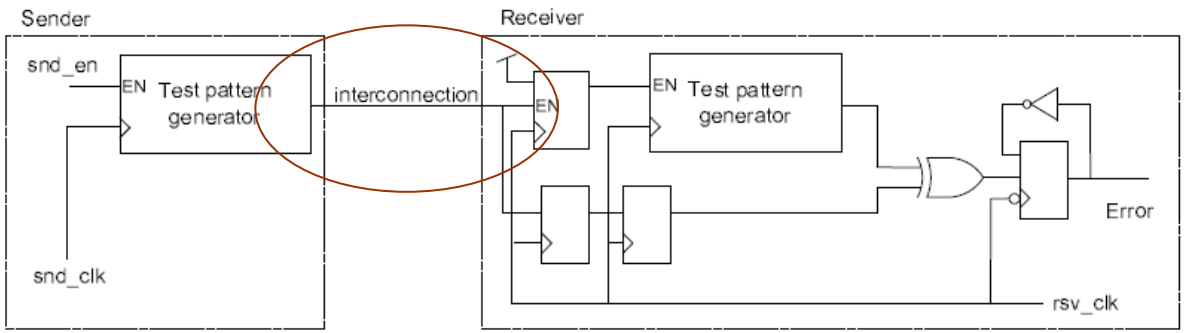
Delay Based

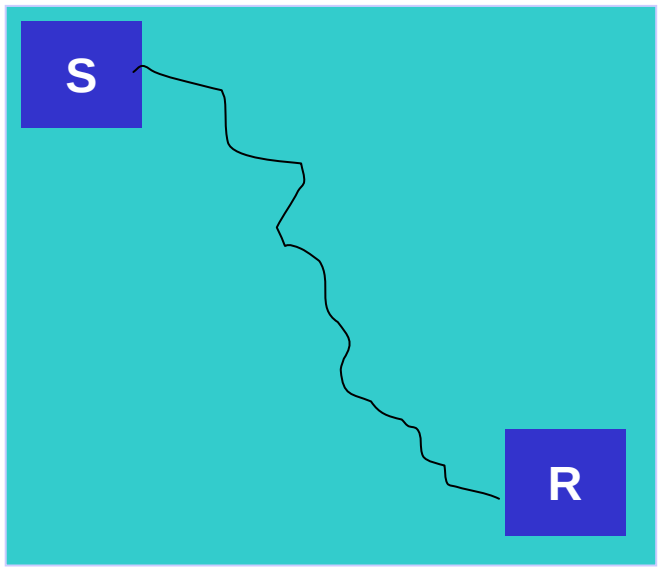
- SPICE simulation based on 90nm PTM model
- Cadence Spectra and Analog Environment
- Up to 4 types of interconnects (Single, Double, Hex, 24-long)

Throughput Ratio



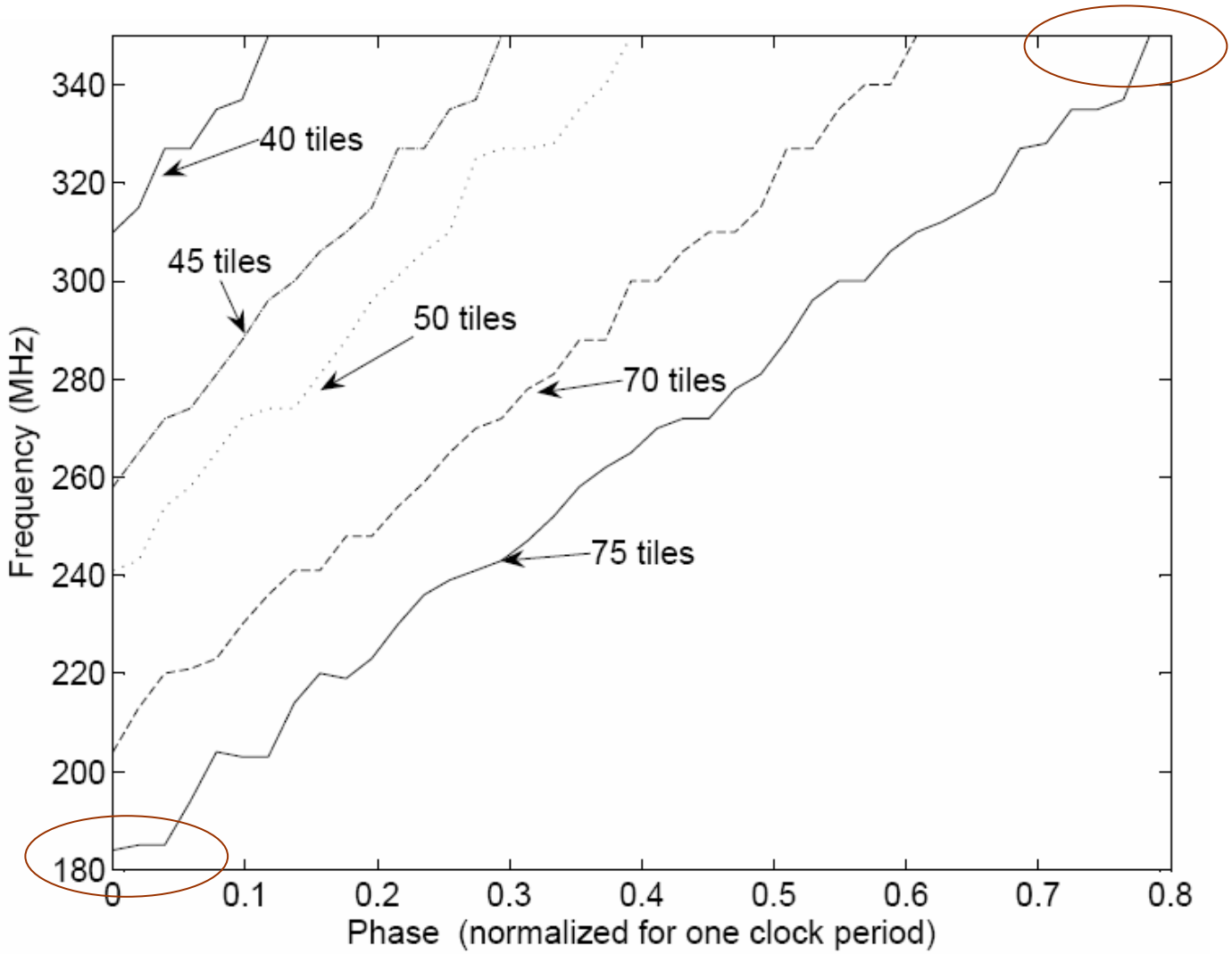
FPGA Virtex-5 Experiments





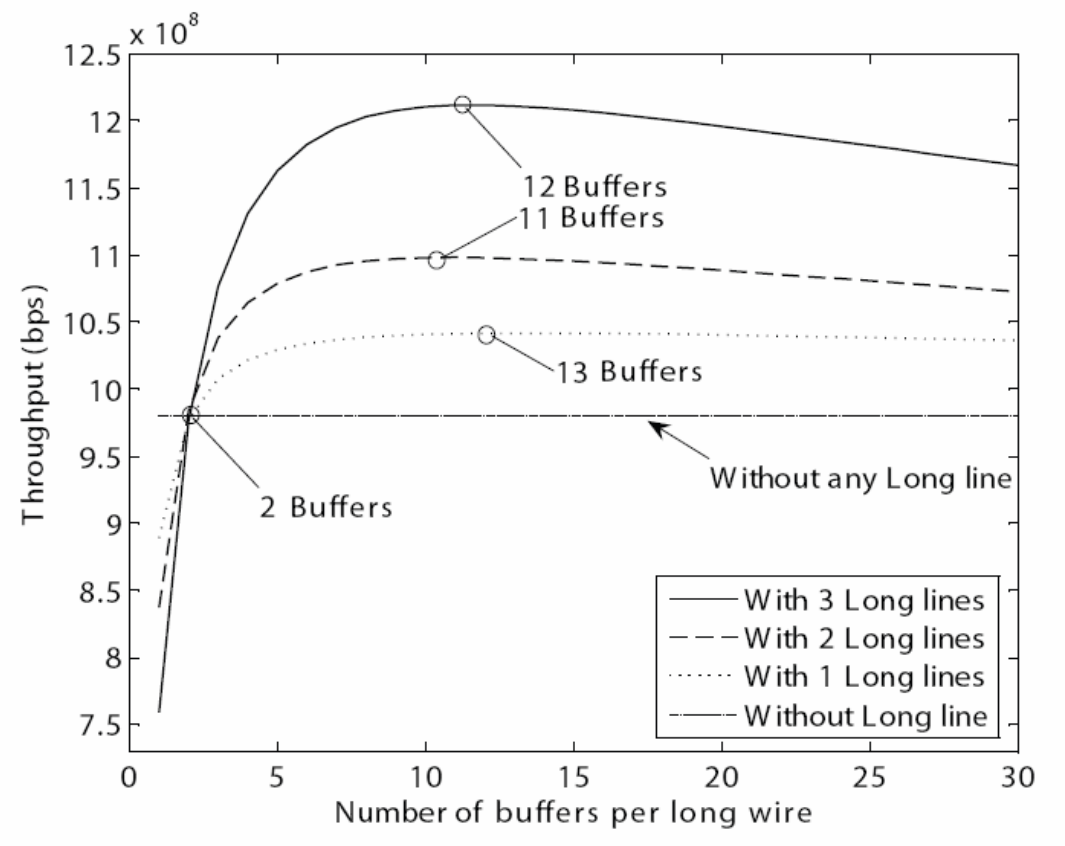
- Built-In-Self-Test system (Wong *et al.* FPT'07)
- Run-time reconfigurable frequency and phase sweep
- Microblaze processor for control, measurement and interfacing
- Xilinx 65nm Virtex-5 device

Result (Frequency-phase profile)



FPGA Architecture Modification

- Adding more buffers to the long wires



Conclusion

- A FPGA global interconnection model
- Studied the delay and throughput
- Experiments on a Virtex-5 FPGA
- Implications
  - Interconnect wave-pipelining can be realized in FPGA for higher throughput
  - On-FPGA serialization
  - FPGA architecture modification for interconnect wave-pipelining