MDGRAPE-4 NoC Links

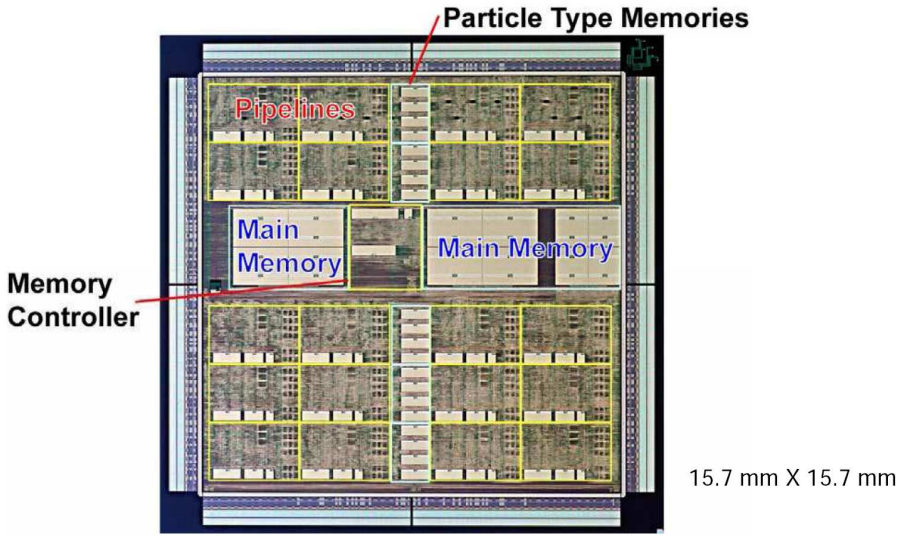
Circuit and Physical Design

Duraid Madina, Makoto Taiji

SLIP 2008

MDGRAPE-3

MDGRAPE-3 is an efficient chip that accelerates n-body simulations:



Vital stats:

- 130nm, 1.2V, 7Cu, 250mm^2
- 230GFLOPS @ 19W, 350MHz (250MHz worst-case)
- 20 force calculation pipelines (˜single precision): ˜660 flops/cycle

MDGRAPE-3

Put 12 chips on a board:

(˜2.7TFLOPs, ˜250W)

MDGRAPE-3

Put 400 boards in a room, sprinkle Xeon boxes:

(~1PFLOPs, ~200kW, 22 racks - that's all of them)

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- However...
  - Single purpose (more or less)

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- A broader range of scientific tasks
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- A broader range of scientific tasks
  - A heterogenous, tiled processor
  - Lightweight processor cores and special-purpose units
- A more efficient design
  - Moving from limited use of custom cells to more widespread custom blocks
  - Low power design used wherever possible to enable high system performance through scalability

MDGRAPE-4 Early Design

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  - Upper local layers freed for intra-tile and neighbouring-tile full-swing buses.

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- Picked most promising layouts (minimum maximum length, turn and via counts etc) to investigate further

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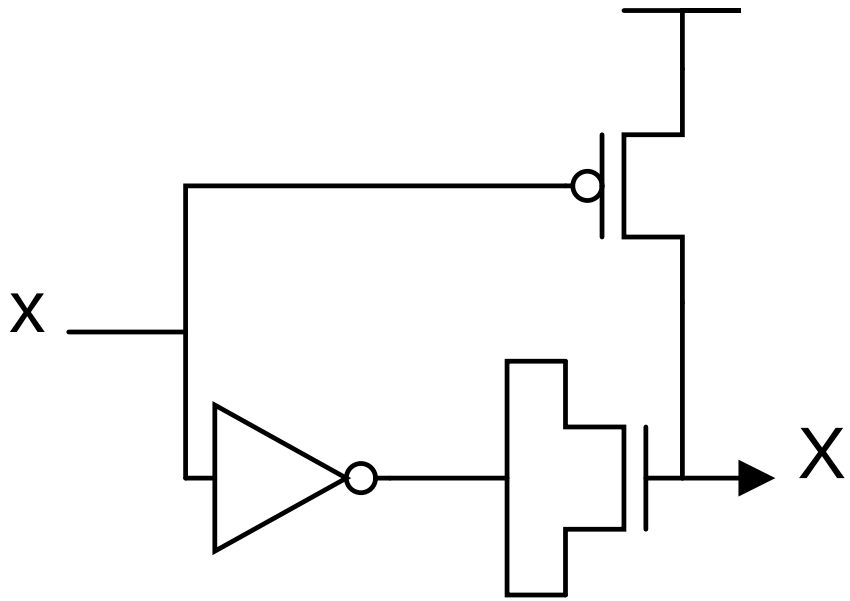
- Settled on capacitively signalled LVS diff pairs (following Mensink et al.)

Early MDGRAPE-4 Links

- Basic idea: use capacitive transmitter to save power and boost effective bandwidth



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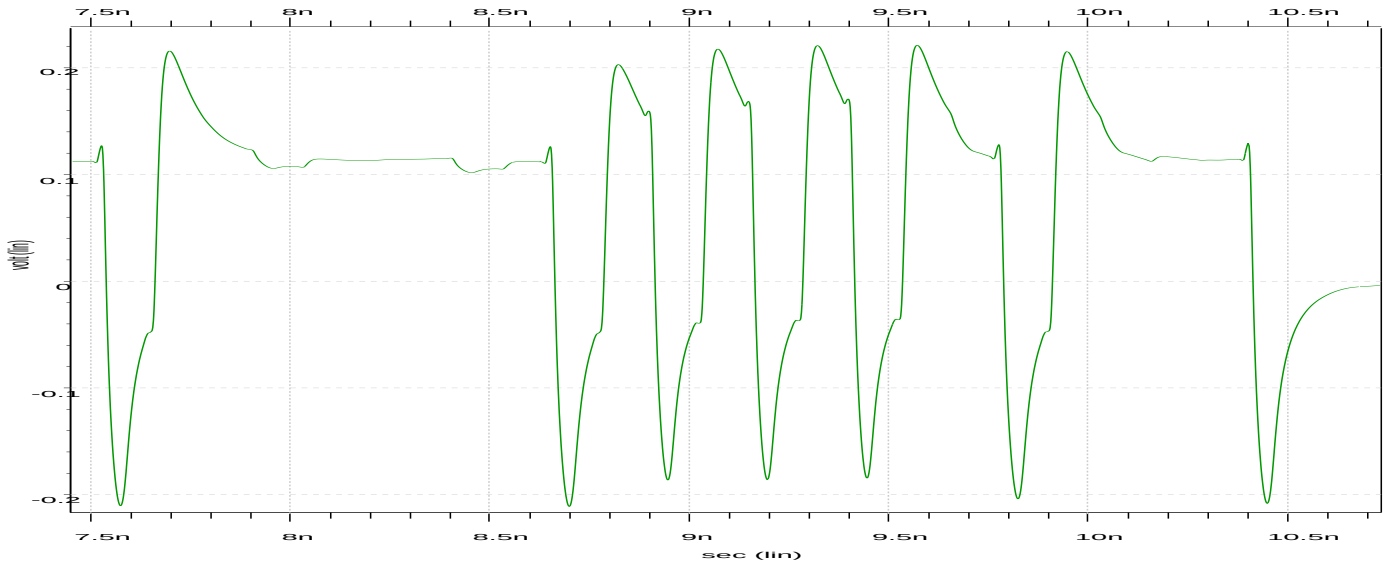

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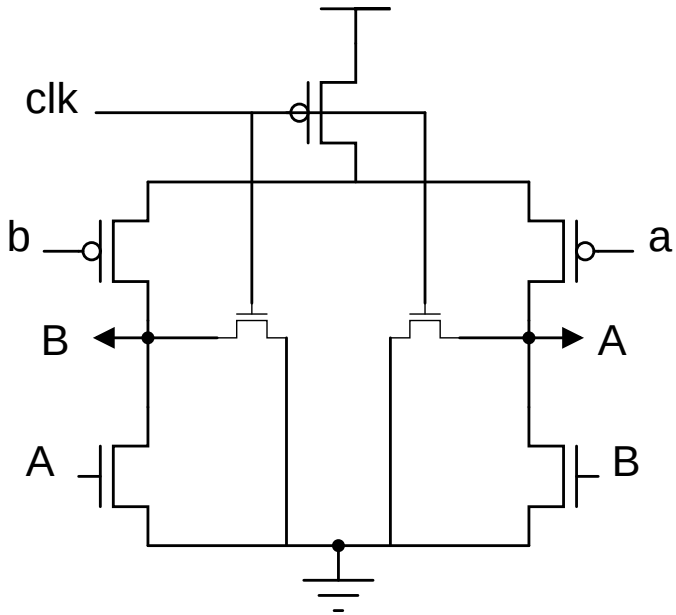

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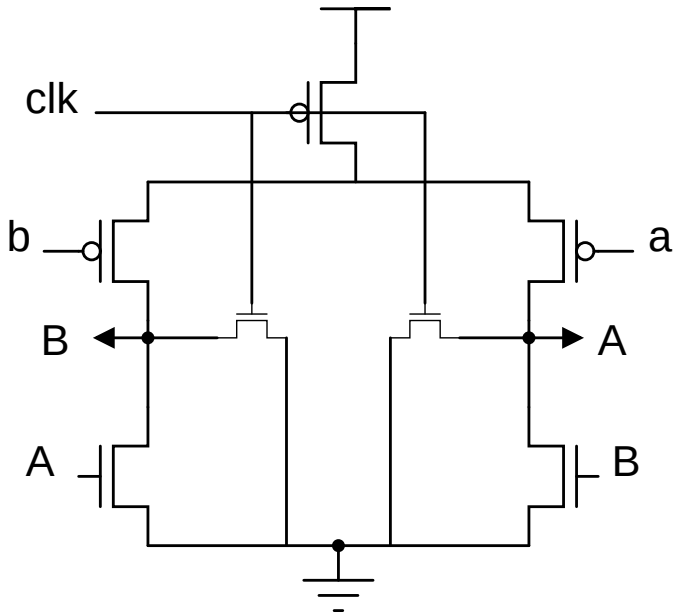

- "Problem": 4.5mm link performance/power rolled off at ~5GHz

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  - Active, passive RX-side equalization
- All these cost significant power and/or area

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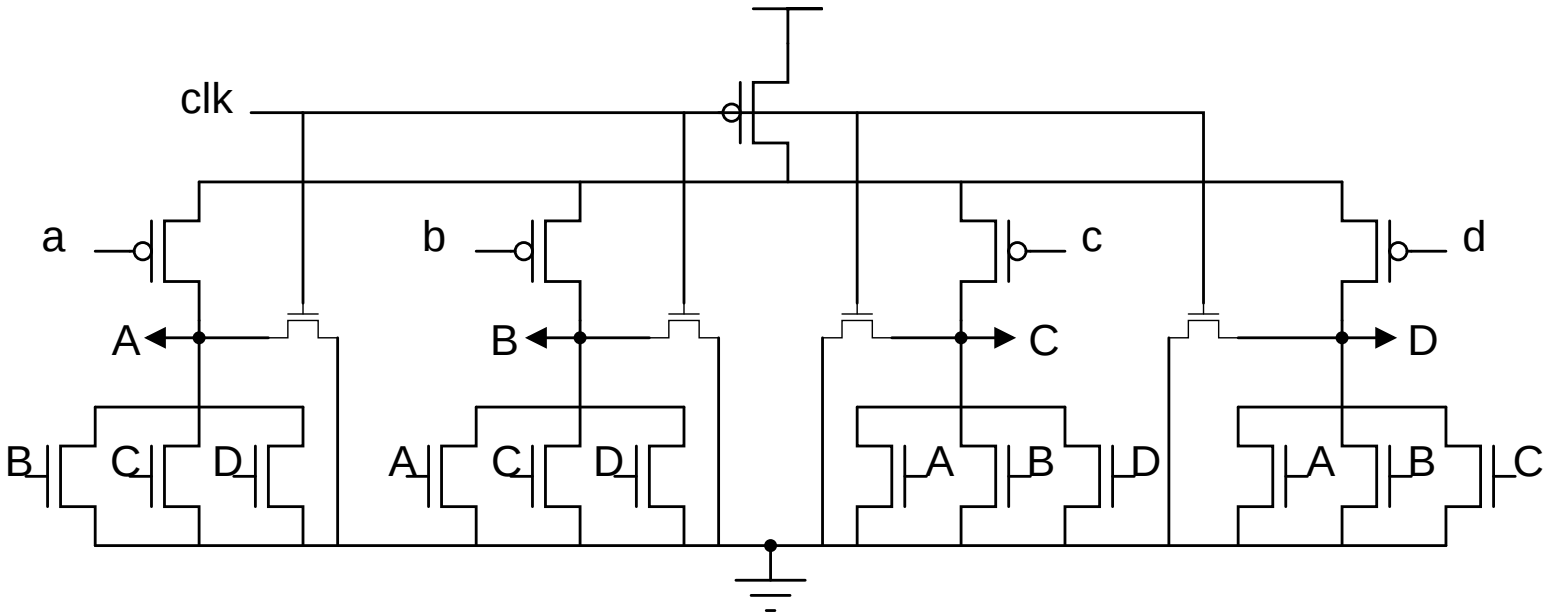
- It turns out that you can build a sense-amp to sense quadrature signals. With a bit of care, the following circuit works reliably:



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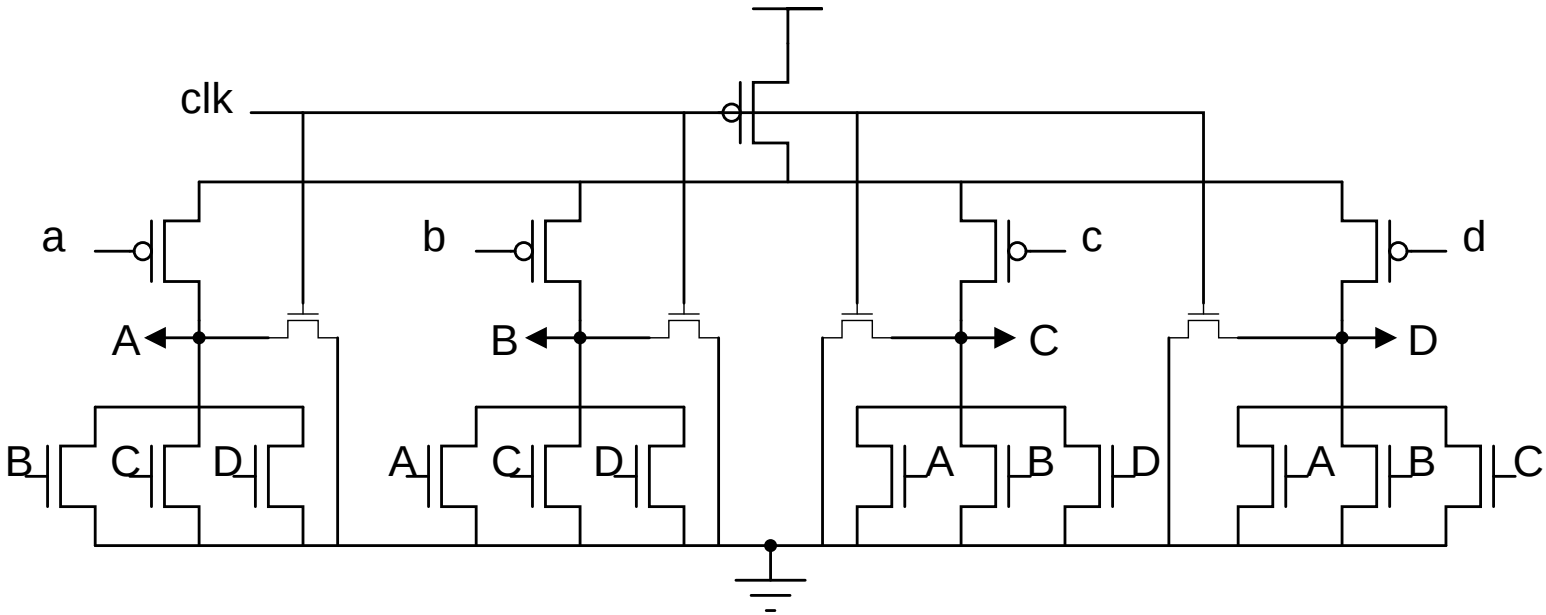

- Just need to watch out for pitfalls

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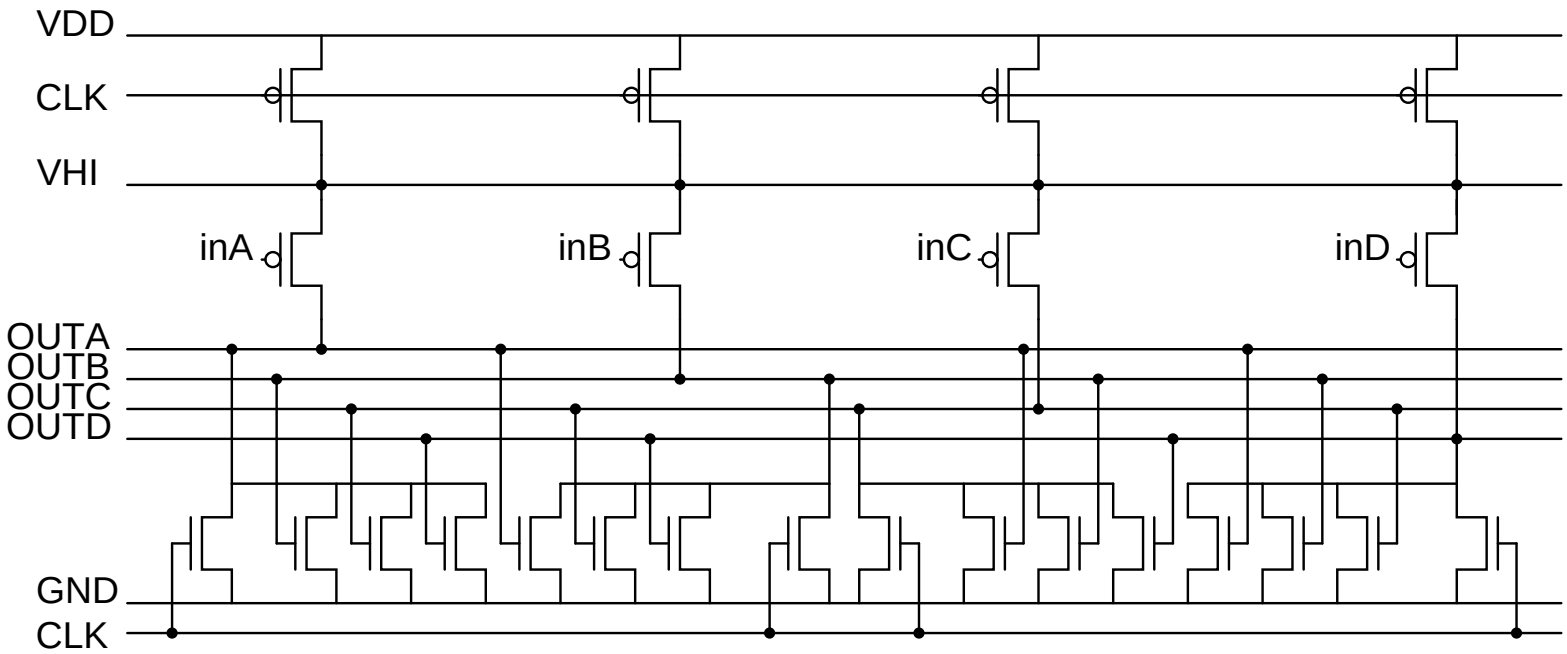
- Layout critical on both ends

Pitfall: Layout

- QSA layout is more or less as in this schematic:



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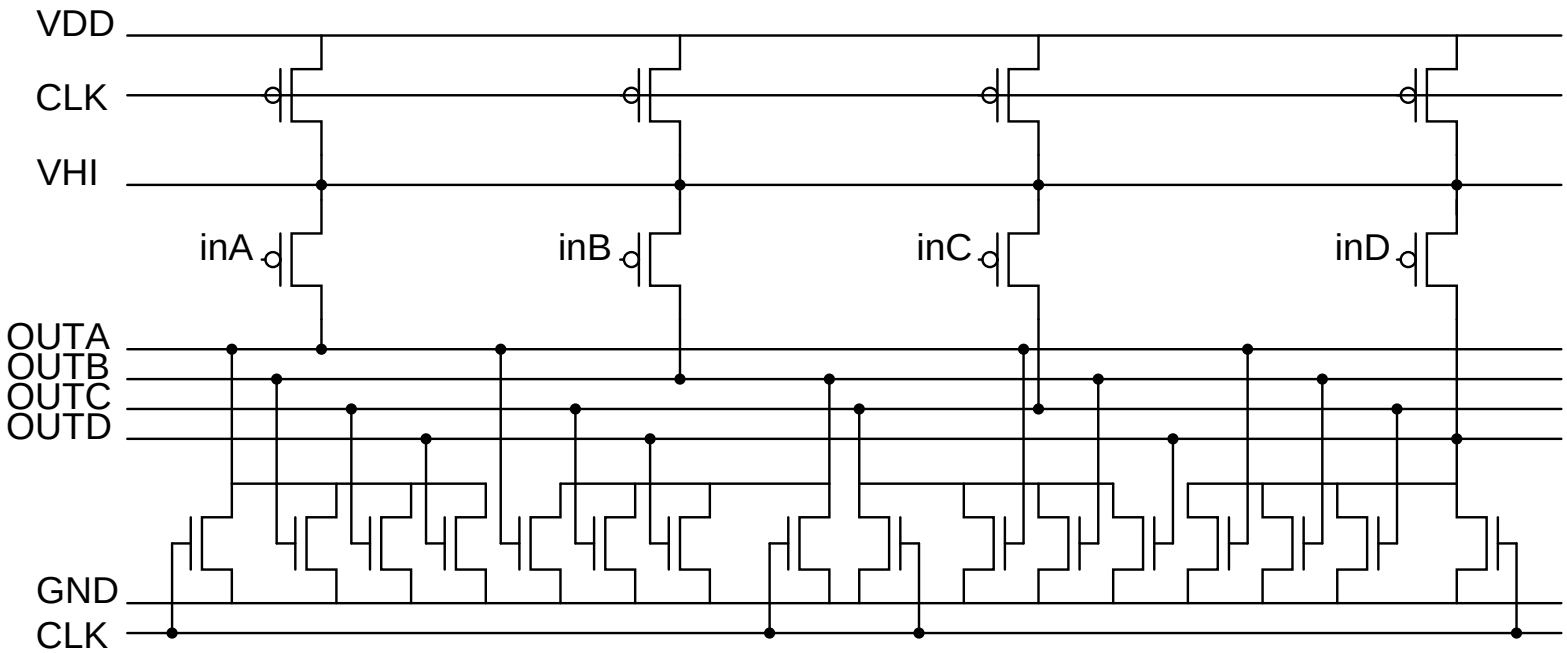

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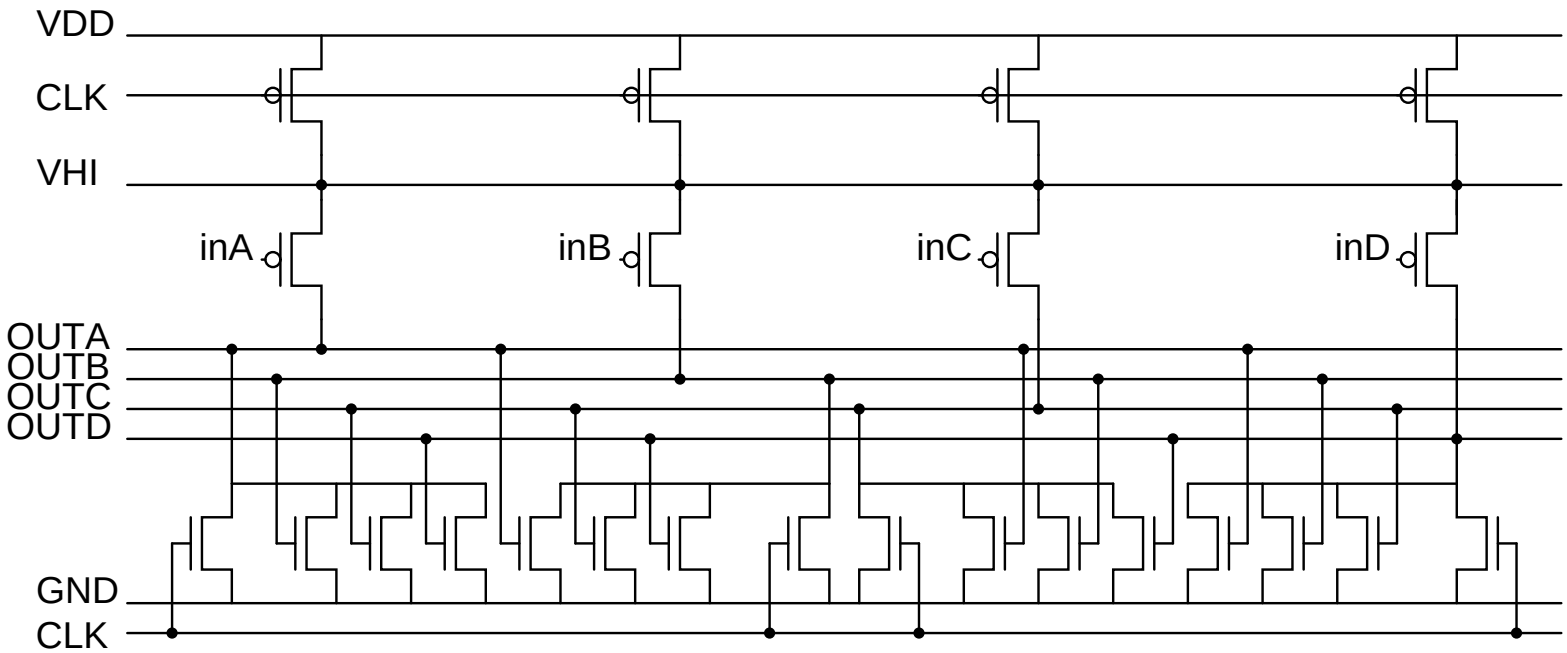

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- Each has pros and cons...

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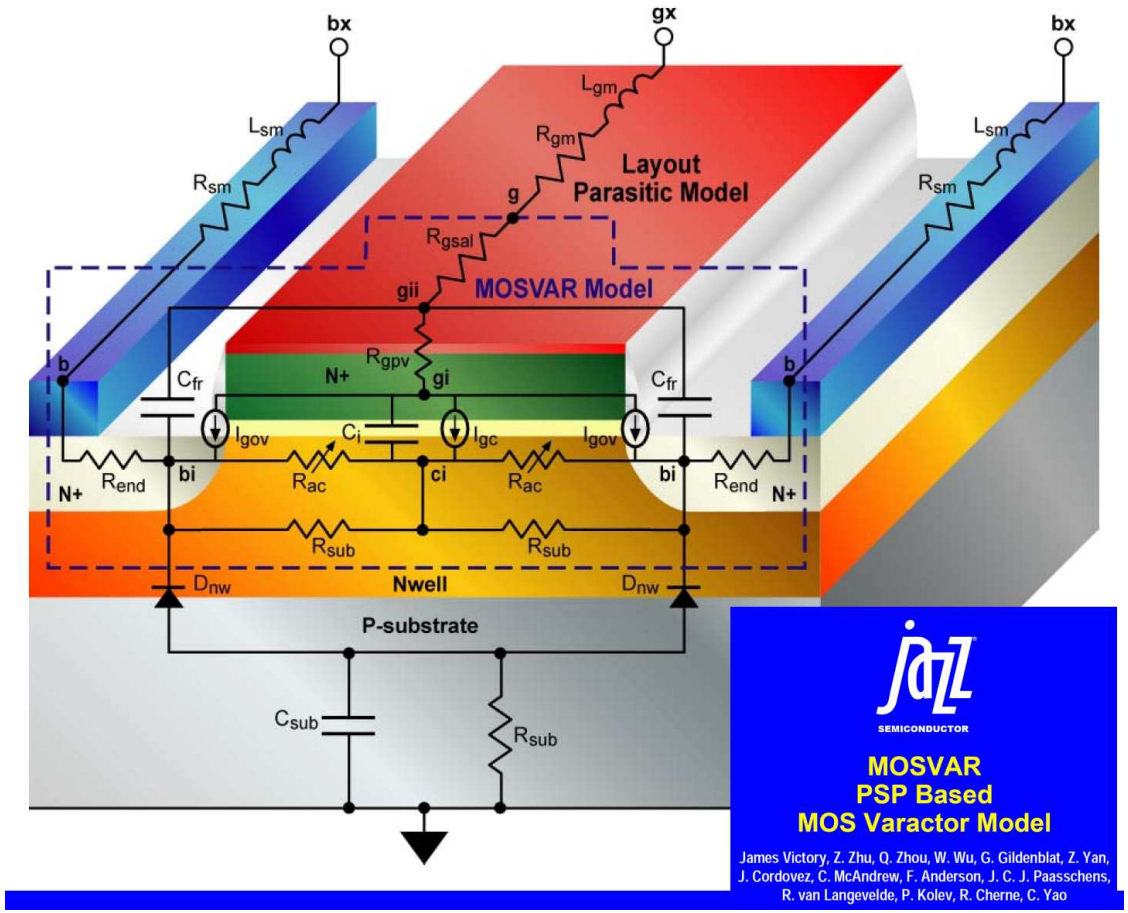
- Signalling around vdd gets higher capacitance and lower variation from the TX varactors:



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- In our situation, this turned out to be the more important effect.

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- Thermal and cross-wafer/lot-to-lot variation handled through per-bus clock verniers

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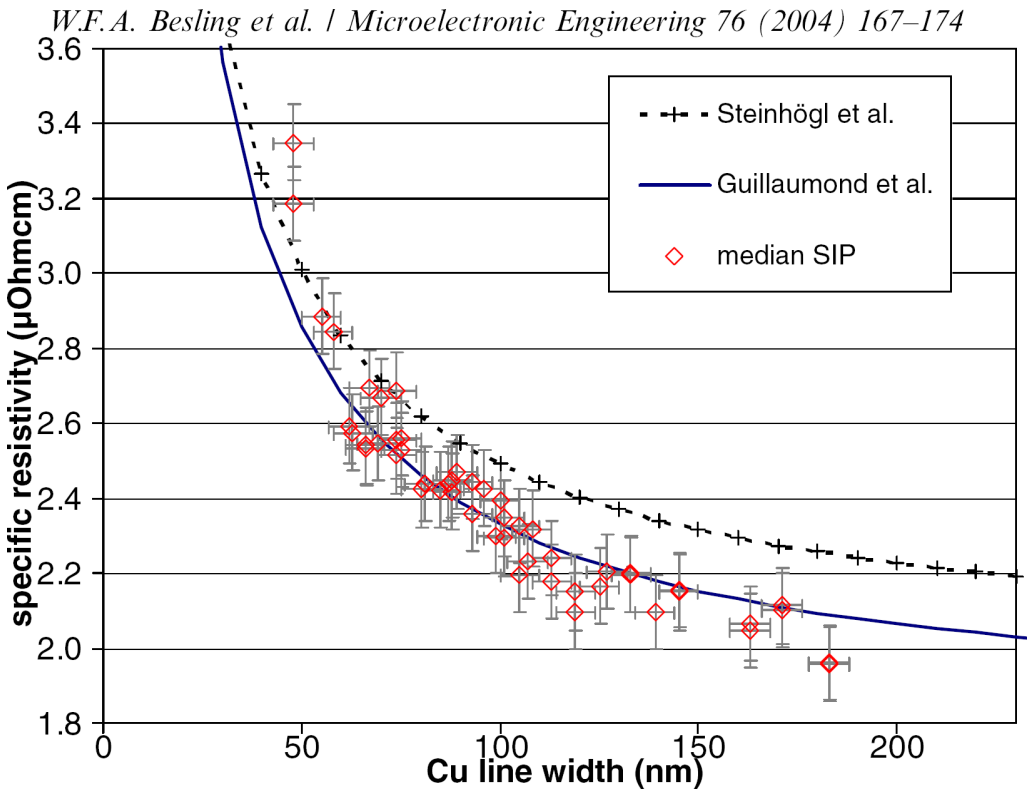
- Often true today, but problems with wire scaling motivate fatter serial links:



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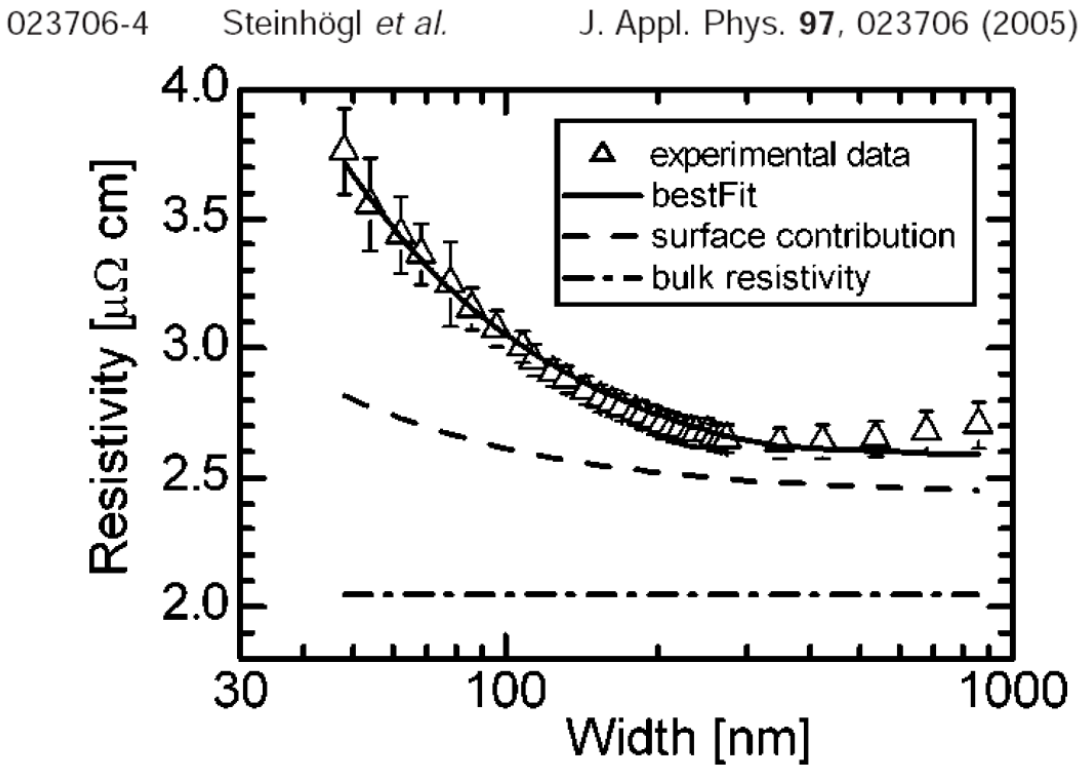

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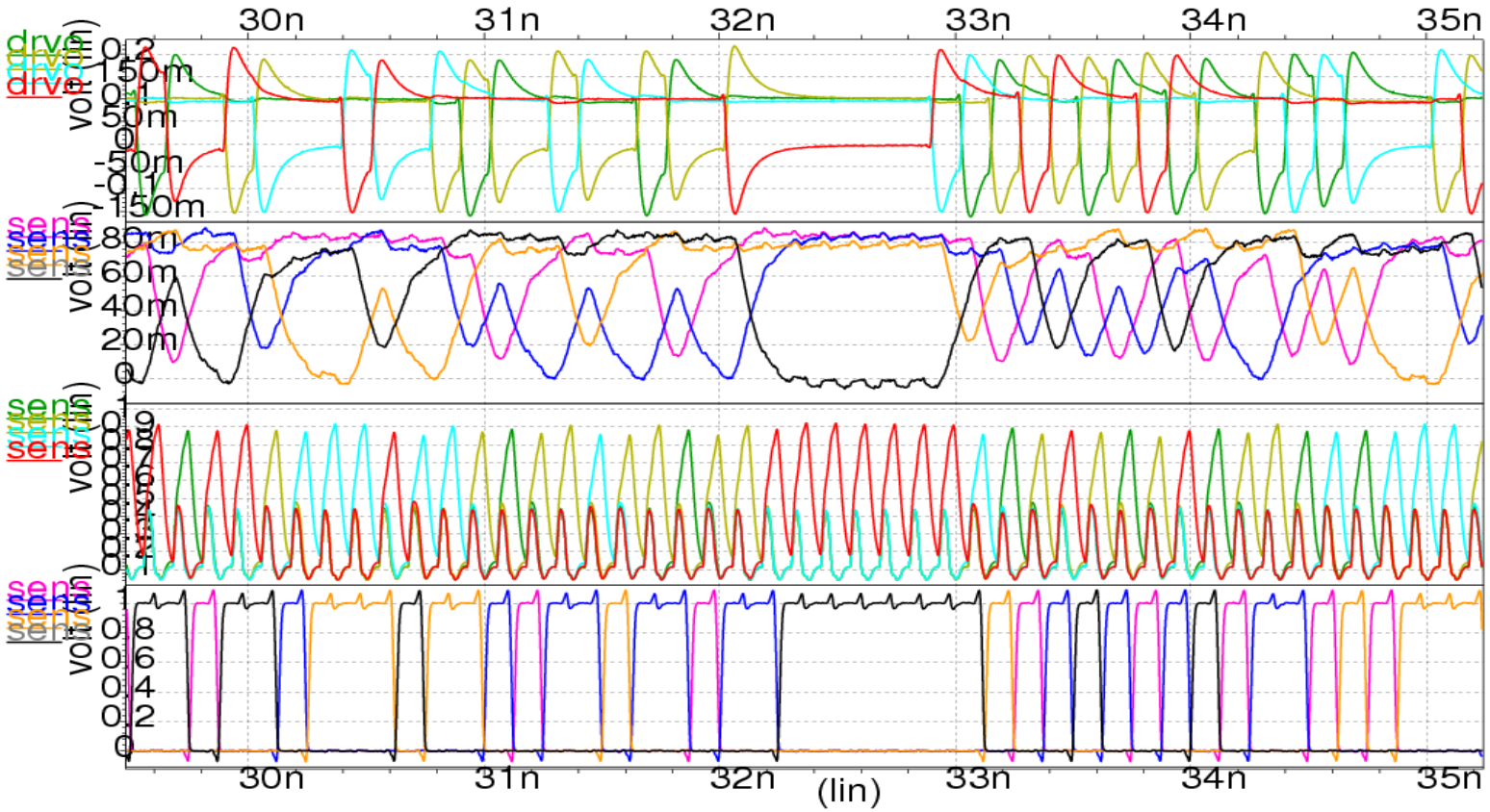
- Essential to insert spare bus lines
  - QSAs small and reliable enough (temporally speaking) that adding spares is more effective than adding sophisticated ECC from a power/performance standpoint

Result

- Result: Quadrature TX/RX enables successful 8GHz operation across 4.5mm links
  - With low area.. (TX essentially unchanged, RX reduced due to elimination of EQ)
  - ..and low power (61fJ/bit typical at 8GHz in 1.0V 65nm)



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- A number of well-known equalizer designs plug directly into a QSA: where yield and/or area are much less important than absolute speed, these deliver significant gains, sometimes at modest power costs

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- This works fine, but we can potentially improve router and extraction runtimes if placement/symmetry information can be communicated to these tools

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- NoC design exploration used periodic wire router to quickly prototype various designs
- One-hot quadrature links save power, reduce area and improve link speed compared to standard differential designs

Acknowledgements

- We'd like to thank Fujitsu Microelectronics, Berkeley Design Automation and Magma Design Automation for their support
- Thanks to Miki Tanaka (AIST) for work on the periodic router
- Thanks also to James Victory (Jazz Semiconductor) for MOSVAR model insights
- We're grateful for funding from Japan's JSPS and RIKEN

Thanks for listening!

Thanks for listening - any questions?

- More bits and pieces online: `http://mdgrape.gsc.riken.jp`