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Process-Induced Skew Variation for Scaled 2-D and 3-D ICs

Hu Xu, Vasilis F. Pavlidis, and Giovanni De Micheli
LSI-EPFL

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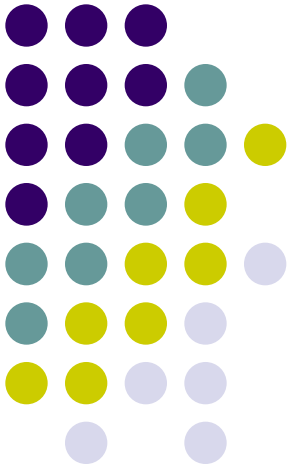
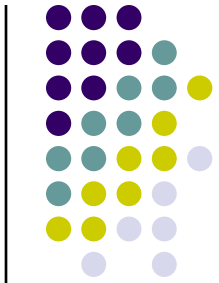
SLIP 2010, Anaheim, USA



Presentation Outline



- 2-D and 3-D Clock Distribution Networks
- Effect of Process Variations on Clock Skew
- Modeling Process-Induced Skew in 2-D and 3-D Clock Trees
- Comparison between Scaled 2-D and 3-D H-trees
- Conclusions

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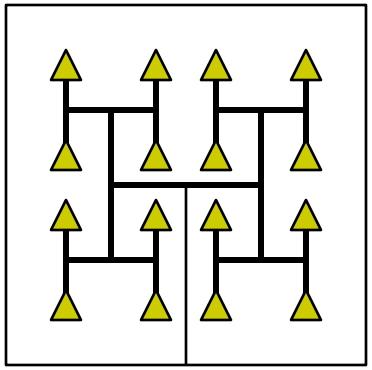
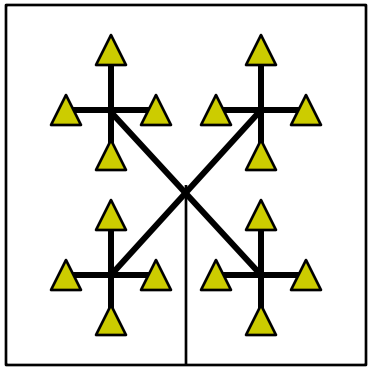
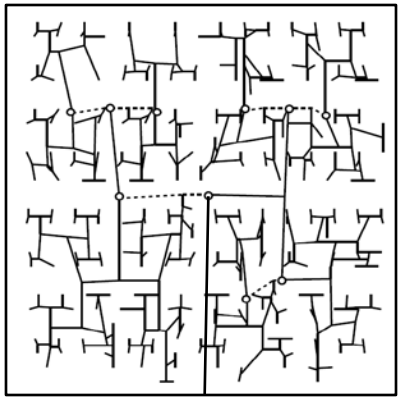
2-D Clock Distribution Networks (CDNs)

- **2-D clock tree**

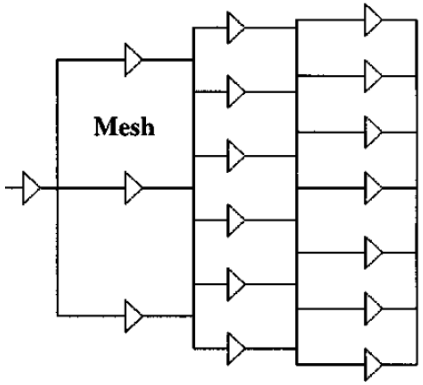




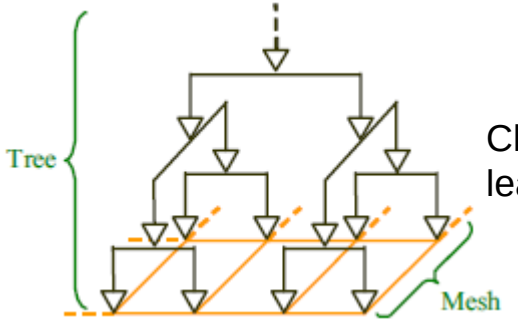


Elmore-Planar-DME [1]

- **2-D clock mesh**



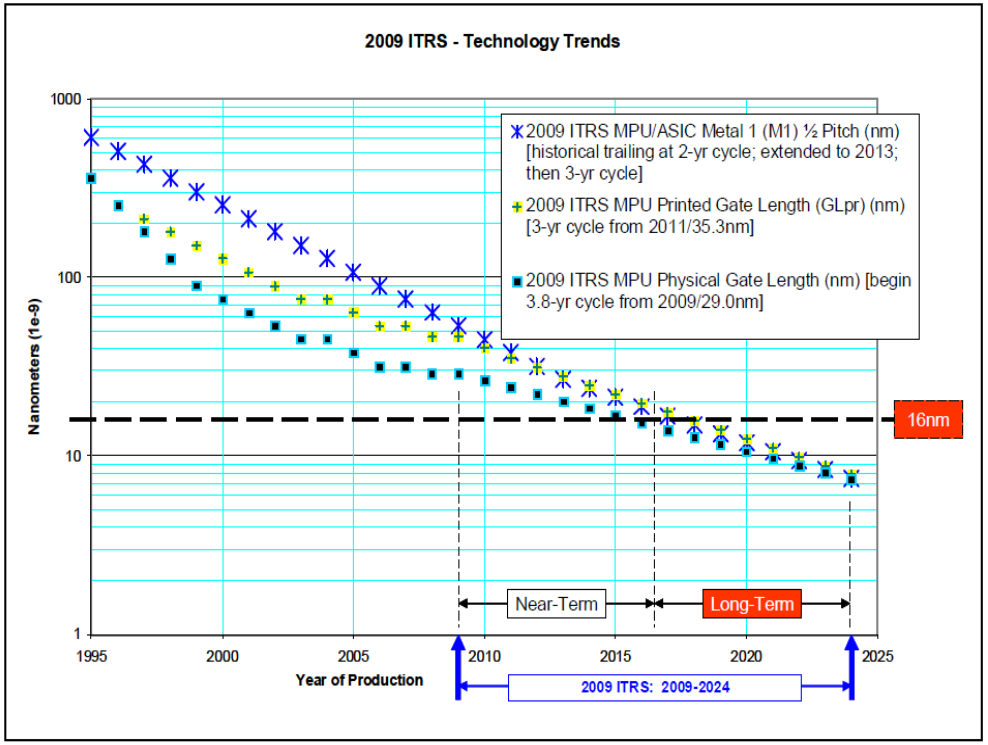
Clock mesh [2]



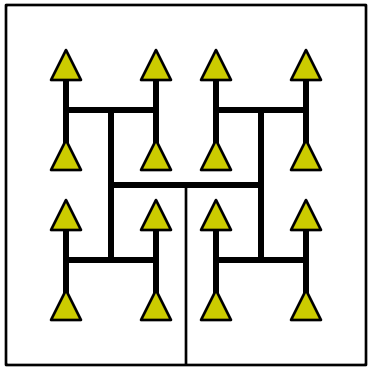
Clock mesh as the leaves of a tree [3]

[1] A. B. Kahng *et. al.,* "Planar-DME : A Single-Layer Zero-Skew Clock Tree Router," *IEEE Trans. on CAD,* 15(1), 1996.
[2] E. Friedman, "Clock Distribution Networks in Synchronous Digital Integrated Circuits," *Proc. of the IEEE*, 89(5), 2001.
[3] S. Abe *et al.*, "Clock Skew Evaluation Considering Manufacturing Variability in Mesh-Style Clock Distribution," *Proc. of ISQED*, 2008.

2-D CDNs with Technology Scaling



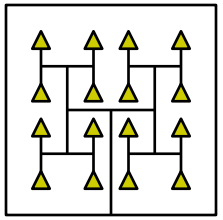
2009 ITRS—MPU/ASIC Half Pitch and Gate Length Trends [1]



90 nm

- Area decreases
- Delay of buffer decreases

- Leakage power increases
- *R* of wire increases
- Variability/mean increases

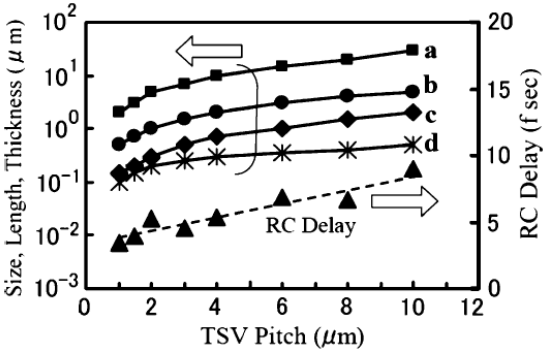


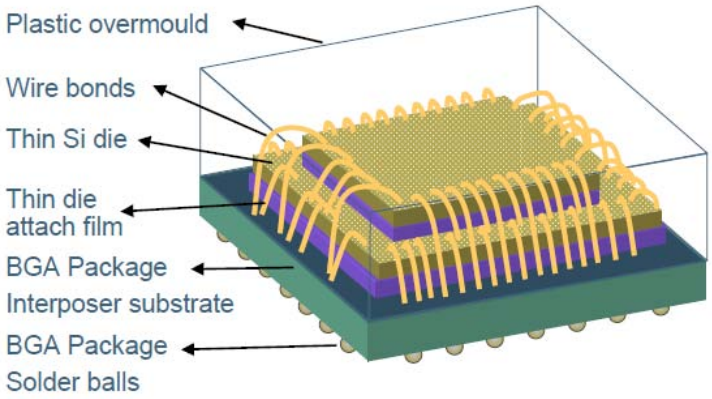
22 nm

[1] “International Technology Roadmap for Semiconductors," 2009. [Online]. Available: http://www.itrs.net.

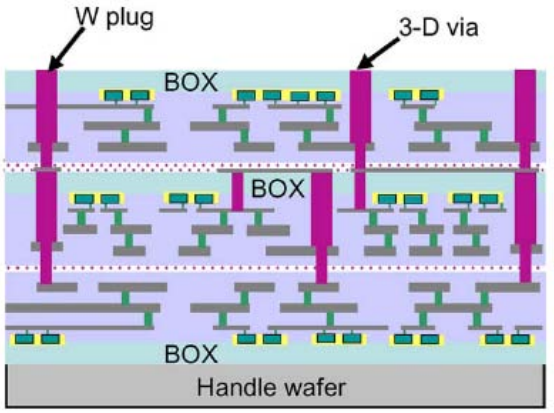
Integration Approaches for 3-D ICs

- Wire-bond packaging
- Wafer/die-bond integration
  - Through Silicon Via (TSV)





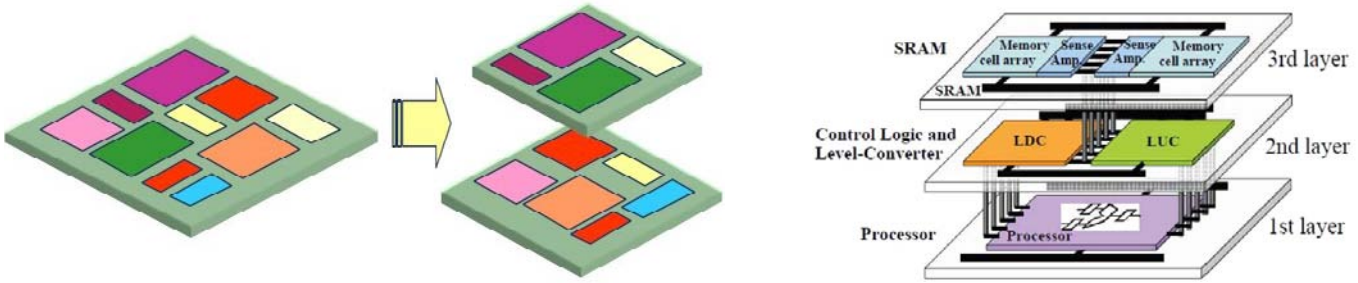
(a) Wire-bond packaging [1]



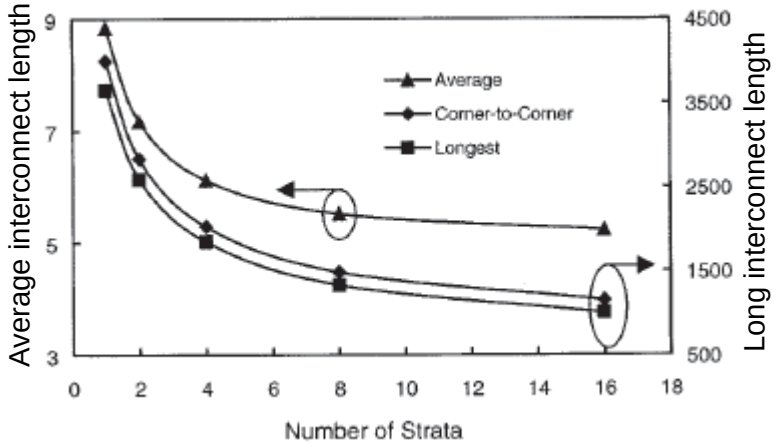
(b) Wafer/die bonding and TSVs [2, 3]

[1] E. Beyne, "3D Interconnection and Packaging," *Electronics System Integration Technology Conference*, 2006.
[2] M. Koyanagi *et. al.*, "High-Density Through Silicon Vias for 3-D LSIs," *Proceedings of the IEEE*, 97(1), 2009.
[3] *MITLL Low-Power FDSOI CMOS Process Design Guide*, MIT Lincoln Laboratory, Lexington, MA, 2006.

3-D Integrated Circuits



3-D ICs – vertically stacked devices and/or circuit blocks in one circuit. [1, 2]

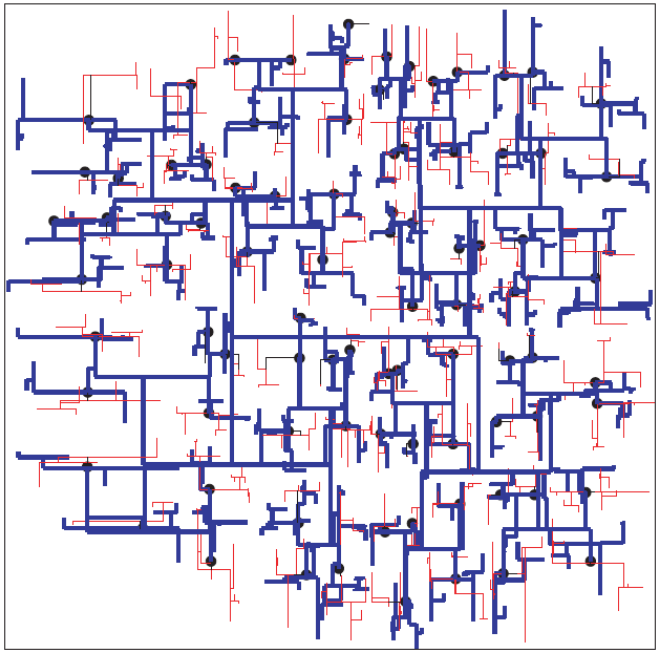


Interconnect length vs. number of planes. [3]

[1] E. Beyne, "3D Interconnection and Packaging," *Electronics System Integration Technology Conference*, 2006.
[2] M. Koyanagi *et al.*, "High-Density Through Silicon Vias for 3-D LSIs," *Proc. of the IEEE*, 97(1), 2009.
[3] J.W. Joyner *et al.*, "Impact of Three-Dimensional Architectures on Interconnects in Gigascale Integration," *TVLSI*, 9(6), 2001.

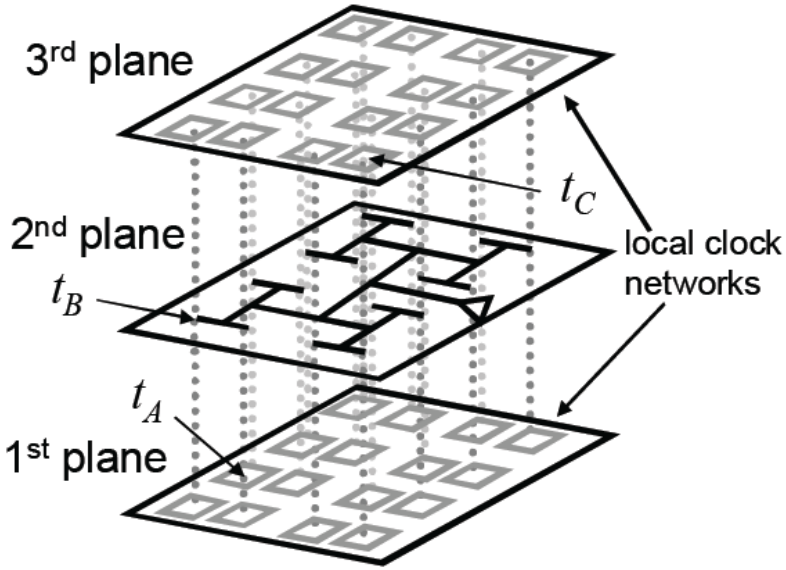
CDNs in 3-D circuits

- **Synthesized 3-D clock tree**



A synthesized 3-D clock tree with 87 TSVs [1]

- **Symmetric 3-D clock tree**



3-D global H-trees spanning multiple planes. [2]

[1] J. Minz *et al.*, "Buffered Clock Tree Synthesis for 3D ICs Under Thermal Variations," *Proc. of ASPDAC*, 2008.
[2] V.F. Pavlidis, "Clock Distribution Networks for 3-D Integrated Circuits," *Proc. of IEEE CICC,* 2008.

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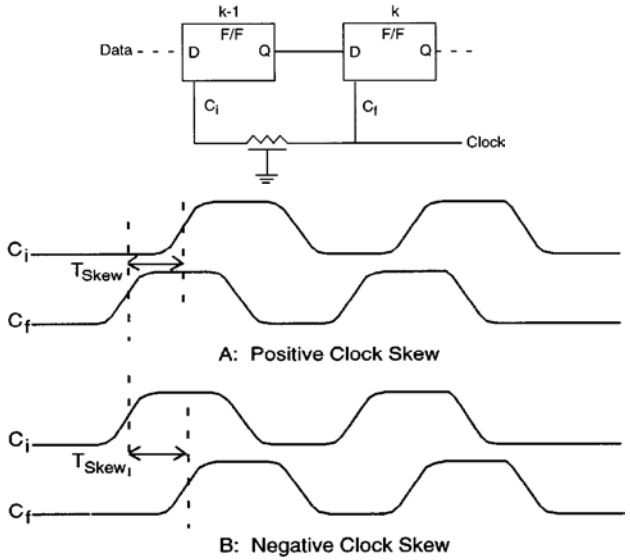
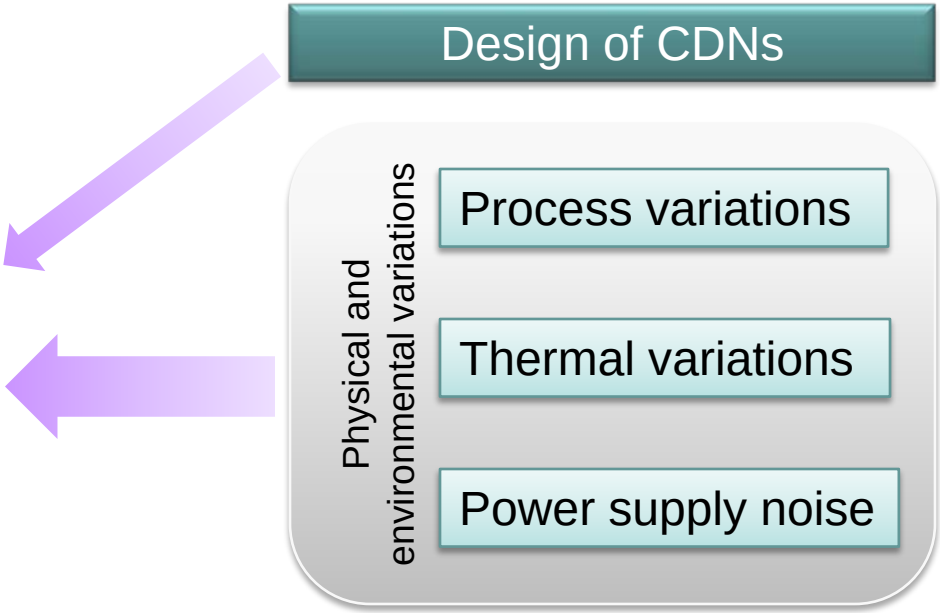
Skew of CDNs

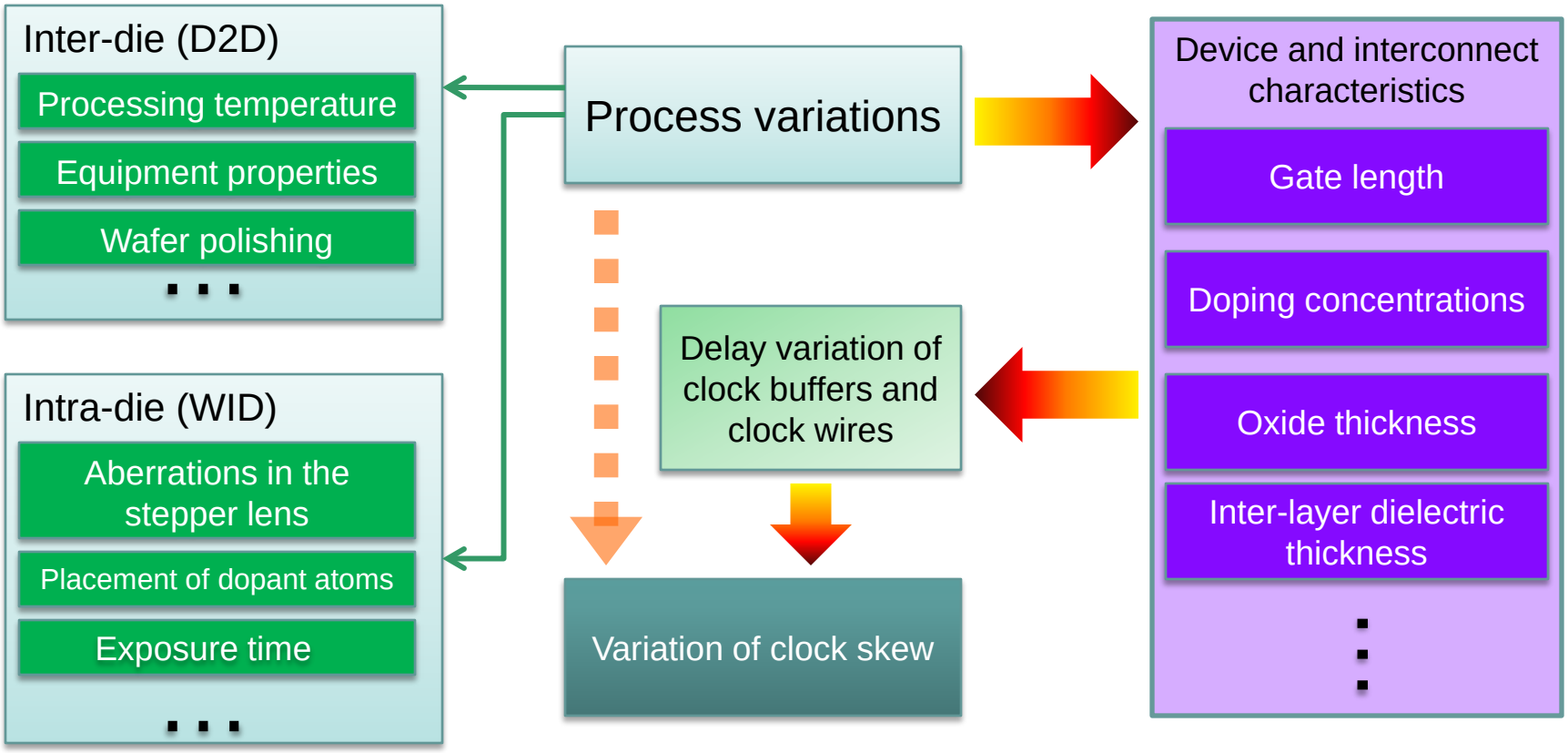
- Clock skew is the difference between the delay from the clock source to various clock sinks
  - Pair wise skew – the skew between each pair of sinks (data-related sinks)
  - Global skew – the skew between the minimum and maximum path delay
- The highest operating frequency of a circuit is constrained by the skew of the CDN





* E. Friedman, "Clock Distribution Networks in Synchronous Digital Integrated Circuits," *Proc. of the IEEE*, 89(5), 2001.

Sources of Process Variations



* K. Bowman *et al.*, "Impact of Die-to-Die and Within-Die Parameter Fluctuations on the Maximum Clock Frequency Distribution for Gigascale Integration," *IEEE Journal of Solid-State Circuits*, 37(2), pp.183-190, February, 2002.

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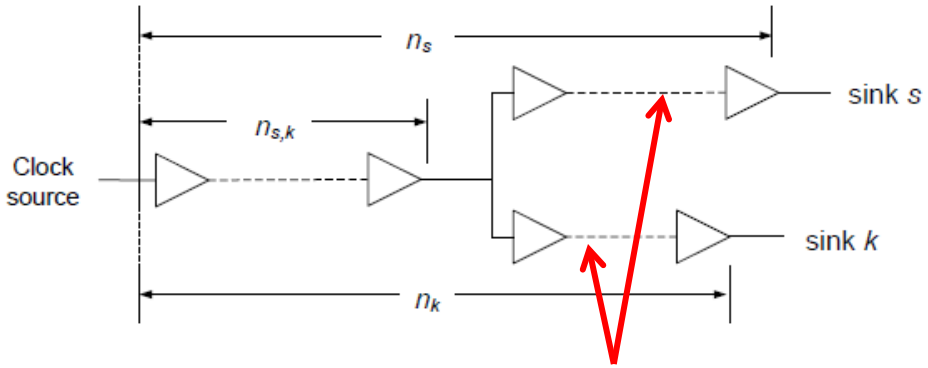
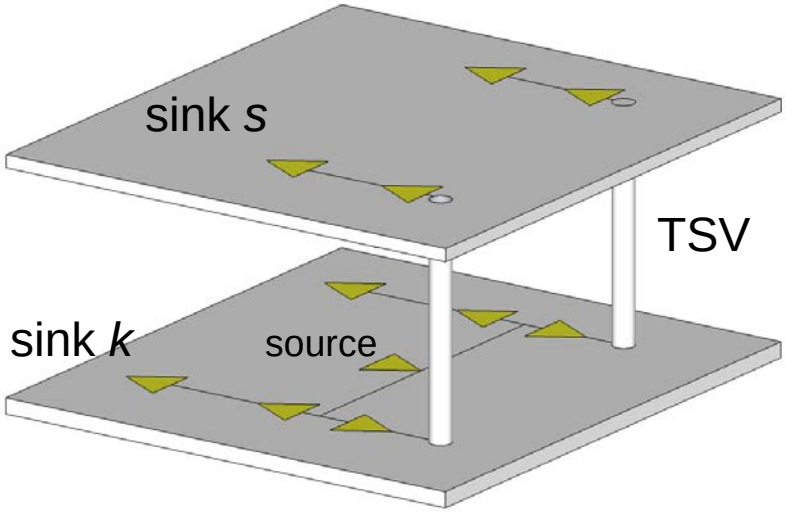
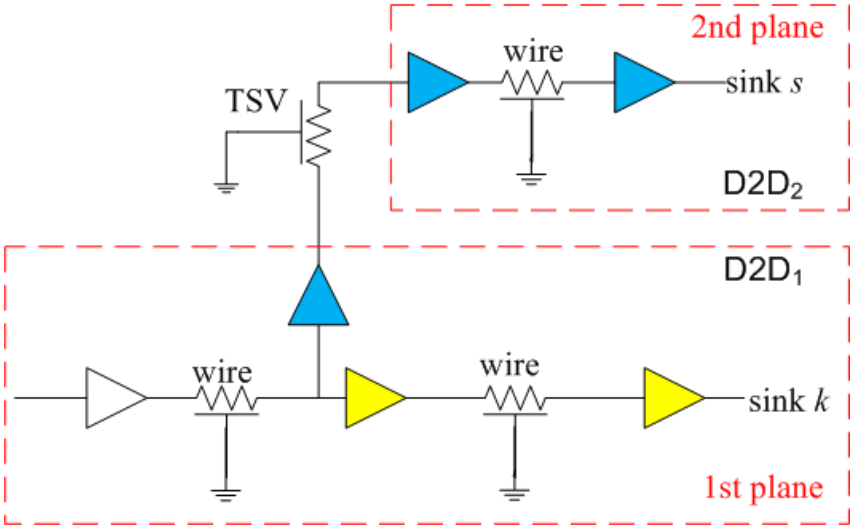
Modeling Process-Induced Skew in 2-D Clock Trees

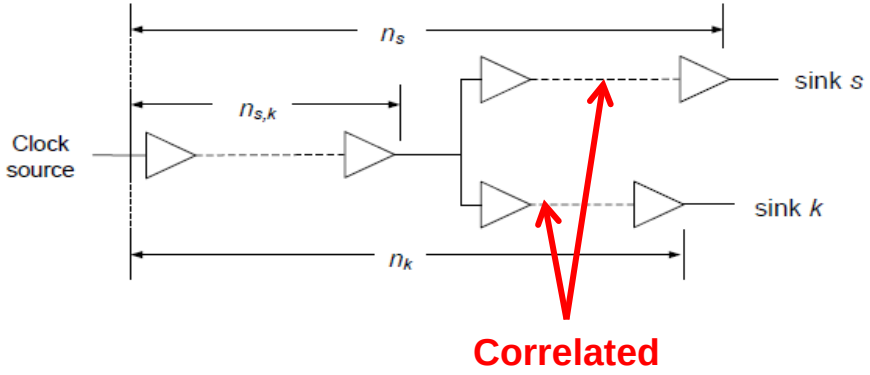
- Corner analysis (best/nominal/worst-case analysis) – coarse estimation
- Statistical skew analysis (SSA)
  - Only random variations (WID) are handled
  - The subpaths rooted at the same node are considered independent from each other
- Statistical static timing analysis (SSTA)
  - Apply SSTA to CDNs
  - The methodology and requirements are similar to SSA



Clock Paths in 3-D Clock Trees



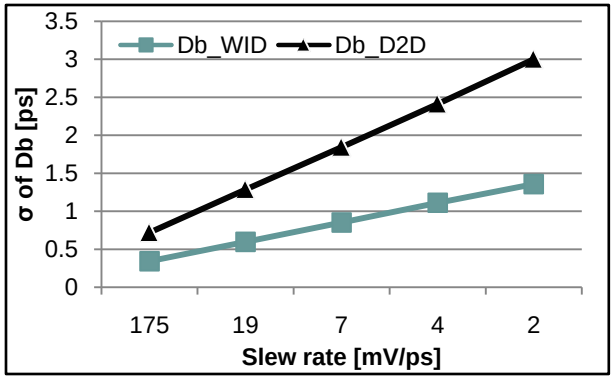


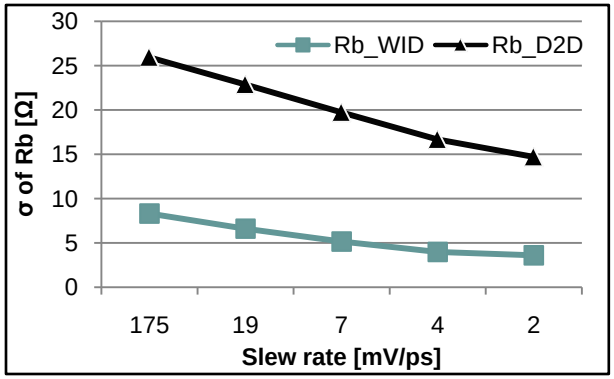


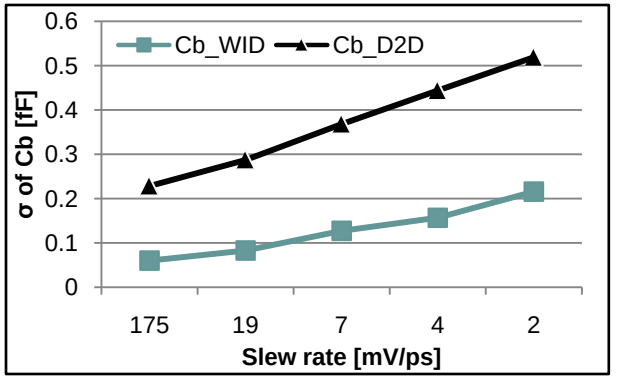
Correlated

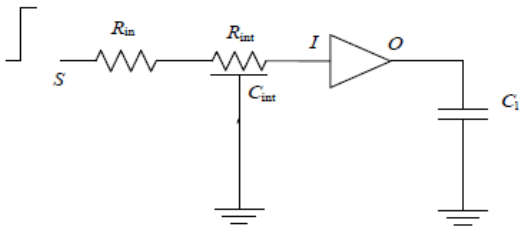
Distribution of Buffer Characteristics

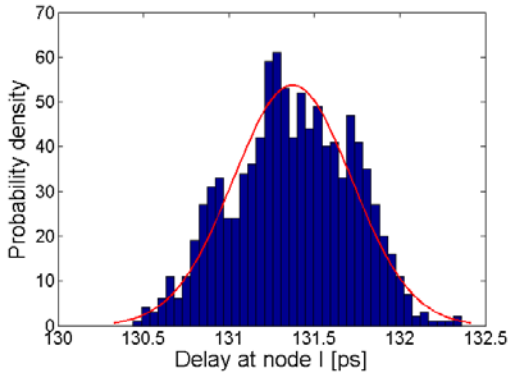
- The distribution of buffer characteristics depends on the input slew rate
- An elemental circuit is used to determine the PDF of D_b, R_b, C_b, which are considered as Gaussian distributions

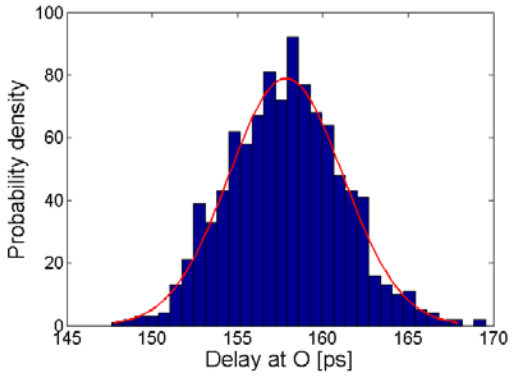












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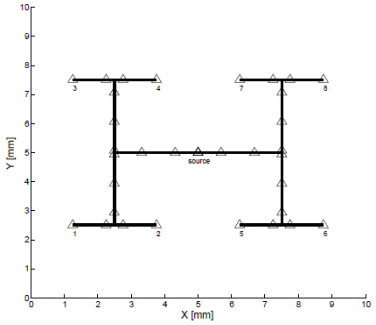
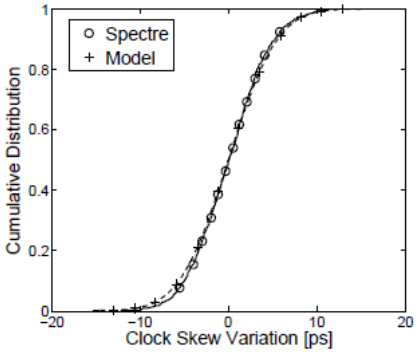
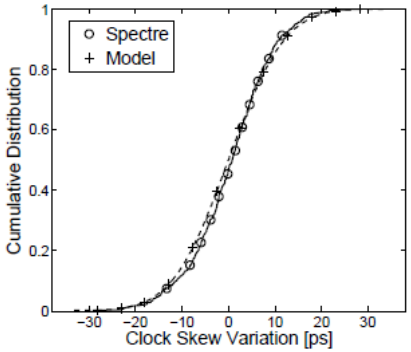
Accuracy of the Model

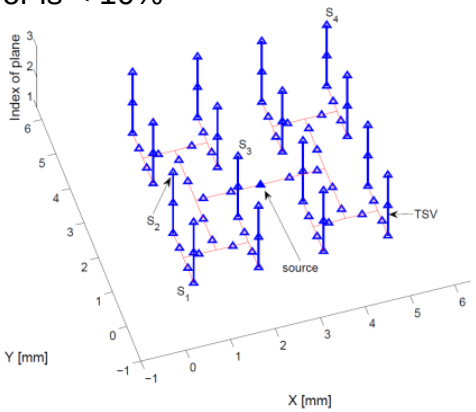
- 2-D CDNs
  - UMC 90 nm CMOS technology
  - Buffers are inserted under the same constraint of slew rate
  - The error compared with Monte-Carlo simulations is below 10%

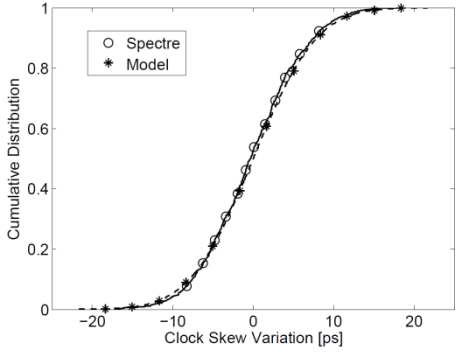


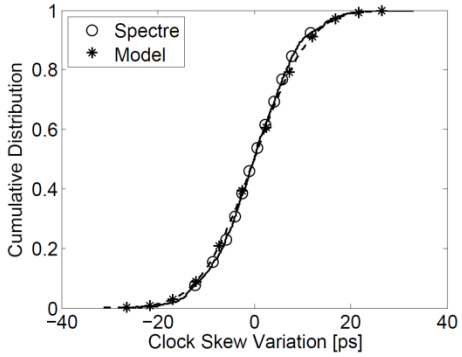




- 3-D CDNs
  - UMC 90 nm CMOS technology
  - Three planes, 48 sinks in total
  - The error is < 10%







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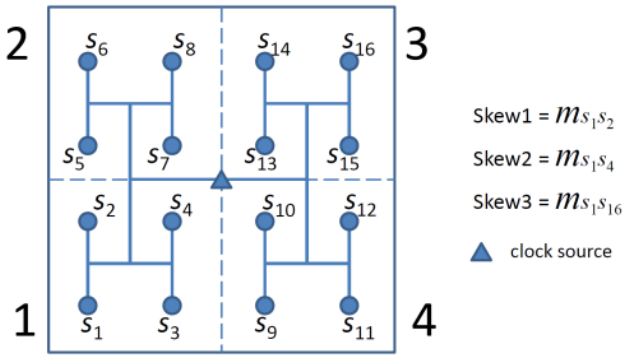
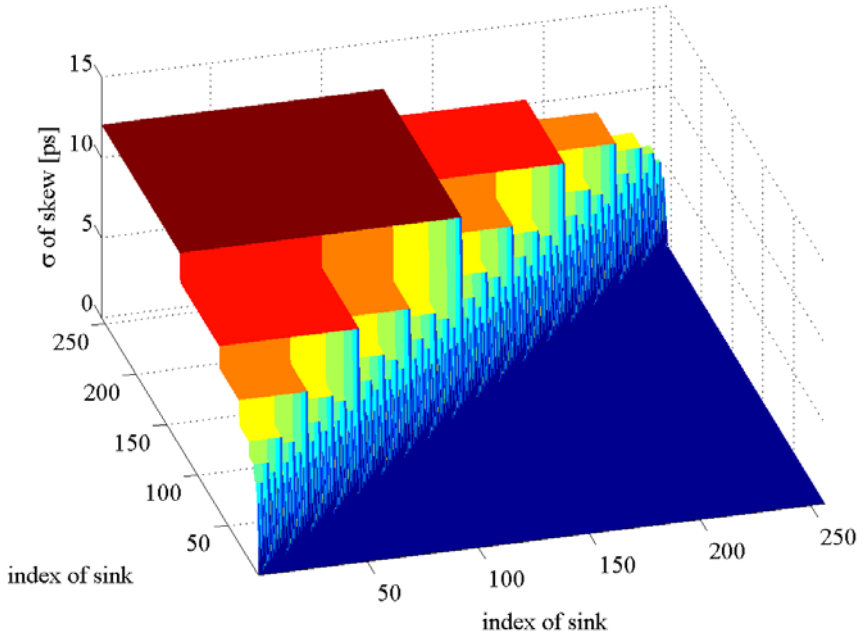
Skew Variation of Clock Trees in Scaled 2-D ICs

- A global clock H-tree with 256 sinks
  - The characteristics of buffers is obtained from ITRS
  - The σ of skew variation is compared for five technology nodes

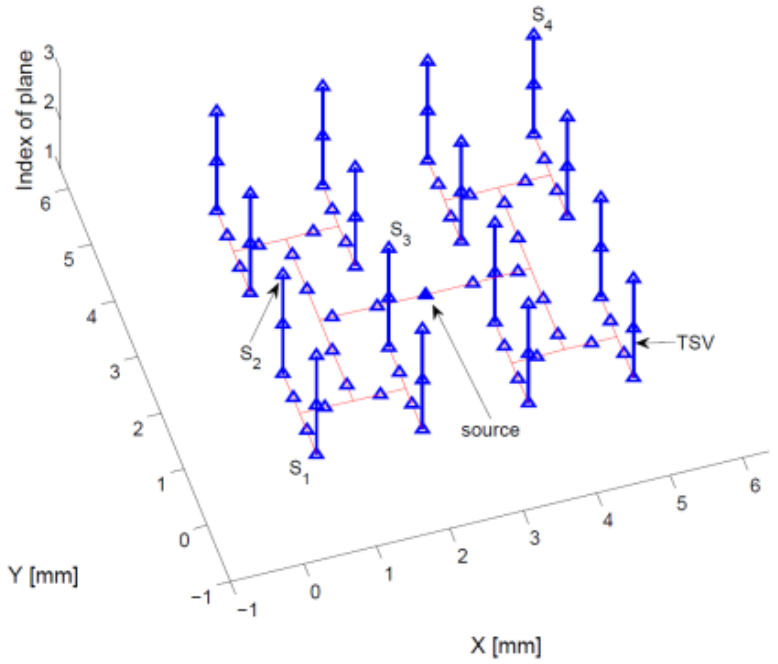




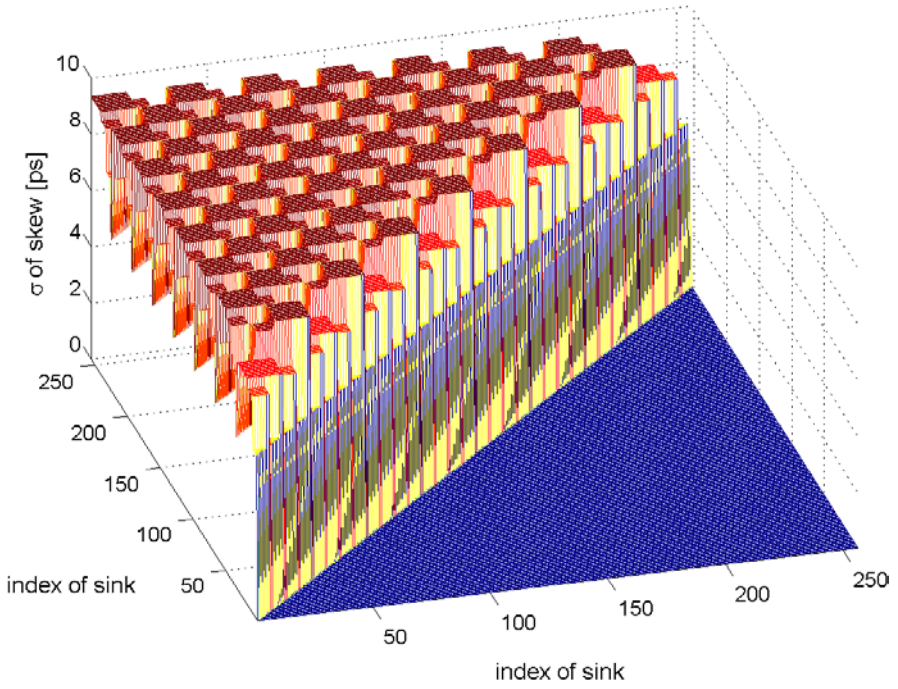
- Standard deviation array at 90 nm technology node

Skew Variation in 3-D Clock Trees

- A global clock H-tree with 256 sinks
  - The parameters are similar to the 2-D CDN at 90 nm technology node
  - The σ of the skew3 between the bottom and topmost planes is the largest



- Example of a 3-plane H-tree with 48 sinks

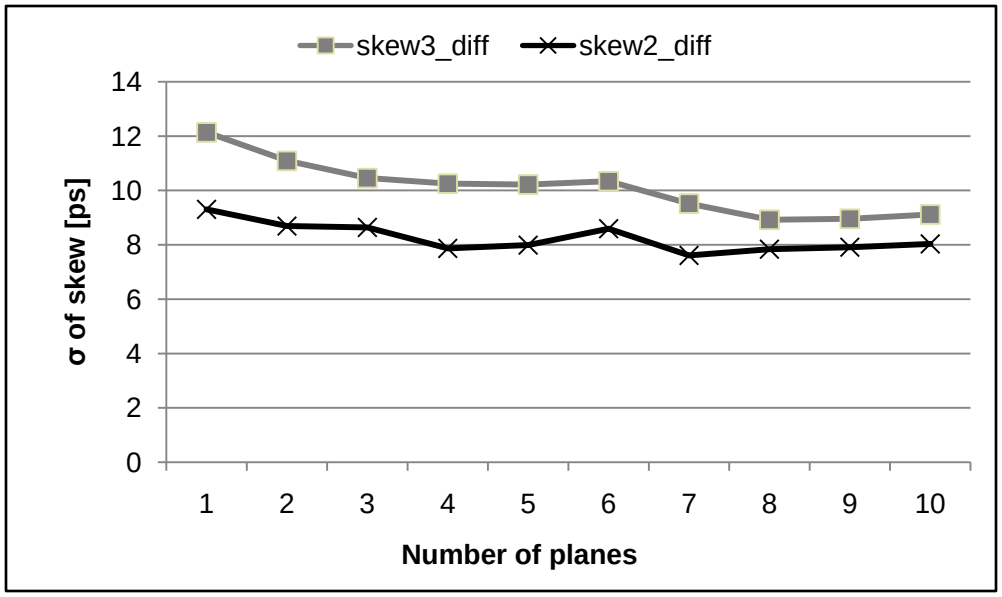


- σ of skew in a 8-plane H-tree

Skew Variation in 3-D ICs with Different Numbers of Planes

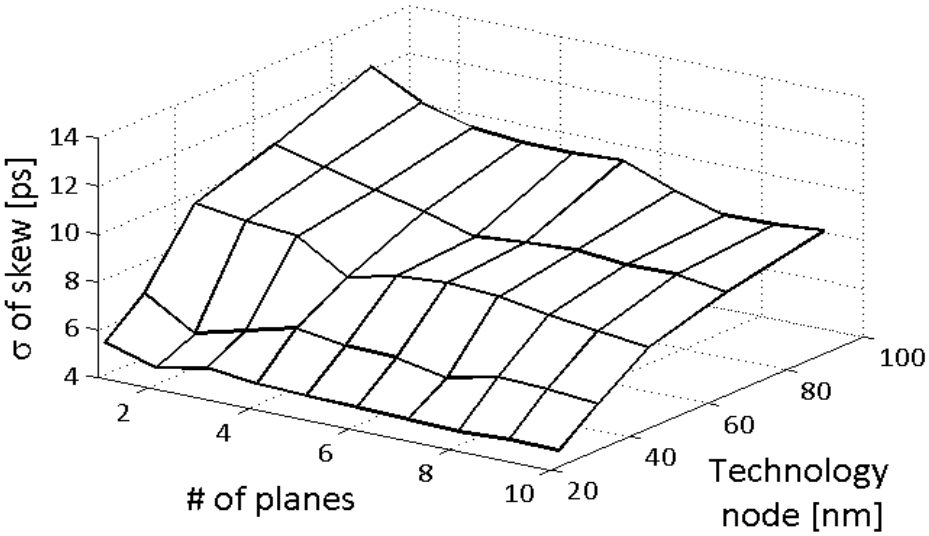
- The number of planes increases from one to ten
- The side length decreases with # of planes, $L_{plane} \propto \sqrt{\frac{A_1}{N}}$

# of planes	1	2	3	4	5	6	7	8	9	10
μ [fs]	0	2.9	9.8	20.9	36.0	55.2	78.5	106	137	173
σ [ps]	12.1	11.1	10.5	10.3	10.2	10.3	9.5	8.9	9.0	9.1
μ/σ [%]	0	0.0	0.1	0.2	0.4	0.5	0.8	1.2	1.5	1.9
f_{max} [GHz]	2.75	3.00	3.19	3.25	3.26	3.22	3.50	3.74	3.72	3.65



Comparison on Process-Induced Skew Variation between Technology Scaling and 3-D Integration

Tech. node	# of planes									
	1	2	3	4	5	6	7	8	9	10
90 nm	12.1	11.2	10.5	10.3	10.2	10.3	9.5	8.9	9.0	9.1
65 nm	10.6	10.1	9.6	9.1	8.5	8.7	8.8	8.6	8.6	8.3
45 nm	9.6	9.3	9.0	7.7	8.2	8.3	8.2	7.9	7.6	7.4
32 nm	6.7	5.4	6.0	6.5	6.2	6.2	5.7	6.2	6.1	5.9
22 nm	5.4	4.8	5.2	4.9	4.8	4.8	4.7	4.6	4.7	4.7



- The skew variation is shown to decrease more with technology scaling as compared to 3-D integration
- However, a multiplane circuit with a comparable or smaller skew variation can provide an alternative to aggressive technology scaling

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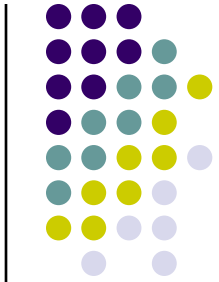

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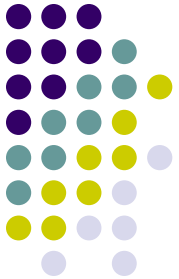
- The effect of process variations on the clock skew of scaled 2-D ICs and 3-D ICs is analyzed
- An accurate method to estimate the skew variation considering the input slew of buffers has been developed
- Skew variation decreases in different ways between technology scaling and 3-D integration
- Skew variation in 2-D ICs with technology scaling decreases more than in 3-D ICs
- 3-D integration provides an alternative to offer high device density and low process-induced skew variation



Thank you!