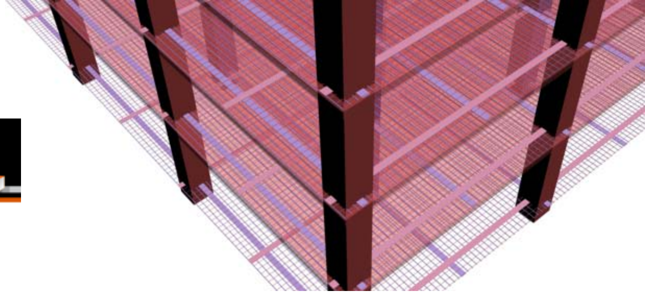
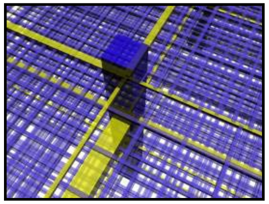
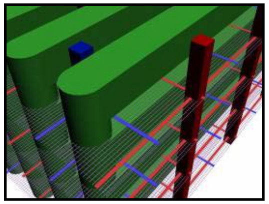
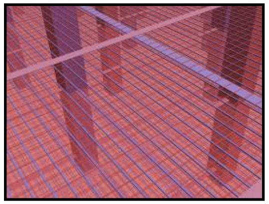
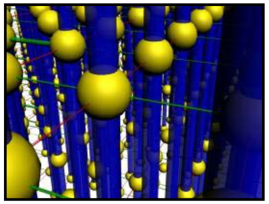


Through-Silicon-Via-Aware Delay and Power Prediction Model for Buffered Interconnects in 3D ICs

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Atlanta, Georgia, U.S.A.

SLIP'10, Anaheim, CA (06. 13. 2010.)

3D ICs

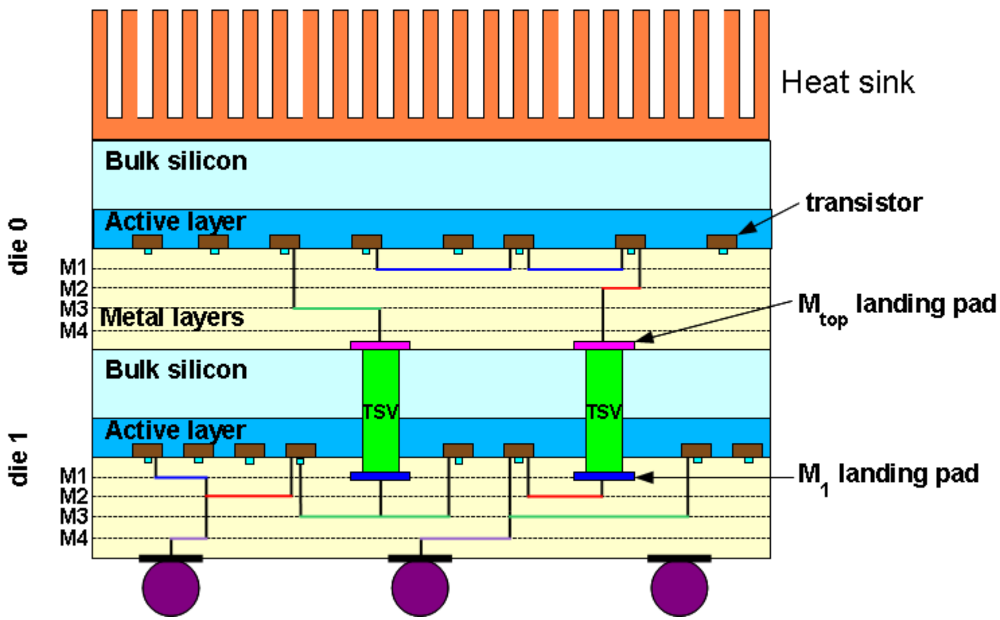
- Use of through-silicon vias (TSVs) + die stacking

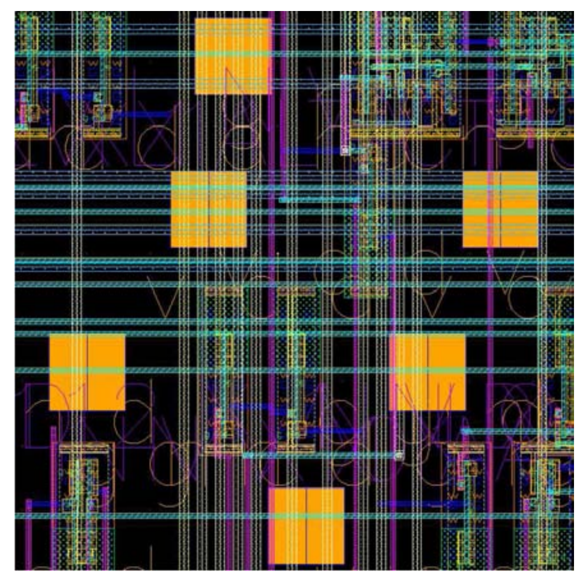
  → Smaller footprint area

  → Shorter wirelength

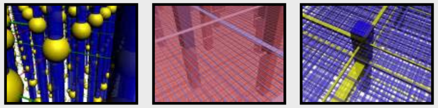
  → Better performance

  → Less interconnect power

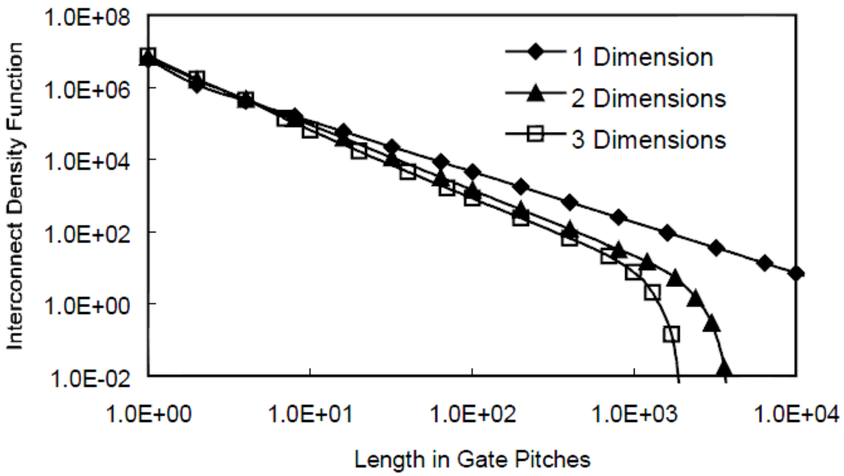




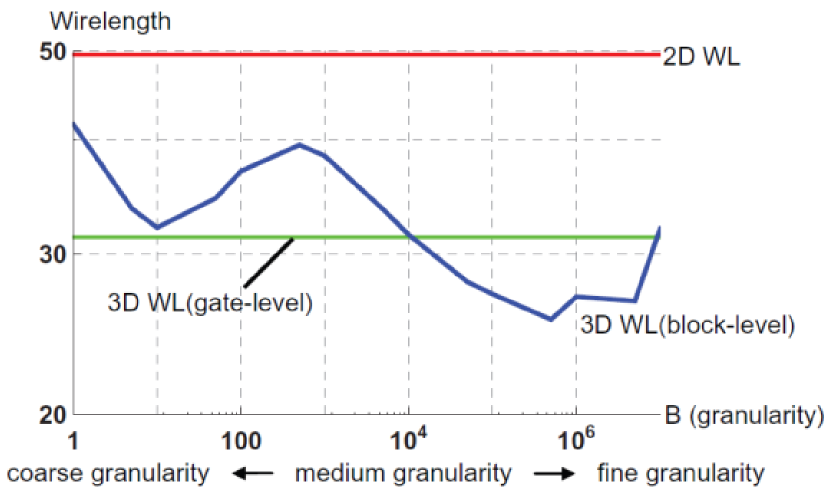
Three Aspects of 3D ICs (1/3) – Wirelength



- Several works have shown reduced total wirelength.
- Prediction studies
  - J. W. Joyner, P. Zarkesh-Ha, J. A. Davis, and J. D. Meindl, IITC’00 [1]
  - D. H. Kim, S. Mukhopadhyay, and S. K. Lim, SLIP’09 [2]



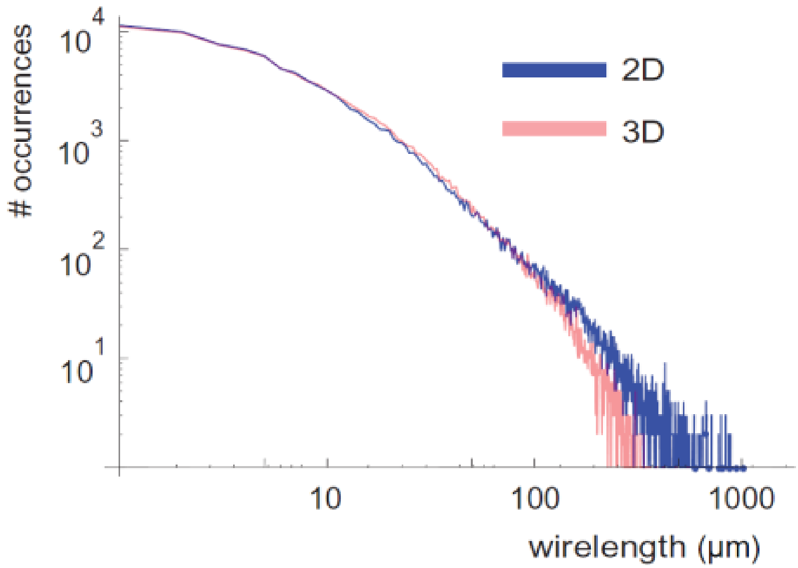
[1]



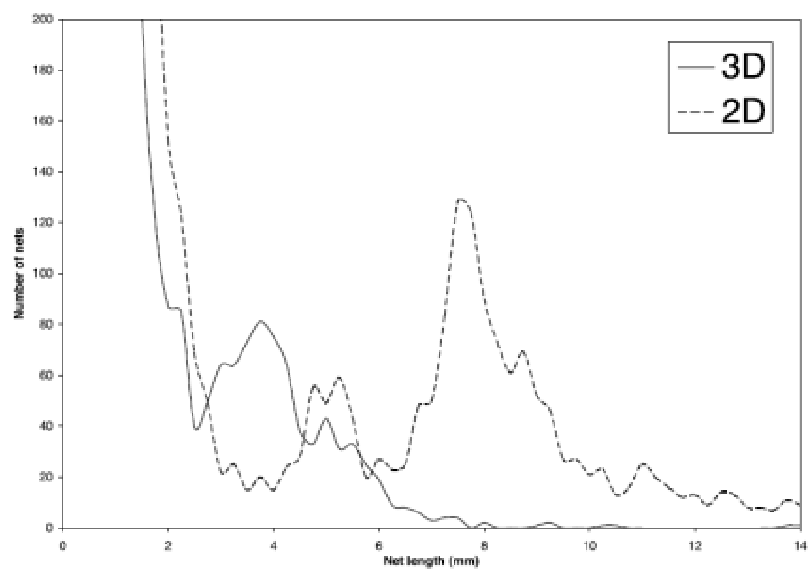
[2]

Three Aspects of 3D ICs (1/3)
– Wirelength

- GDSII-level design
  - D. H. Kim, K. Athikulwongse, and S. K. Lim, ICCAD'09 [3]
- Real chip design
  - T. Thorolfsson, K. Gonsalves, and P. D. Franzon, DAC'09 [4]

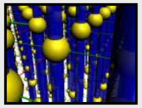
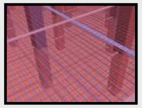
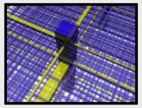


[3]

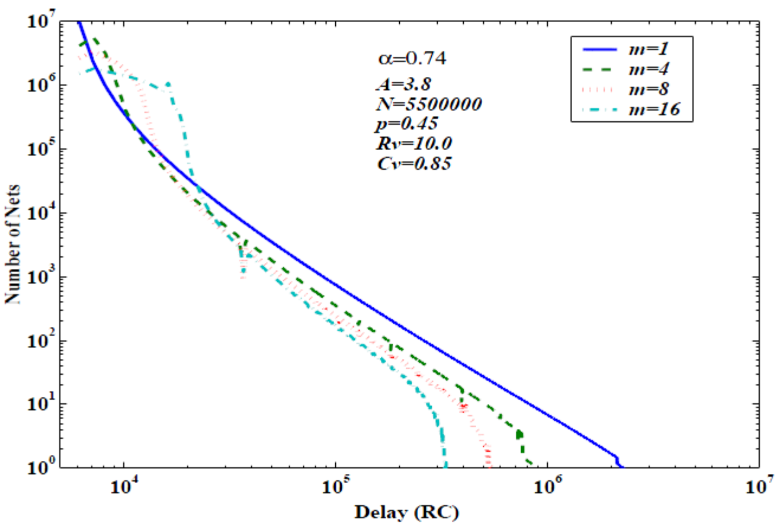


[4]

Three Aspects of 3D ICs (2/3)
– Delay

- Several works have shown decreased delay. (up to 24.6%)
- Prediction studies
  - R. Zhang, K. Roy, C.-K. Koh, and D. B. Janes, ICCAD'00 [5]
- Real chip design
  - T. Thorolfsson, K. Gonsalves, and P. D. Franzon, DAC'09 [4]

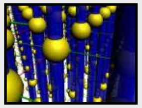
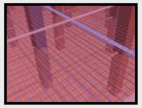
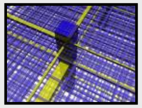


[5]

Metric	2D	3D	%
Total Area (mm^2)	31.36	23.40	25.3%
Core Area (mm^2)	29.16	20.16	30.9%
Mean Net Length (μm)	836.0	392.9	53.0%
Total Wire Length (m)	19.107	8.238	56.9%
Max Speed (MHz)	63.7	79.4	24.6%
Critical Path (ns)	15.7	12.6	19.7%
Logic Power @ 63.7MHz (mW)	340.0	324.9	4.4%
Logic Power @ 79.4 MHz (mW)	——	409.2	——
FFT Logic Energy (μJ)	3.552	3.366	5.2%

[4]

Three Aspects of 3D ICs (3/3)
– Power

- Several works have shown decreased power.
- Prediction studies
  - D. H. Kim, S. Mukhopadhyay, and S. K. Lim, IITC'09 [6]
- Real chip design
  - T. Thorolfsson, K. Gonsalves, and P. D. Franzon, DAC'09 [4]

# gates	# dies	Interconnect power ratio (3D/2D) (1) w/o TSV power	Interconnect power ratio (3D/2D) (2) with TSV power
4M	2	0.89	0.95
	4	0.83	0.96
40M	2	0.82	0.87
	4	0.71	0.80
400M	2	0.79	0.81
	4	0.63	0.68

[6]

Metric	2D	3D	%
Total Area (mm^2)	31.36	23.40	25.3%
Core Area (mm^2)	29.16	20.16	30.9%
Mean Net Length (μm)	836.0	392.9	53.0%
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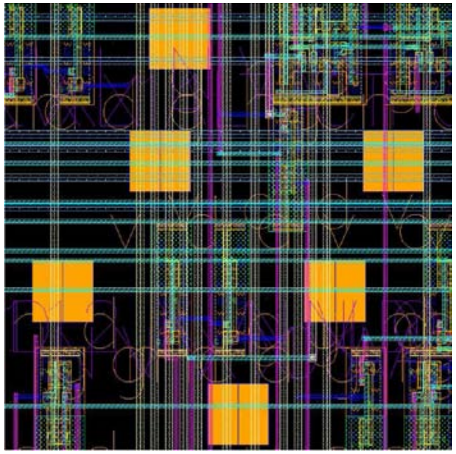
[4]

Side-Effects of Using TSVs



- **Additional silicon area**
  - TSVs occupy silicon area.
  - Total silicon area increases.
  - Wirelength reduction decreases.

- **Non-negligible TSV capacitance**
  - It could increase interconnect power.
  - It could increase the number of buffers.

TSV diameter (μm)	**Liner thickness (nm)**	$N_a(/cm^3)$	$C_{TSV}(fF)$
5	120	$2*10^{15}$	37.20
5	120	$1*10^{17}$	69.98
2	50	$2*10^{15}$	21.65
2	50	$1*10^{17}$	52.37

● Source: G. Katti *et al.*, TED'10

Need for TSV-aware Models

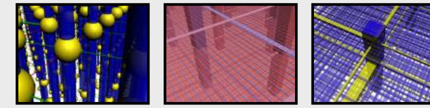
- **TSV-aware wirelength prediction model for 3D ICs**
  - D. H. Kim, S. Mukhopadhyay, and S. K. Lim, SLIP'09 [2]

Table 4: Impact of TSV size consideration on wirelength. N_{DIE} : 4, p_{gates} : 1, L_{gate} : 1.37μm and L_{TSV} : 1.37μm. $B = N_{gates}/N_{DIE}$ (gate-level).

r	N_{gates}	# TSVs	2D WL	TSV size consideration	3D WL	Δ WL
5	1M	0.66M	17.23	no	11.23	-34.82%
				yes	14.35	-20.07%
	100M	75.2M	53.96	no	29.82	-44.74%
				yes	40.00	-25.87%
30	1M	0.17M	17.23	no	13.37	-22.40%
				yes	14.82	-13.99%
	100M	24.3M	53.96	no	30.37	-43.72%
				yes	34.51	-36.05%

This table is from [2].

Non-TSV-Aware vs. TSV-Aware Prediction Models



- TSV-aware prediction models show more realistic pictures.

		Non-TSV-aware prediction model	TSV-aware prediction model
Wirelength	TSVs are treated as	Infinitely-small dots [1,5]	**Gates** [2]
	TSVs occupy silicon area	No [1,5]	**Yes** [2]
	Wirelength reduction	Significant [1,5]	**Acceptable** [2]
Delay & Power	TSVs are represented by	Wires of length $f(H_{TSV})$ [1]	**TSVs**
	TSV resistance	Wire resistance [5]	**TSV resistance**
	TSV capacitance	Wire capacitance [5]	**TSV capacitance**

+ Buffered interconnects

The goal of this paper.

[1]: J. W. Joyner, P. Zarkesh-Ha, J. A. Davis, and J. D. Meindl, IITC'00
[5]: R. Zhang, K. Roy, C.-K. Koh, and D. B. Janes, ICCAD'00

[2]: D. H. Kim, S. Mukhopadhyay, and S. K. Lim, SLIP'09

What to Consider For TSV-Aware Delay&Power Prediction

- **TSV resistance**
- **TSV capacitance**
- **“TSVs should be represented by TSVs.”**
- **Buffered interconnects**

What to Consider For TSV-Aware Delay&Power Prediction

- **TSV resistance**
- **TSV capacitance**
- **“TSVs should be represented by TSVs.”**
- **Buffered interconnects**

Wire vs. TSV

- **Wire (in 45*nm* technology)**

	M1	**M2, M3**	**M4 – M6**	**M7, M8**	**M9, M10**
Min. Width	65 *nm*	70 *nm*	0.14 μm	0.4 μm	0.8 μm
Thickness	0.13 μm	0.14 μm	0.28 μm	0.8 μm	2.0 μm

  – Resistance: 0.439 $\Omega/\mu m$ (M4-M6)

  – Capacitance: 0.171 *fF*/*um* (M4-M6)

● Source: NCSU FreePDK 45nm.
(http://www.eda.ncsu.edu/wiki/FreePDK)

- **TSV (via-first, 5μm width)**
  – Resistance: very small (~ mΩ)

  – Capacitance: 5 *fF* ~ 100 *fF* /TSV

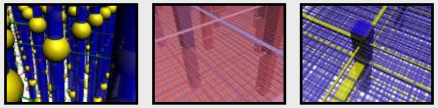
● Source: I. Savidis and E. G. Friedman, TED'09,
G. Katti *et al*., TED'10,
and from our own Raphael simulation

- **TSVs cannot be directly converted into wires**.

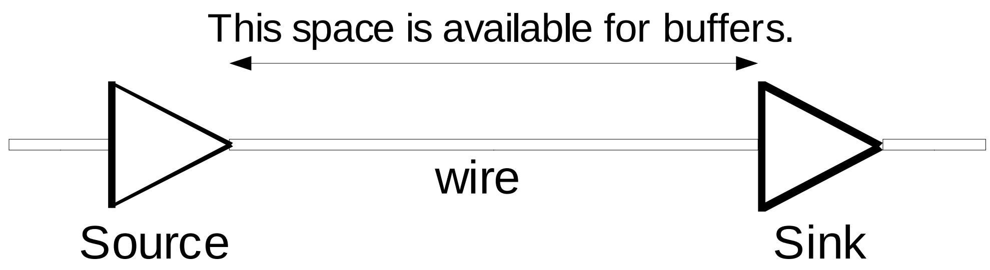
What to Consider For TSV-Aware Delay&Power Prediction

- **TSV resistance**
- **TSV capacitance**
- **“TSVs should be represented by TSVs.”**
- **Buffered interconnects**

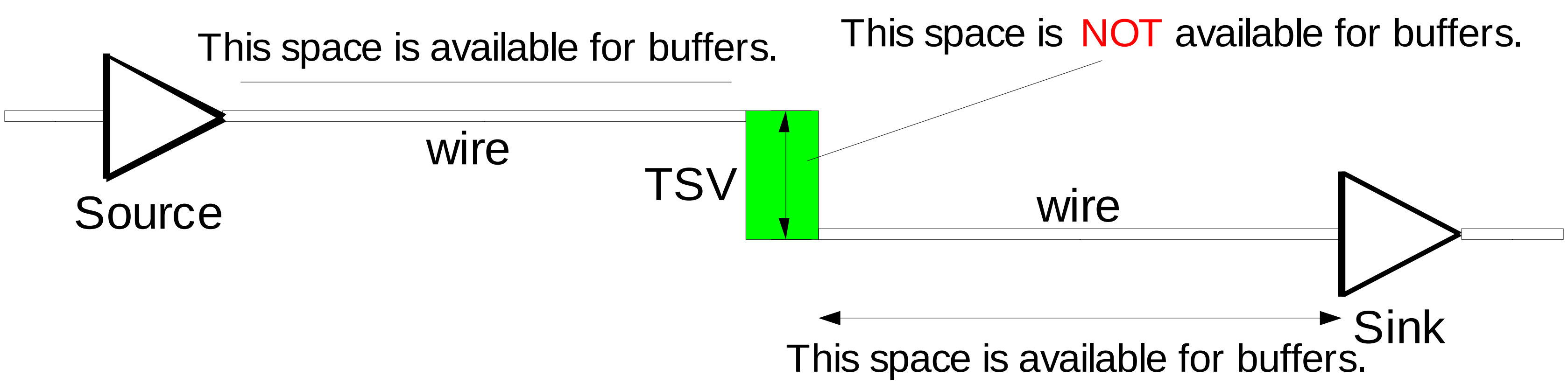
Buffered Interconnects in 2D & 3D ICs



- **In 2D ICs**

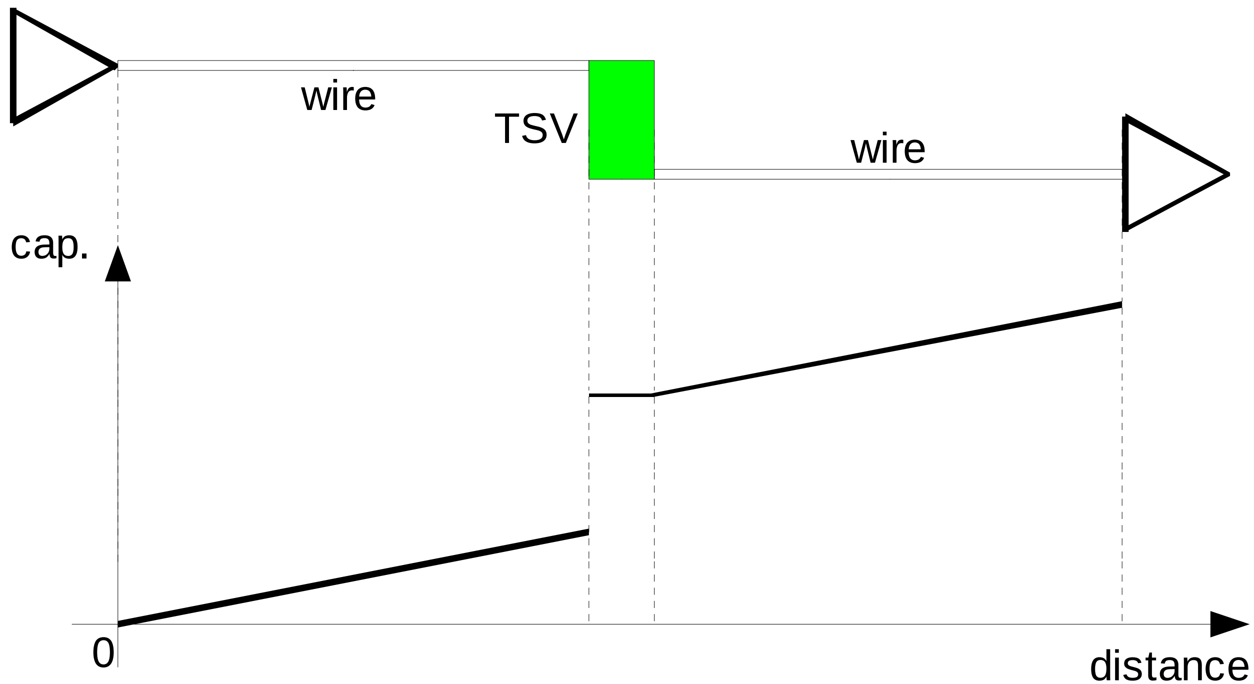


- **In 3D ICs**

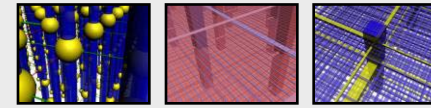


Distance – Capacitance Plot

- **3D wire**



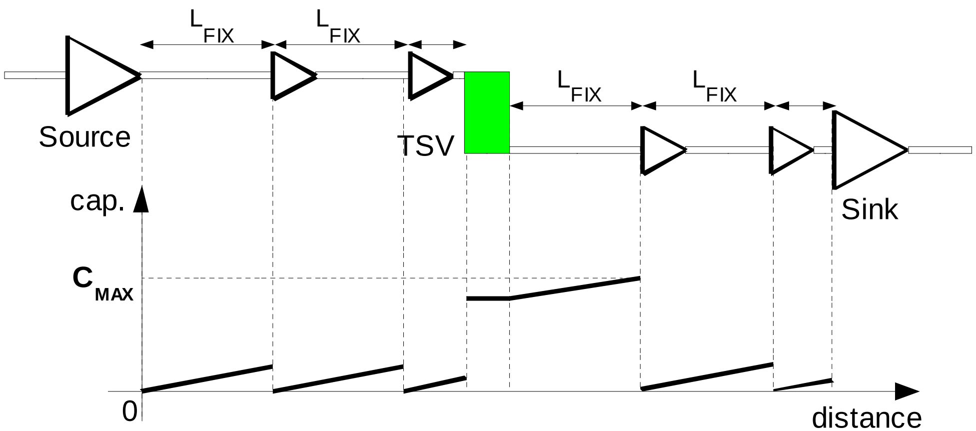
What to Consider For TSV-Aware Delay&Power Prediction



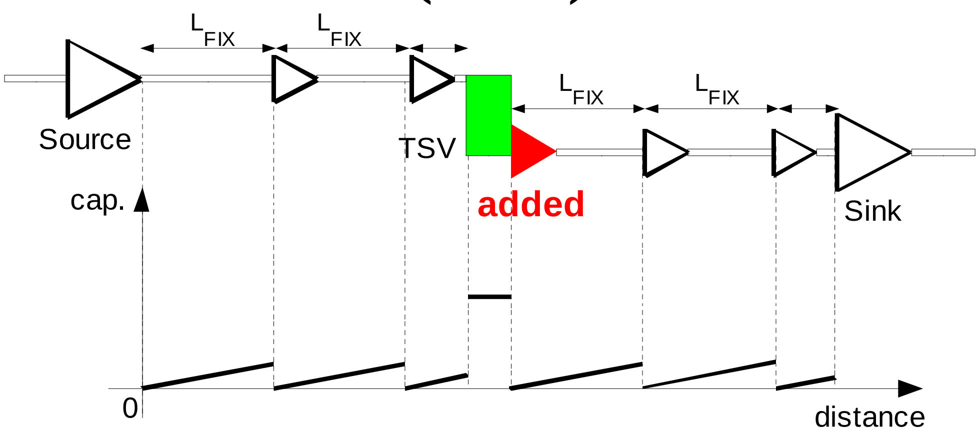
- **TSV resistance**
- **TSV capacitance**
- **"TSVs should be represented by TSVs."**
- **Buffered interconnects**

Buffer Insertion Schemes

- **Buffer Insertion Scheme 1 (BIS1)**



- **Buffer Insertion Scheme 2 (BIS2)**



L_{FIX}: 200μm

Experimental Results

1. Maximum delay and buffer count

2. Impact of TSV RC on short and medium wires

3. Impact of TSV RC on delay in different circuit sizes

4. Impact of TSV RC on power

5. Impact of buffer insertion on silicon area

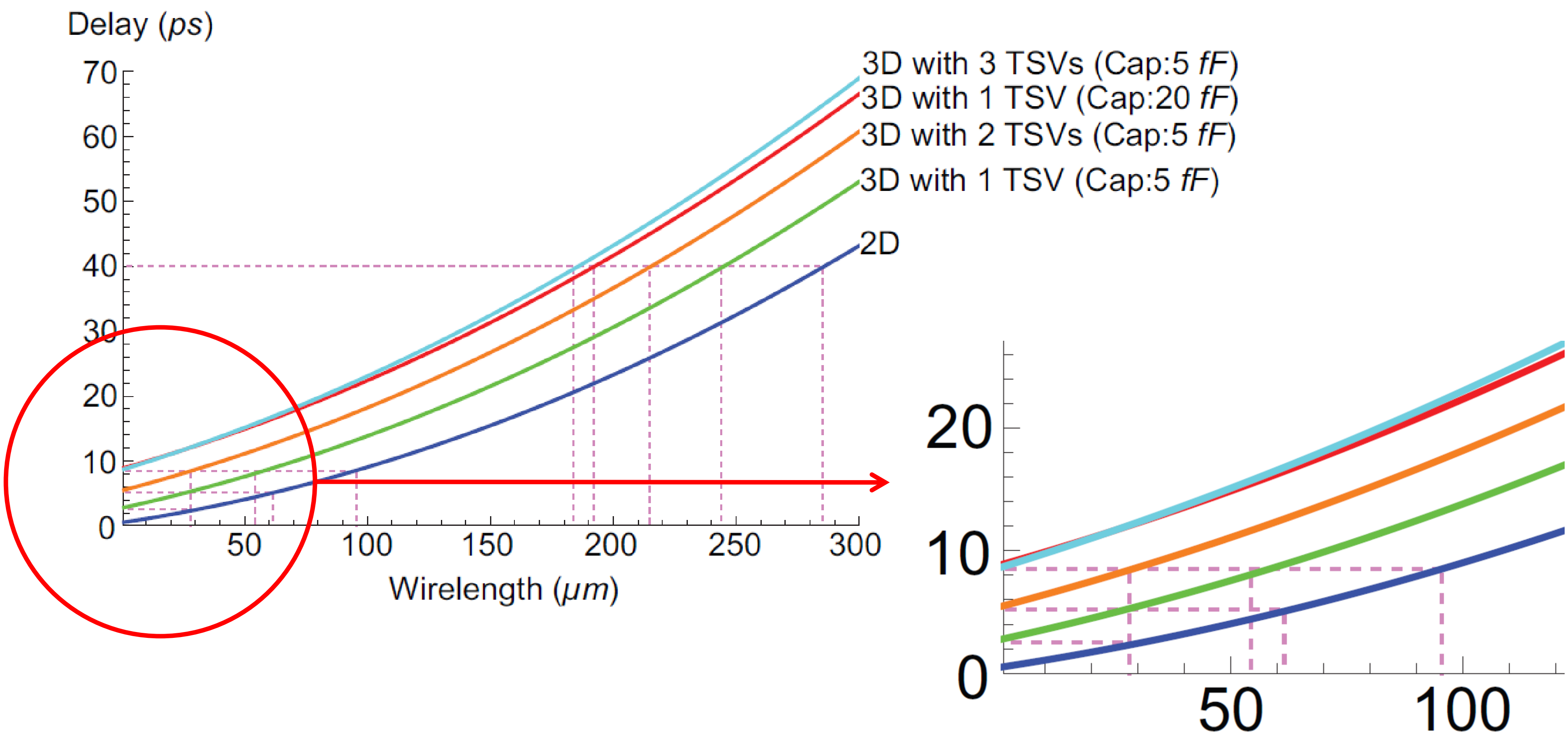
Experimental Results 1/5 – Max. Delay and Buffer Count

- # gates:40M (footprint area:100mm^2 (2D), 25mm^2 (3D))
- # dies:4
- # signal TSVs:8.3M

		(# buffers)	Max. delay			
				TSV cap. (*fF*)		
				5	20	50
2D		w/o B.I.	61.3 *ns*			
		BIS1 (9.8 *M*)	**5.29** *ns*			
3D	w/o TSV RC	w/o B.I.	23.5 *ns*			
		BIS1 (4.94 *M*)	3.24 *ns*			
	with TSV RC	w/o B.I.		23.5 *ns*	24.0 *ns*	25.4 *ns*
		BIS1 (11.8 *M*)		**9.22** *ns*	**9.23** *ns*	**9.24** *ns*
		BIS2 (20.1 *M*)		**3.56** *ns*	**3.57** *ns*	**3.61** *ns*

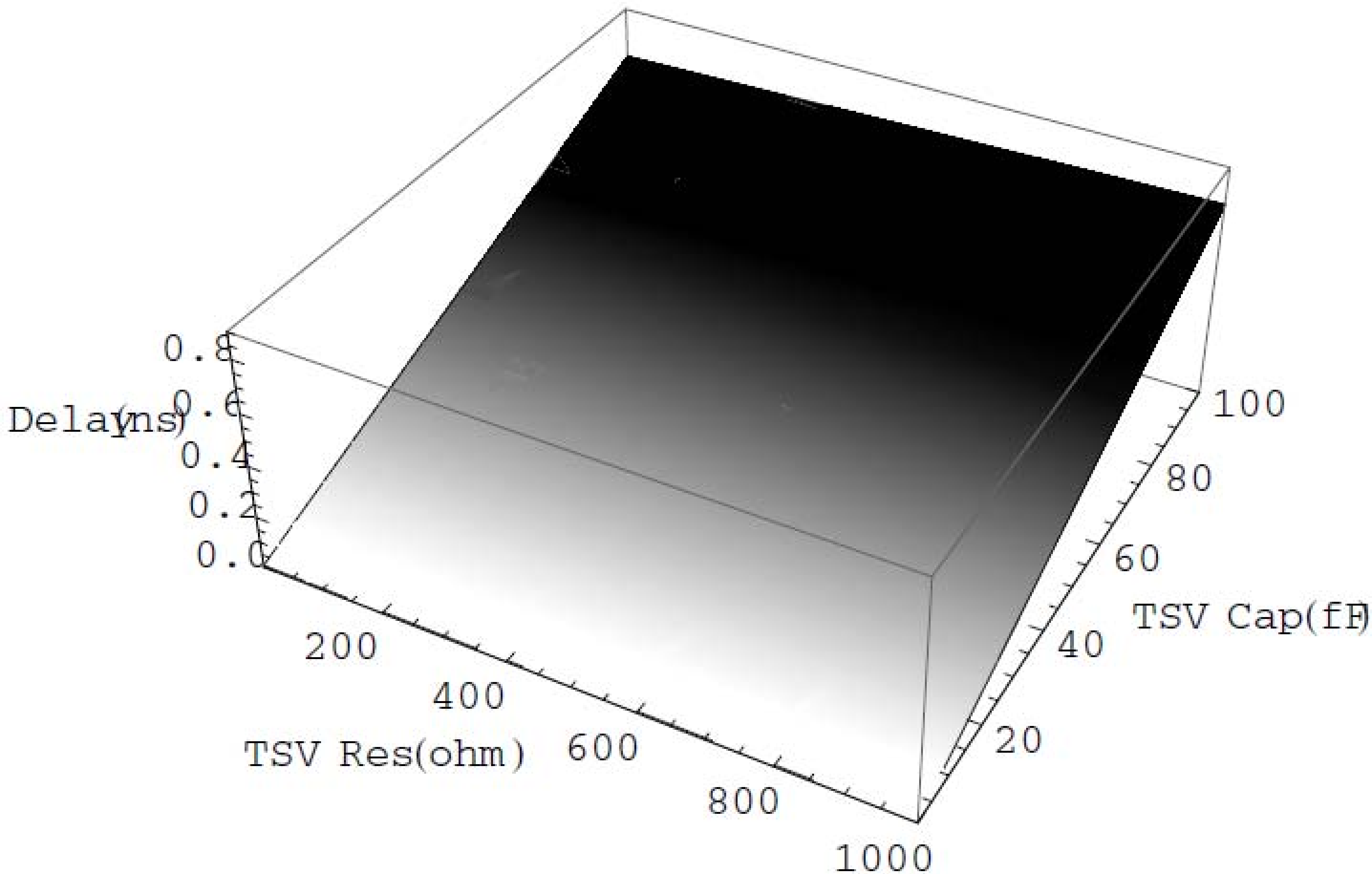
Experimental Results 2/5 –
Impact of TSV RC on Short & Medium Wires

- Drive size : 20x, without buffer insertion

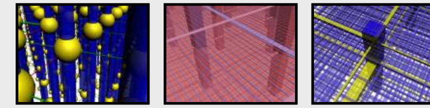


Experimental Results 2/5 –
Impact of TSV RC on Short & Medium Wires

- Sensitivity of TSV resistance and capacitance on delay



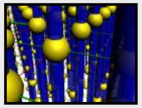
Experimental Results 3/5 –
Impact of TSV RC on Delay in Different Circuit Sizes

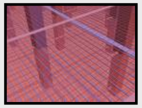


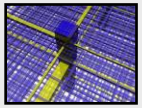
- Max. delay and buffer count (in parentheses)
- TSV R:1Ω, C:20*fF*, # dies:4

			Circuit Area (mm^2)				
			1	25	100	225	400
		(# gates) →	400*K*	10*M*	40*M*	90*M*	160*M*
2D	BIS1		**0.52** *ns* (7.09 *K*)	**2.61** *ns* (1.38 *M*)	**5.29** *ns* (9.78 *M*)	**7.98** *ns* (29.6 *M*)	**10.7** *ns* (64.2 *M*)
3D	w/o TSV RC	BIS1	0.27 *ns* (1.90 *K*)	1.57 *ns* (0.66 *M*)	3.24 *ns* (4.94 *M*)	4.92 *ns* (15.3 *M*)	6.60 *ns* (33 *M*)
	with TSV RC	BIS1	**0.45** *ns* (51.7 *K*)	**3.12** *ns* (2.28 *M*)	**9.23** *ns* (12 *M*)	**18.5** *ns* (31 *M*)	**30.6** *ns* (62 *M*)
		BIS 2	**0.45** *ns* (103 *K*)	**2.00** *ns* (4.17 *M*)	**3.57** *ns* (20 *M*)	**5.18** *ns* (50 *M*)	**6.86** *ns* (97 *M*)

Experimental Results 4/5 – Impact of TSV RC on Power

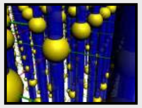
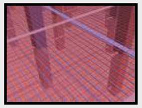
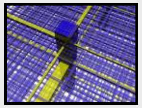






			Circuit Area (mm^2)				
			0.25	1.25	2.50	12.5	25.0
2D	BIS1		**0.49** W	**2.71** W	**6.16** W	**33.7** W	**73.5** W
3D	w/o TSV RC	BIS1	0.50 W (+2.04 %)	2.69 W (-0.74 %)	4.43 W (-28.1 %)	30.4 W (-9.79 %)	63.7 W (-13.3 %)
	with TSV RC (5 *fF*)	BIS1	0.53 W (+8.16 %)	2.88 W (+6.27 %)	5.98 W (-2.92 %)	32.7 W (-2.97 %)	68.7 W (-6.53 %)
		BIS2	0.55 W (+12.2 %)	3.02 W (+11.4 %)	6.27 W (+1.79 %)	34.5 W (+2.37 %)	72.4 W (-1.50 %)
	with TSV RC (20 *fF*)	BIS1	**0.58** W (+18.4 %)	**3.21** W (+18.5 %)	**6.72** W (+9.09 %)	**37.2** W (+10.4 %)	**78.1** W (+6.26 %)
		BIS2	**0.60** W (+22.4 %)	**3.35** W (+23.6 %)	**7.01** W (+13.8 %)	**39.0** W (+15.7 %)	**81.8** W (+11.3 %)
	with TSV RC (50 *fF*)	BIS1	0.65 W (+32.7 %)	3.71 W (+36.9 %)	7.82 W (+26.9 %)	43.9 W (+30.3 %)	92.3 W (+25.6 %)
		BIS2	0.67 W (+36.7 %)	3.85 W (+42.1 %)	8.11 W (+31.7 %)	45.7 W (+35.6 %)	96.0 W (+30.6 %)

Experimental Results 5/5 –
Impact of Buffer Insertion on Silicon Area

- Notice that our buffer insertion scheme is very aggressive. (We insert buffers into all nets although some of them do not need buffers).

			Circuit Area (mm^2)						
			0.25	1.25	2.50	12.5	25.0	125.1	250.3
2D	BIS1		**0.0004** (+0.16 %)	**0.02** (+1.60 %)	**0.07** (+2.80 %)	**1.4** (+11.2 %)	**2.63** (+10.5 %)	**25.0** (+20.0 %)	**64.0** (+25.6 %)
3D	w/o TSV RC	BIS1	0.0001 (+0.04 %)	0.01 (+0.80 %)	0.03 (+1.20 %)	0.43 (+3.40 %)	1.24 (+4.96 %)	12.7 (+10.2 %)	33.0 (+13.2 %)
	with TSV RC	BIS1	**0.02** (+8.0 %)	**0.13** (+10.4 %)	**0.29** (+11.6 %)	**1.90** (+15.2 %)	**4.28** (+17.1 %)	**28.9** (+23.1 %)	**66.1** (+26.4 %)
		BIS 2	**0.04** (+16.0 %)	**0.25** (+20.0 %)	**0.56** (+22.4 %)	**3.57** (+28.6 %)	**7.83** (+31.3 %)	**48.6** (+38.8 %)	**106.8** (+42.7 %)

Conclusions

- **TSV characteristics**
  - TSVs occupy silicon area.
  - TSV capacitance is not negligible.
- **Prediction models for delay and power of 3D ICs**
  - We should consider TSV characteristics shown above.
  - We should treat TSVs not as wires but as TSVs.
- **Buffer insertion in 3D ICs**
  - BIS1 has less area usage but higher delay.
  - BIS2 has bigger area usage but lower delay.
  - There is a strong need for development of buffer insertion algorithms for 3D ICs considering TSV capacitance.

Welcome Your Questions !!