Fast, Accurate A Priori Routing Delay Estimation

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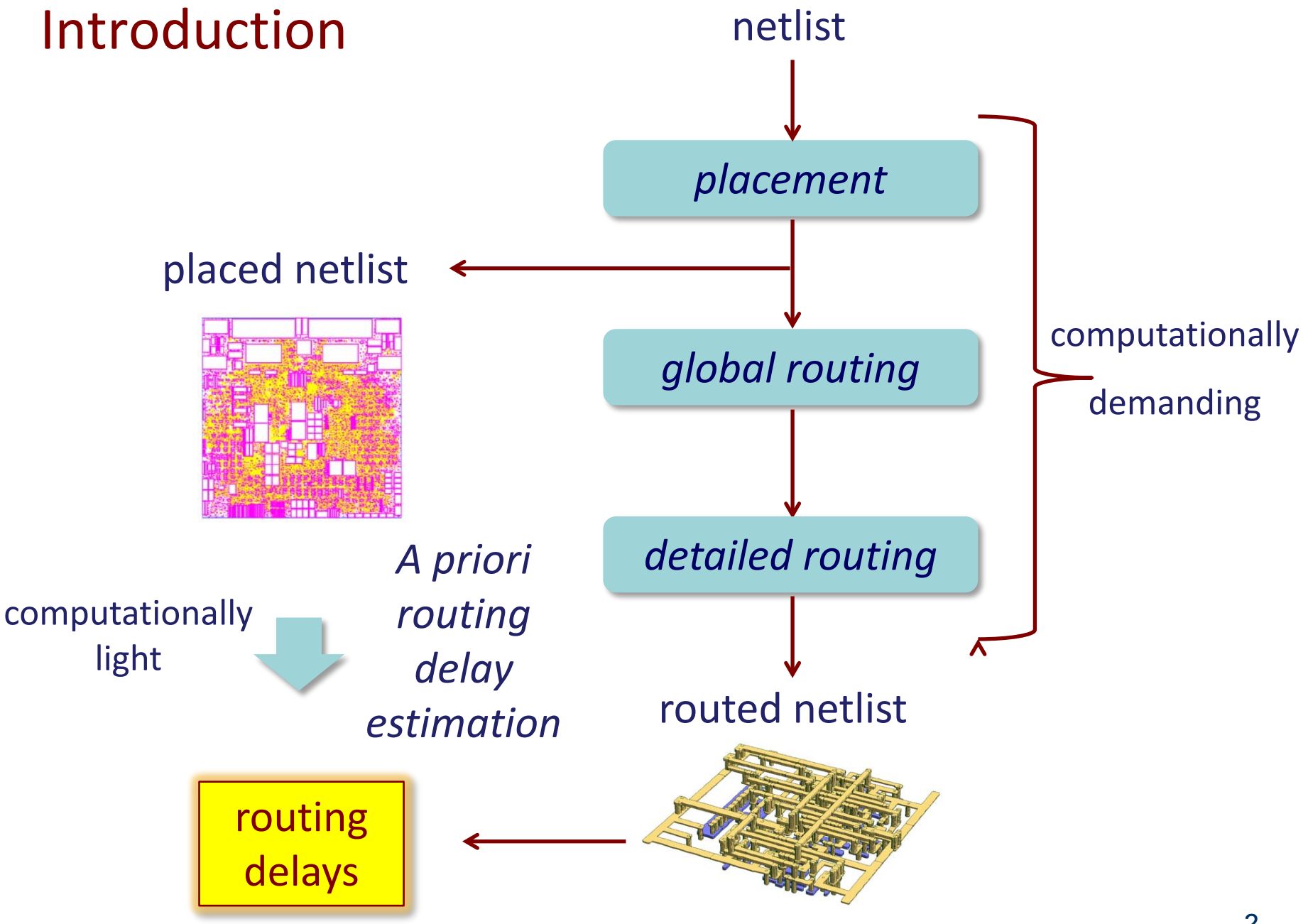
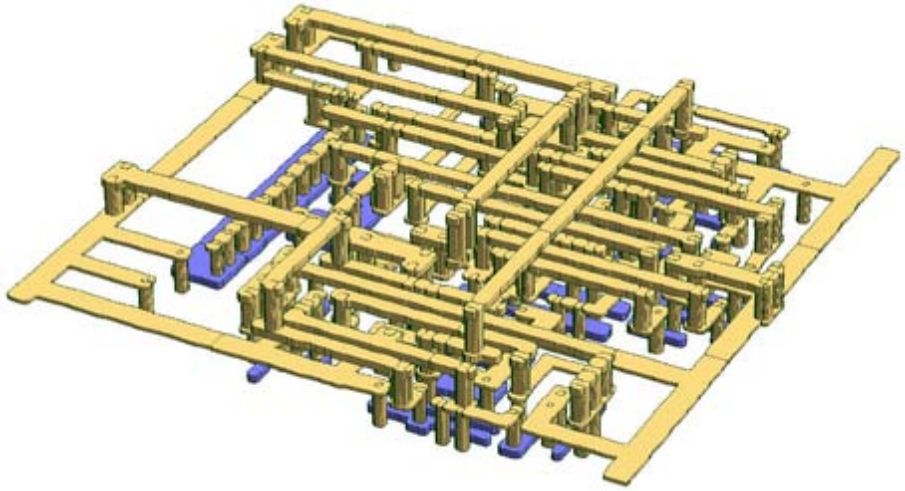
Introduction



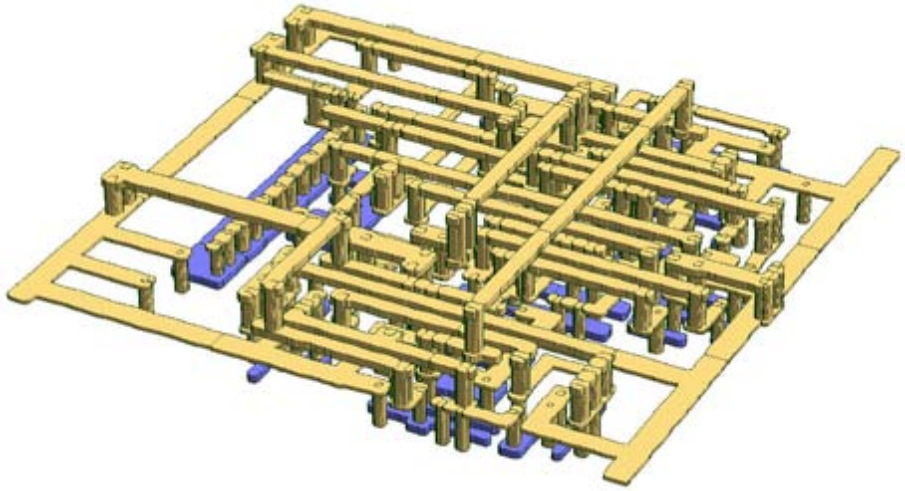
Objectives



[image from wikipedia]

1. Detailed routing delay estimation
2. Accurate (at least better than delay from placement)
3. Fast look-up table based technique
4. Implement and verify within an industrial flow

Challenges in routing delay estimation



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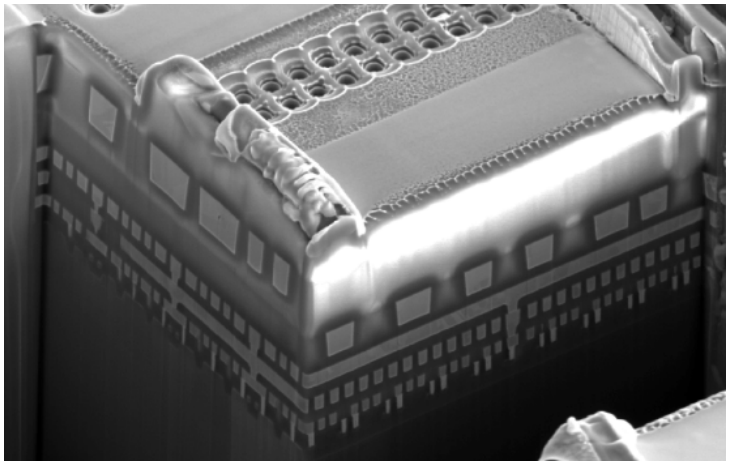
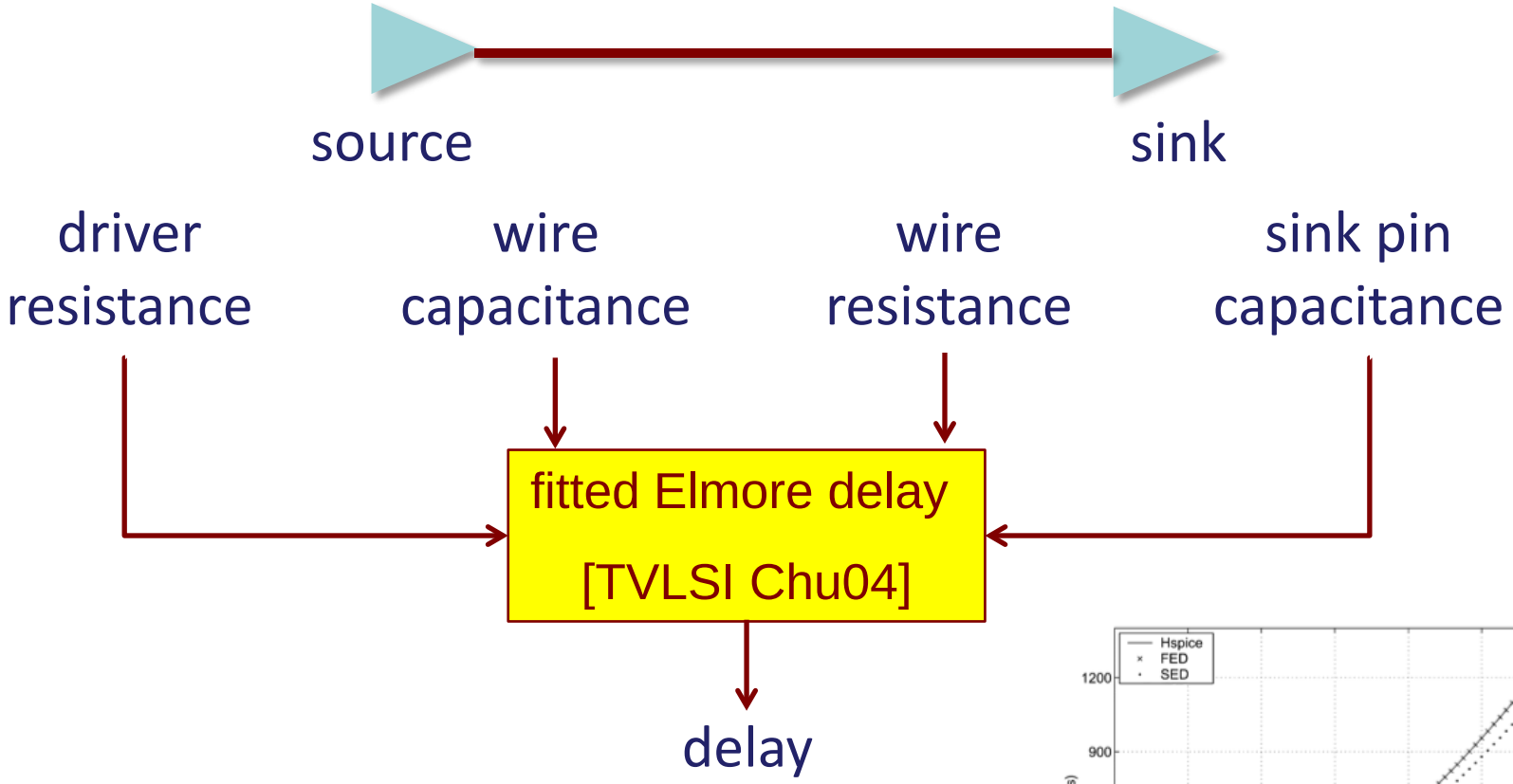
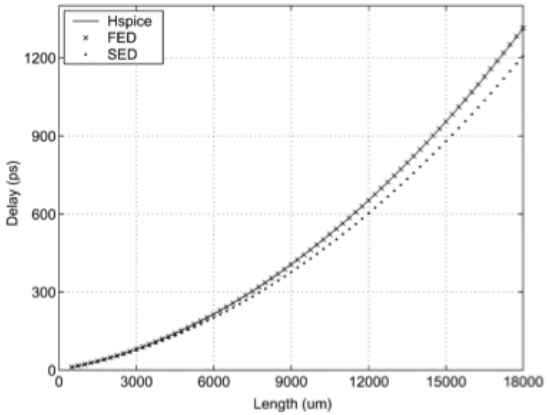


[image using Brown's FIB facility]

1. Metal layer assignment
2. Detours due to congestion and blockages
3. Cross talk from neighboring wires

Computing wiring delays





- How to know the exact R, C, and delay for a routed net given only the placement of its nodes?

Overview of proposed techniques

- Available information after placement:
  - Net degree
  - Pin locations and capacitances
  - Steiner tree length

"A lack of information cannot be remedied by any mathematical trickery," C. Lanczos 1961.

- Approach:
  - Build empirical models and look-up tablesto characterize the results of a router on known designs.
  - Apply these models to placements of variant or new designs

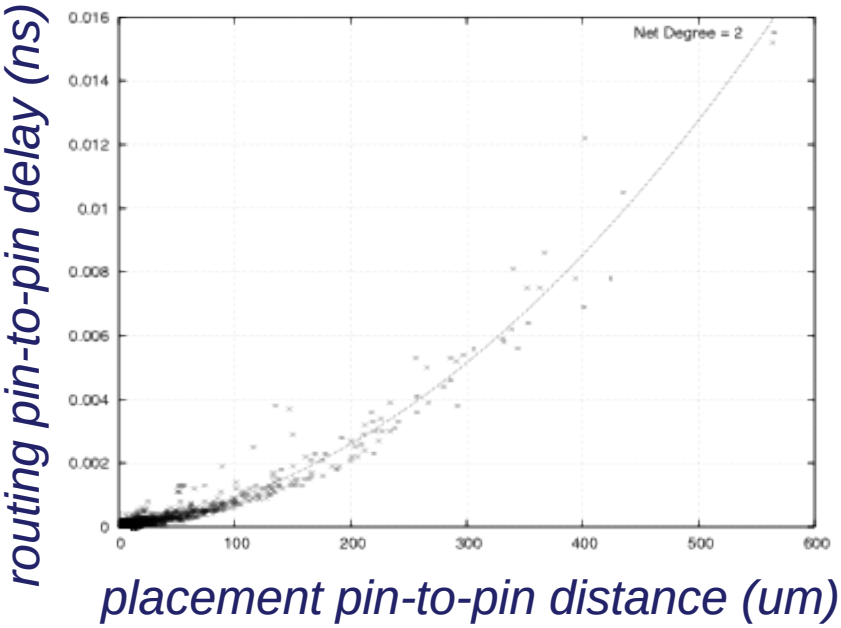
Rationale

- Empirical models quantify common-sense physical design characteristics:
  - Long nets are likely to be routed on top metal layers
  - Nets with larger degrees are likely to encounter more congestion
- Router-specific sorting rules or tie breaking mechanisms lead to systematic routing delay characteristics that can be captured our method
- Some of the popular estimation methods, e.g., RISA (Cheng93) for FLUTE (Chu04) Rectilinear Minimum Steiner Tree are empirical and lookup-table driven.

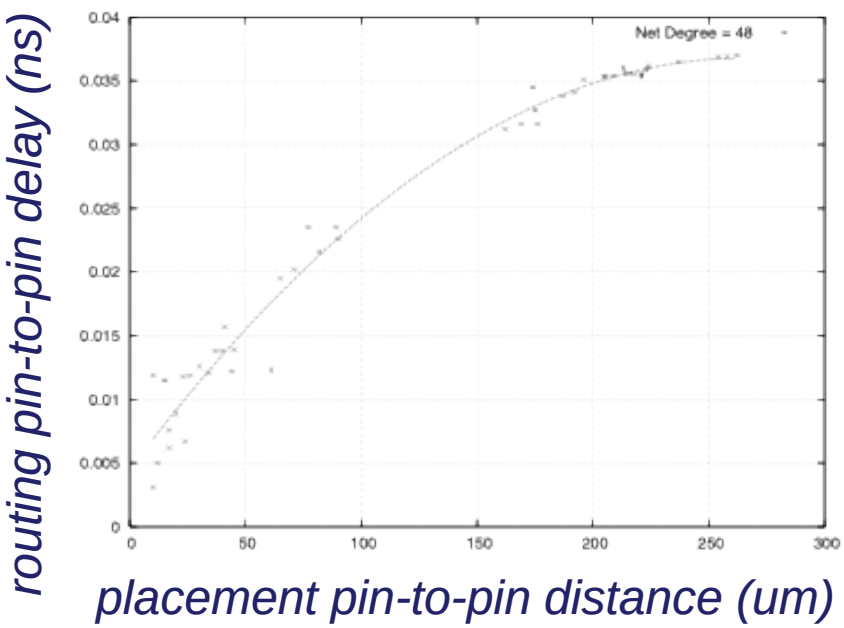
1. Delay Sampling (DS)

- Motivation: source-sink delays depend quadratically on the pin-pin placement length

net degree = 2

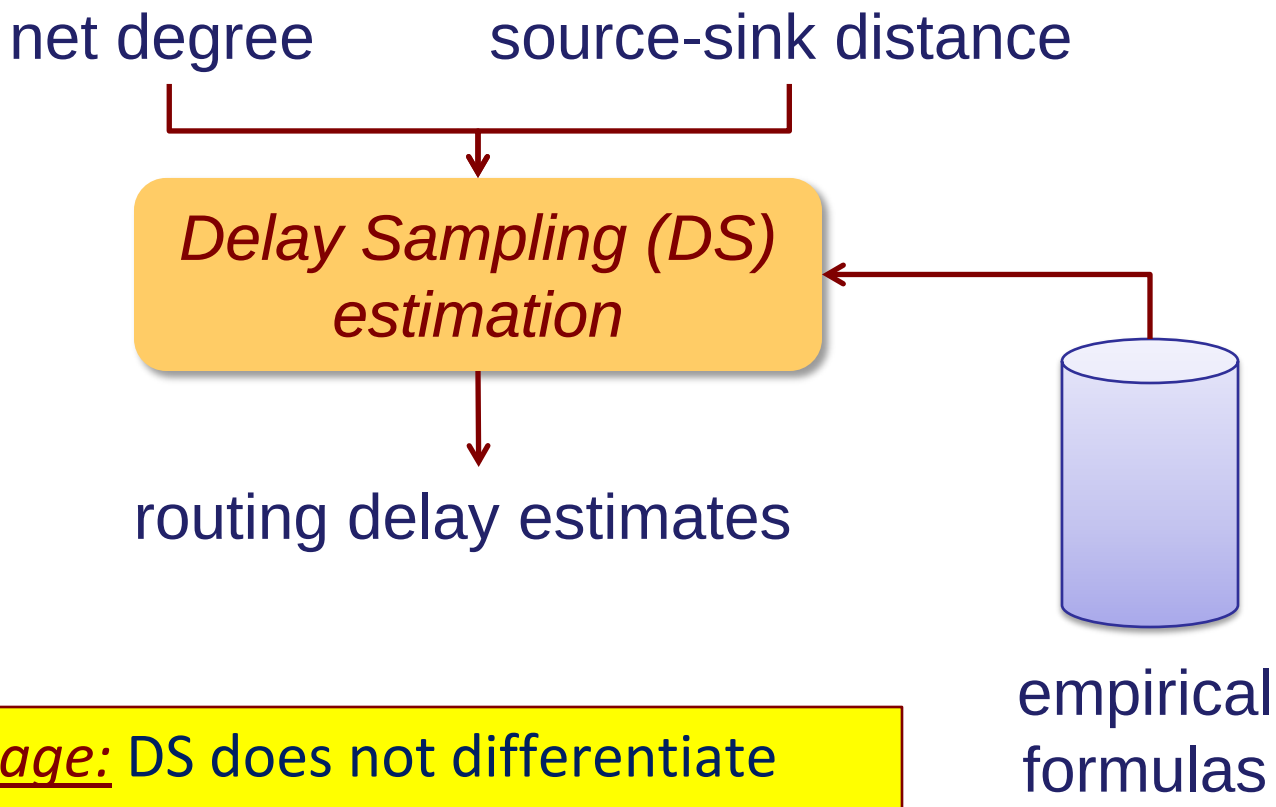


net degree = 48



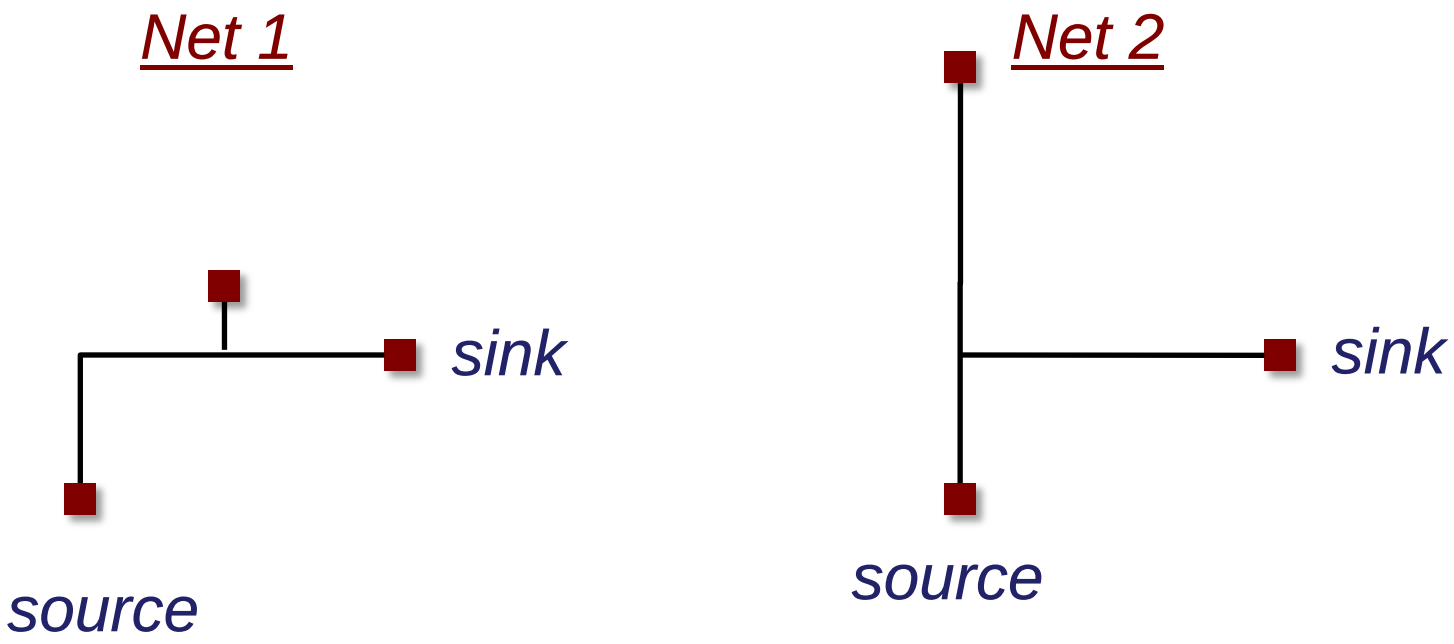
- Construct quadratic formulas in the pin-pin length where the coefficients depend on the net degree

1. Delay Sampling (DS)



Disadvantage: DS does not differentiate between two wires of the same length belong to nets with the same degree but different Steiner length.

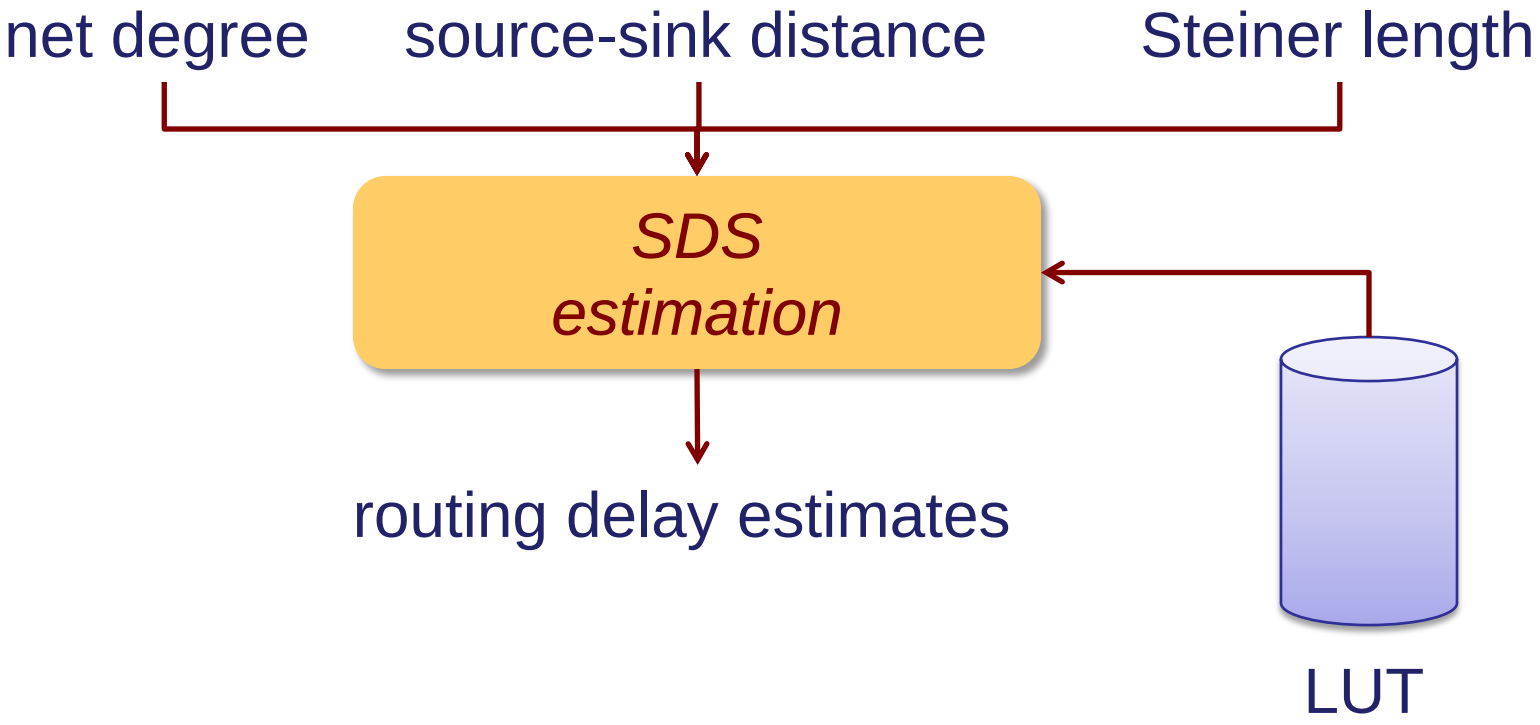
2. Steiner-Aware Delay Sampling (SDS)



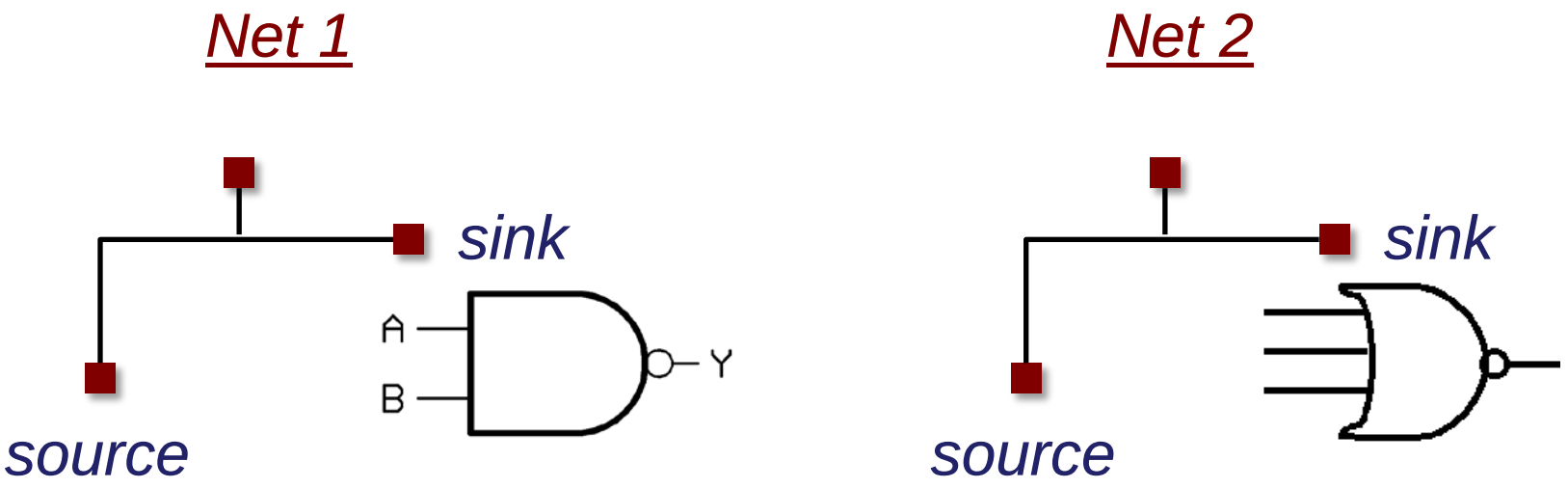
- Steiner-Aware Delay Sampling (SDS) technique improves over Delay Sampling by incorporating a net's total wire length into its post-route pin-to-pin delay estimations.

2. Steiner-Aware Delay Sampling (SDS)

- Using a base design(s), sample the delay for each pin-to-pin wire, group and then average the delays according to net degree, pin-to-pin distance, and the Steiner-tree wirelength.



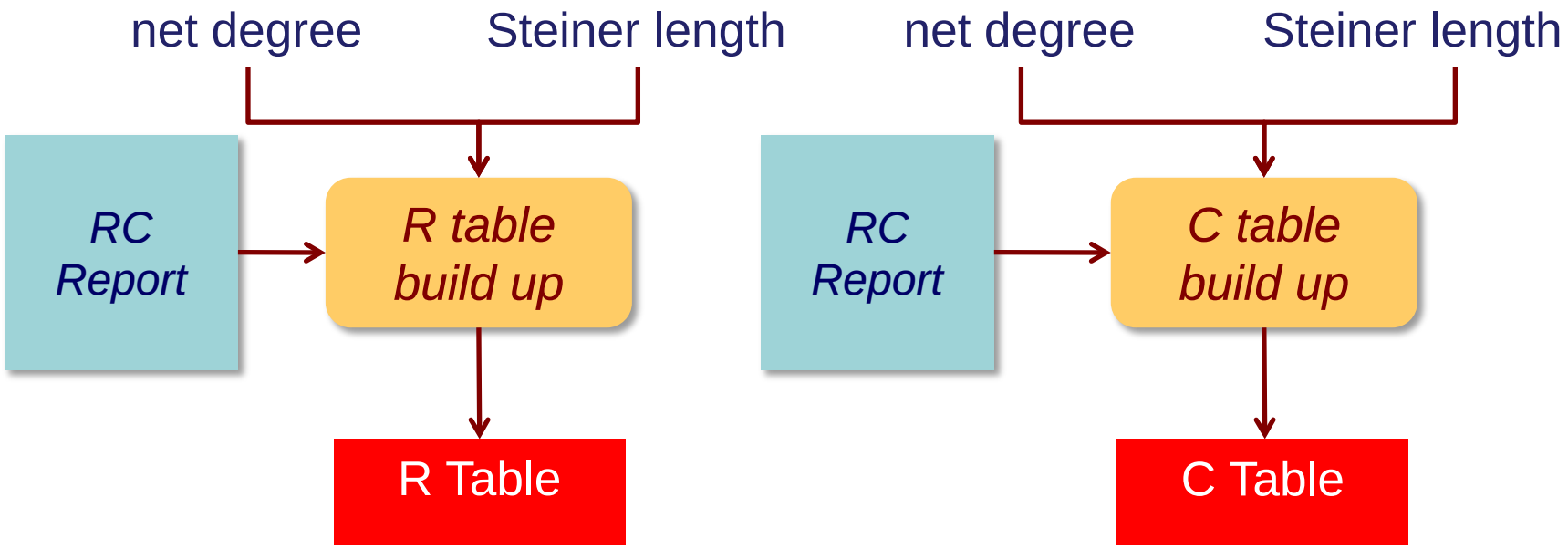
3. Steiner-Aware RC Sampling (SRCS)



The sink pin capacitance could be an important factor that differentiate wire delays

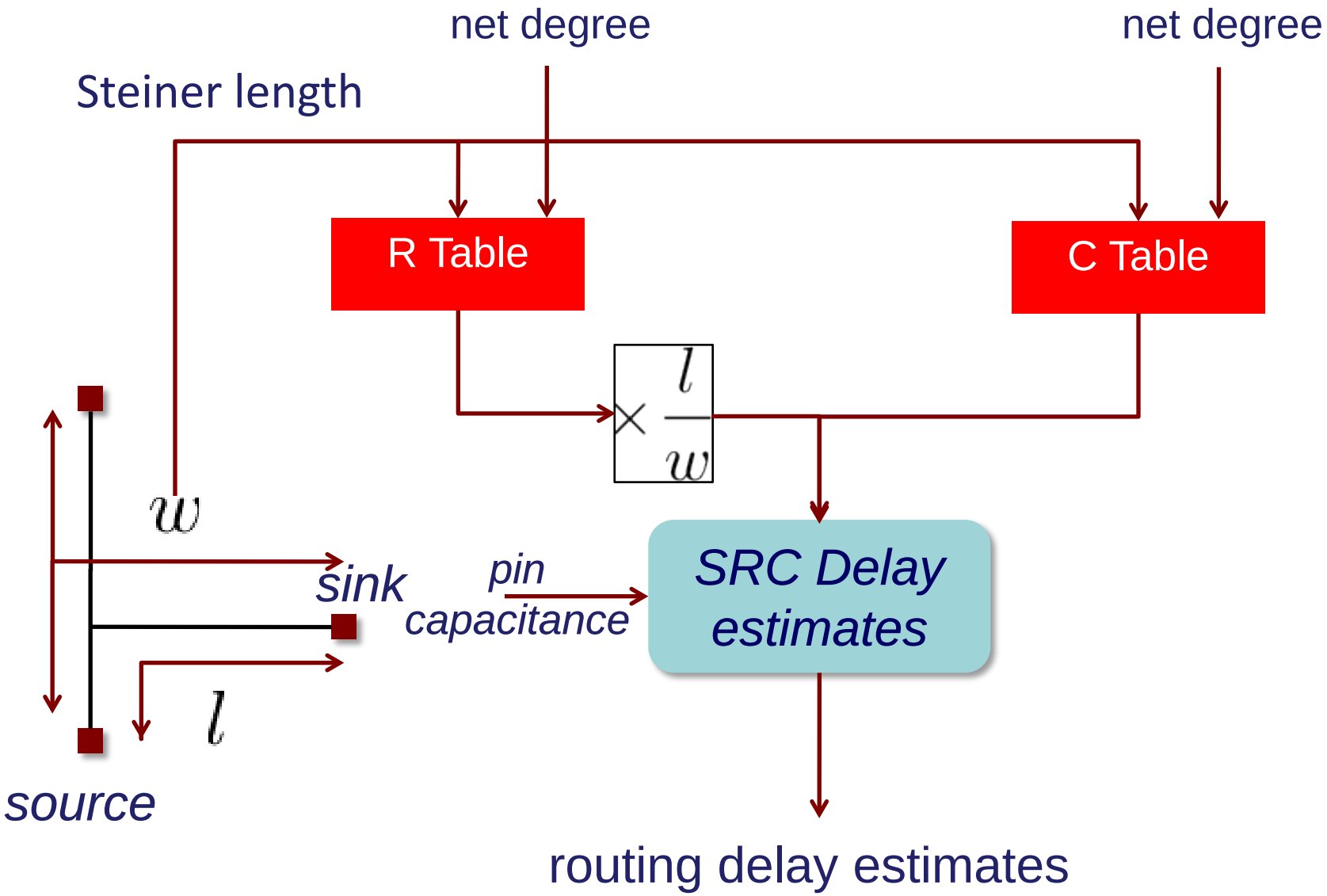
- To incorporate sink pin capacitance, it is necessary to estimate wire resistance and capacitance separately and then combine appropriate to estimate the wire delay

3. Steiner-Aware RC Sampling (SRCS): Table build-up



- Build resistance and capacitance LUTs that are function of net degree and Steiner lengtha

3. SRCS: Table lookup

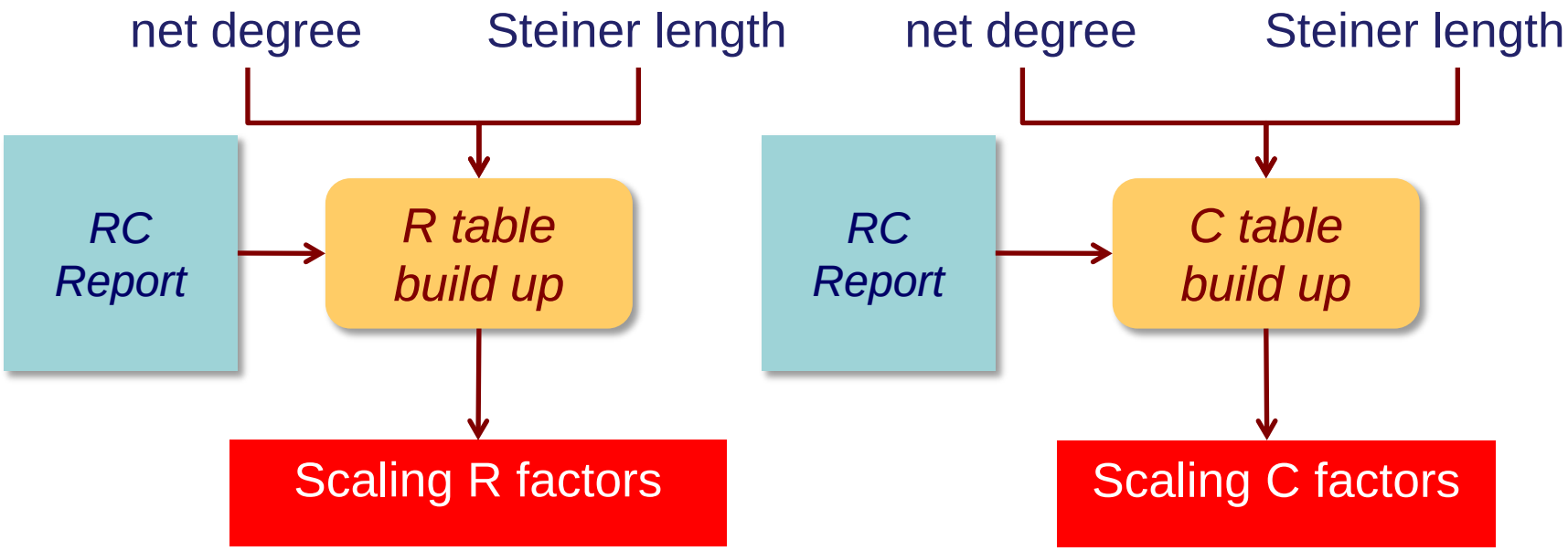


4. Scaled SRCS

- Motivation: What happens when a query does not match any of the entries in the LUTs?

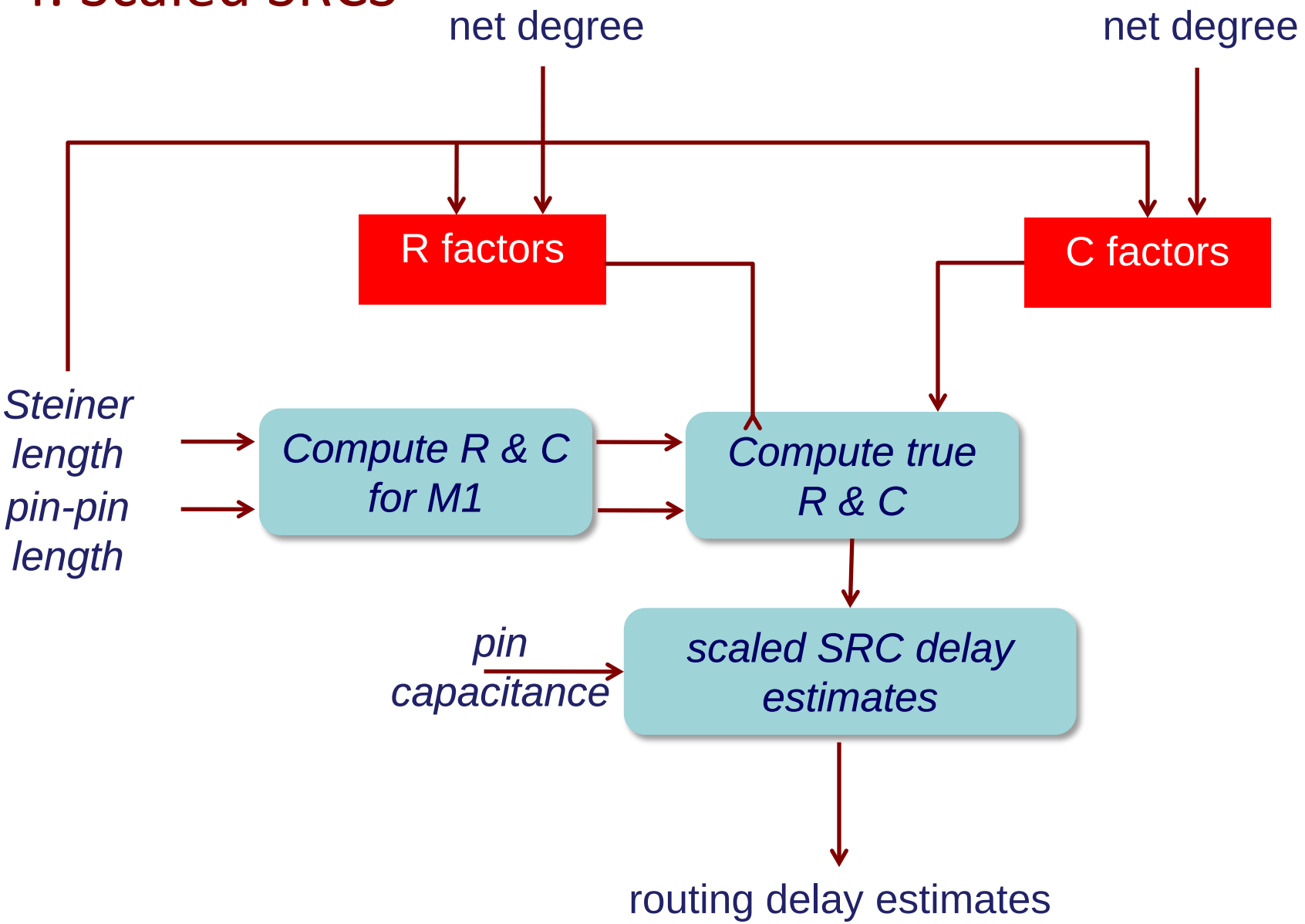
(4, 120) →

Net degree	Steiner tree	resistance
3	100	Ω_1
5	150	Ω_2



- The R & C scaling factor tables provide the necessary adjustment to convert an M1 R & C to the true R & C

4. Scaled SRCS



Experimental Setup

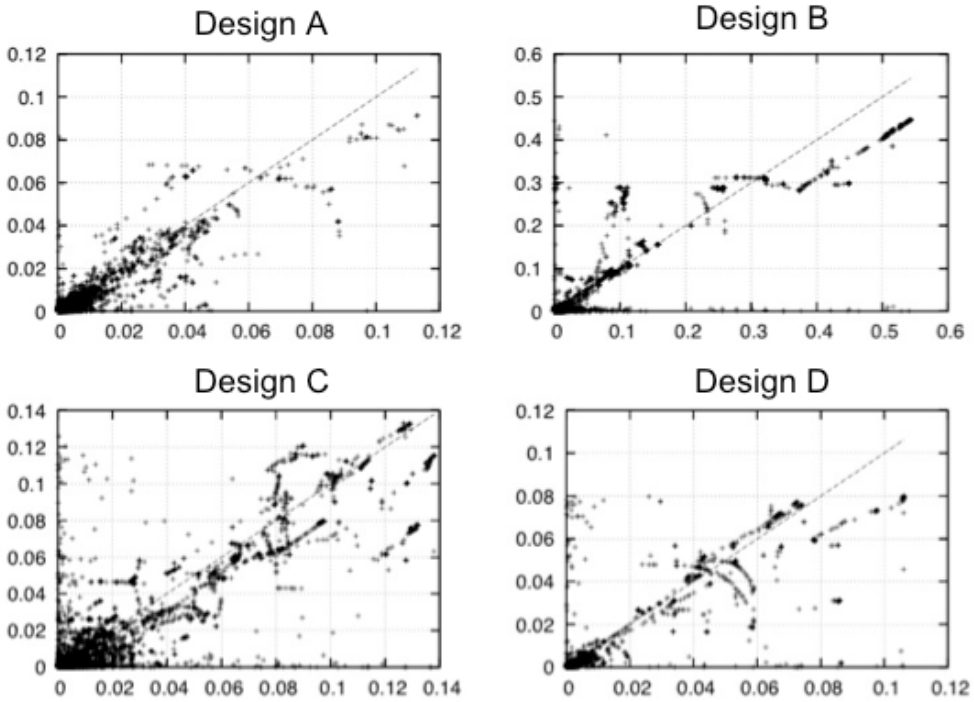
- Cadence Encounter v4.1 for placement, routing, and RC extraction
- Industrial 90 nm technology library
- Four benchmarks:

Circuit	#nets	#cells	Core area (um^2)
A (des)	27478	27104	285861
B (aes cipher)	15880	15265	160769
C (s38417)	8558	8529	69713
D (s13207)	2302	2240	21895

$$\text{estimation error} = \left| \frac{\text{estimated delay} - \text{routing delay}}{\text{routing delay}} \right|$$

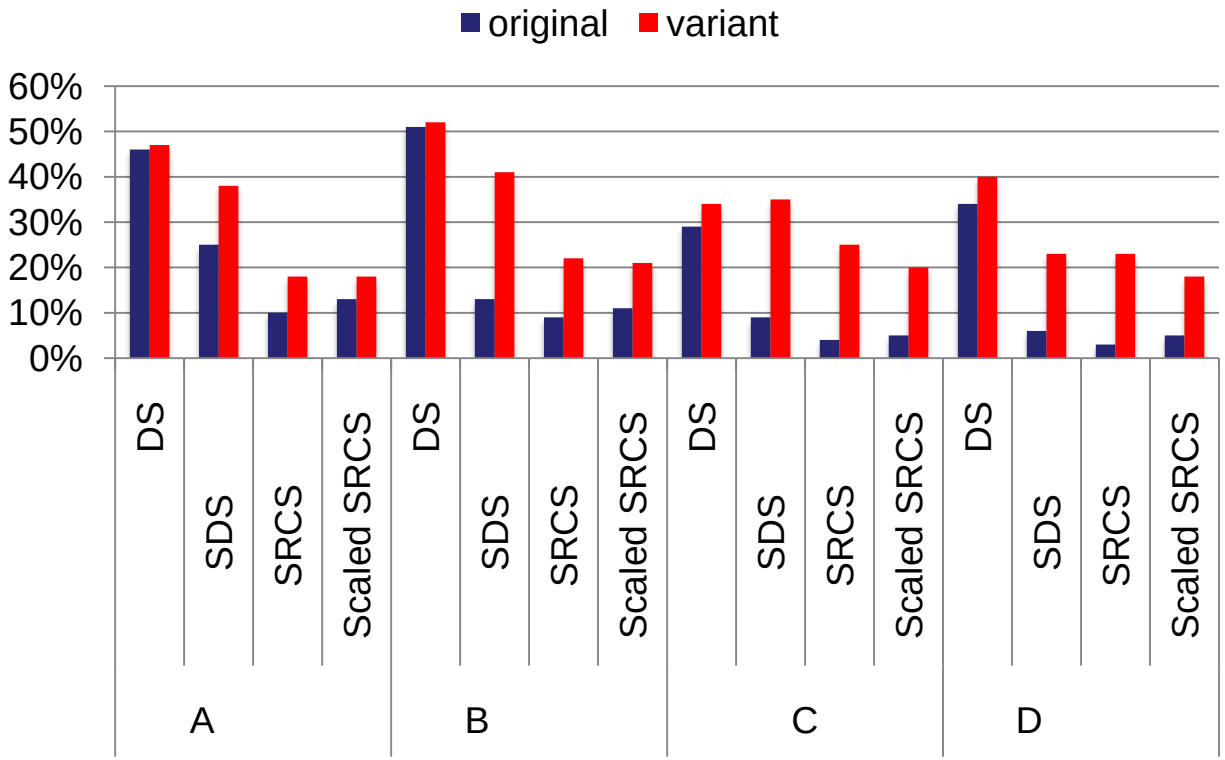
1. Estimator Stability

- Objective: estimate the stability of our estimators against design variants
- Variants are created by introducing blockages in the metal layers



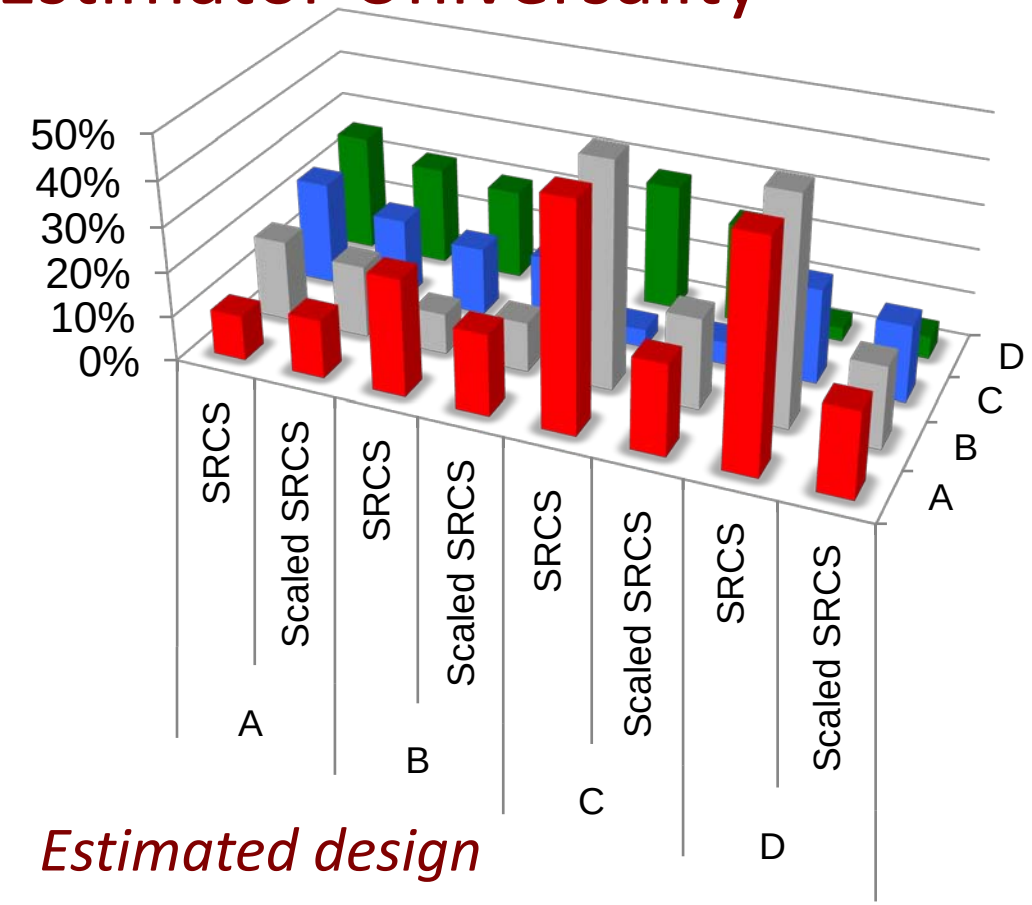
Post-routing delay (ns) before and after variations

Stability Comparison of estimation techniques



- SRCS is best on the original design
- Scaled SCRS is best on the variant with an average estimation error ofabout 22% from the routing delay
- The relative estimation error of techniques is consistent with their capabilities

2. Estimator Universality



Estimated design

design used to build LUT

- SRCS and scaled SCRS provide delay estimations with an average error of 31% and 16%
- Design A (biggest design) is best used for LUT buildup

Conclusions and future work

Conclusions:

- Provide a variety of techniques to handle delay estimation. Scaled Steiner RC sampling give very good delay estimations (16%) error.
- All techniques are based on lookup tables that are indexed by information available after placement.
- Techniques simple and they work

Future Work:

- Estimate the delay of critical paths
- Utilize the results of a fast global router to further improve the delay estimates
- Use in a design house or CAD tool where the LUTs are continuously improved as populated by routing results data

Thank You for your Attention

Summary of techniques

Inputs need to build LUTs:

	net degree	route length	net delay	route steiner tree length	resistance	capacitance
DS	x	x	x			
SDS	x	x	x	x		
SRCS	x			x	x	x
Scaled SRCS	x	x		x	x	x

Inputs need to query LUTs and estimate delay:

	net degree	placement length	placement steiner tree length	C_sink
DS	x	x		
SDS	x	x	x	
SRCS	x	x	x	x
Scaled SRCS	x	x	x	x