SLIP 2012 Technical Program

June 3rd, 2012. Co-located with DAC in Moscone Center, San Francisco, CA

Breakfast 8:00am-8:30am

Welcome Message + Keynote Speech 8:30am-9:30am

Heterogeneity and Interconnect
Ganapati Srinivasa, Intel Corp.

Coffee Break 9:30am-9:45am

Session I: Interconnect Technologies 9:45am-11:10am

Chair: Tan Yan, Synopsys Inc.

(Invited Talk) Interconnect Scaling into Sub-10nm Regime
Xiangyu Chen, Jiale Liang and H.-S. Philip Wong, Stanford University
9:45am-10:15am

Impact of Lithography Retargeting Process on Low Level Interconnect in 20nm Technology
Hongbo Zhang*, Yunfei Deng+, Jongwook Kye+ and Martin D. F. Wong*
* Univ of Illinois at Urbana-Champaign, + GlobalFoundries Inc.
10:15am-10:35am

An On-Chip Global Broadcast Network Design with Equalized Transmission Lines in the 1024-Core Era
Guang Sun*, Shih-Hung Weng+, Chung-Kuan Cheng+, Bill Lin+ and Lieguang Zeng*
* Tsinghua University, + Univ. of California at San Diego
10:35am-10:55am

Discussion Panel
Panelists: David Pan (Univ. of Texas at Austin), Sourav Chakravarty (Intel)
10:55am-11:10am

Coffee Break 11:10 am-11:25am

Embedded Tutorial 11:25am-12:15am

Chair: Marcelo Johann, Universidade Federal do Rio Grande do Sul (UFRGS)

Design and Optimization of Communication Fabrics: An Industrial Perspective
Umit Ogras and Michael Kishinevsky, Intel Corp.

Lunch 12:15am-1:30pm

Special Session: Smart Grids 1:30pm-3pm

Chair: Sung Kyu Lim, Georgia Tech

(Invited Talk) Towards the power networks of the future: needs, challenges and tools
Mario Paolone, École Polytechnique Fédérale de Lausanne (EPFL)
1:30pm-2:00pm

Panel: Smart Grids Technologies: Applications for the Future Electrical Infrastructure
Moderator: Mario Paolone, École Polytechnique Fédérale de Lausanne (EPFL)
Panelists: Mohammad Shahidehpour, Illinois Institute of Technology
Carlo Alberto Nucci, Univ. of Bologna, Italy
Owen Golden, National Instruments
2:00pm-3:00pm

Poster Session + Coffee Break 3:00pm-3:30pm

A Heuristic Method for Obstacle Avoiding Group Steiner Tree Construction
Tuhina Samanta*, Raka Sardar*, Hafizur Rahaman*, Parthasarathi Dasgupta+ and Bhargab B. Bhattacharya+
* Bengal Engineering and Science University, India, + Indian Institute of Management, India

A Locality-Aware Bi-level Mesh-Mesh 2D-NoC Architecture for Furture Thousand Core CMPs
Ankit More, Swetha George and Baris Taskin, Drexel University

Analysis of Post-Placement Length Estimation
Yangyang Li*, Amin Farshidi*, Laleh Behjat* and William Swartz+
* University of Calgary, Canada, + InternetCAD.com, Inc.

Session II: NoC and Wireless Network Optimization 3:30pm-5:15pm

Chair: Paul Bogdan, Carnegie Mellon University

Energy-Guided Exploration of On-Chip Network Design for Exa-Scale Computing
Umit Y. Ogras*, Yunus Emre+, Jianping Xu*, Timothy Kam* and Michael Kishinevsky*
* Intel Corp., + Arizona State University
3:30pm-3:50pm

Optimizing Heterogeneous NoC Design
Yaniv Ben Itzhak, Israel Cidon and Avinoam Kolodny, Technion – Israel Institute of Technology
3:50pm-4:10pm

Handling Global Traffic in Future CMP NoCs
Ran Manevich, Israel Cidon and Avinoam Kolodny, Technion – Israel Institute of Technology
4:10pm-4:30pm

Improving Broadcast Efficiency in Wireless Sensor Network Time Sycnchronization Protocols
Wenxun Huang*, Yujuan Quan+, and Deming Chen*
* Univ. of Illinois at Urbana-Champaign, + Jinan University, China
4:30pm-4:50pm

Discussion Panel
Panelists: Dirk Stroobandt (Ghent University), Paul Gratz (Texas A&M Univ.), Janet Wang (Univ. of Arizona at Tucson)
4:50pm-5:15pm

Evening Banquet 6:30pm-9:00pm