FINAL PROGRAM

SLIP 2016 Technical Program
June 4, 2016 Saturday
Co-Located with DAC in Austin
www.sliponline.org

Opening Remarks (9:30am-9:45am)
Baris Taskin, Drexel University, General Chair
Tsung-Yi Ho, National Tsing Hua University, Technical Program Chair

Session I: Brain-Inspired Computing (9:45am-10:55am)
Session Chair: Tsung-Yi Ho, National Tsing Hua University

9:45am-10:15am
(Invited) "Hardware Design in Brain Inspired Computing Research"
Yu Wang, Tsinghua University

10:15am-10:35am
"Spin-Hall Assisted STT-RAM Design and Discussion"
Enes Eken, Ismail Bayram, Yajun Zhang, Bonan Yan, Wenqing Wu, Helen Li and Yiran Chen
University of Pittsburgh

10:35am-10:55am
"Connectivity Effects on Energy and Area for Neuromorphic System with High Speed Asynchronous Pulse Mode Links"
Carrie Segal, Aditya Dalakoti, Forrest Brewer and Merritt Miller
UC Santa Barbara

Break (10:55am-11:10am)

Session II: 3D IC (11:10am-11:50pm)
Session Chair: Ioannis Savidis, Drexel University

11:10am-11:30am
"Revisiting 3DIC Benefit with Multiple Tiers"
Wei-Ting J. Chan, Andrew B. Kahng and Jiajia Li
UC San Diego

11:30am-11:50am
"Buffered Interconnects in 3D IC Layout Design"
Mohammad Ahmed, Sucheta Mohapatra and Malgorzata Chrzanowska-Jeske
Portland State University

Lunch (12:00pm-1:30pm)

Keynote (1:30pm-2:30pm)
"Beyond Charge Based Computing"
Kaushik Roy
Purdue University

Panel (2:30pm-3:30pm)
Hardware Security: Is it a Myth or Reality?

Chair: Swaroop Ghosh, University of South Florida

Saverio Fazzari, Booz Allen Hamilton
Swarup Bhunia, Univ. of Florida
Sriram Chellappan, Univ. of South Florida
TBD

Break (3:30pm-3:40pm)

Session III: NoC (3:40pm-4:50pm)
Session Chair: Paul Graz, Texas A&M University

3:40pm-4:10pm
(Invited) "NoC Resource Allocation: Design-Time and Runtime Techniques"
Jiang Hu
Texas A&M University

4:10pm-4:30pm
"A Demand-Aware Predictive Dynamic Bandwidth Allocation Mechanism for Wireless Network-on-Chip"
Naseef Mansoor, Md Shahriar Shamim and Amlan Ganguly
Rochester Institute of Technology

4:30pm-4:50pm
"A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects"
Ishan Thakkar, Sai Vineel Reddy Chittamuru and Sudeep Pasricha
Colorado State University

Session IV: Physical Design (4:50pm-5:30pm)
Session Chair: Chengmo Yang, University of Delaware

4:50pm-5:10pm
"Latch Clustering for Minimizing Detection-to-Boosting Latency Toward Low-Power Resilient Circuits"
Chih-Cheng Hsu[a], Mark Po-Hung Lin[a] and Masanori Hashimoto[b]
National Chung Cheng University[a], Osaka University[b]

5:10pm-5:30pm
“Tologically-Geometric Routing”
Roman Bazylevych[ab], Marek Pałasiński[b] and Lubov Bazylevych[c]
Lviv Polytechnic National University[a], University of Information Technology and Management in Rzeszow[b], Institute of Applied Problems of Mechanics and Mathematics NASU[c]

Closing Remarks and Awards Presentation (5:30pm-5:40pm)