FINAL PROGRAM

SLIP 2017 Technical Program
June 17, 2016 Saturday
Co-Located with DAC in Austin
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Opening Remarks (9:00am-9:10am)
Tsung-Yi Ho, National Tsing Hua University, General Chair
Shiyan Hu, Michigan Technological University, Technical Program Chair

Session I: Routing(9:10am-10:10am)
Session Chair: Tsung-Yi Ho, National Tsing Hua University

9:10am-9:40am
"Analyzing Voltage Bias and Temperature Induced Aging Effects in Photonic Interconnects for Manycore Computing"
Sai Vineel Reddy Chittamuru, Ishan Thakkar and Sudeep Pasricha
Colorado State University

9:40am-10:10am
"Reconfigurable Topology Synthesis for Application-Specific NoC on Partially Dynamically Reconfigurable FPGAs"
Jinglei Huang, Xiaodong Xu, Lan Yao and Song Chen
USTC

Break (10:10am-10:20am)

Session II: (10:20am-12:00pm)
Session Chair: Shiyan Hu, Michigan Technological University

Keynote Talk 10:20am-11:20am
"Frontiers of Timing"
UlfSchlichtmann
Technical University of Munich

Invited Talk11:20am-12:00am
"Making Automobile Safe and Smart by Design Automation"
Xin Li
Duke University

Lunch (12:00pm-1:30pm)

Panel: Neuromorphic Computing and Deep Learning (1:30pm-2:30pm)
Panel Chair: Yanzhi Wang, Syracuse University
Panelists:

Yanzhi Wang, Syracuse University
Bo Yuan, City University of New York
Amit Trivedi, University of Illinois at Chicago
Pierre-Emmanuel Gallardon, University of Utah
Deliang Fan, University of Central Florida
Jae-Sun Seo, Arizona State University

Break (2:30pm-2:40pm)

Session III:DFM and Routing (2:40pm-4:20pm)
Session Chair: Chengmo Yang, University of Delaware

Invited Talk 2:40pm-3:20pm
"Toward Unidirectional Routing Closure in Extreme Scaling"
David Pan and Xiaoqing Xu
University of Texas at Austin, ARM Research

3:20pm-3:50pm
"Timing Driven Routing Tree Construction"
PeishanTu, Wing-Kai Chow and Evangeline Young
Chinese University of Hong Kong

3:50pm-4:20pm
"Fence-aware Detailed-routability Driven Placement"
Wing-Kai Chow, Jian Kuang, PeishanTu and Evangeline F. Y. Young
Chinese University of Hong Kong

Session IV: Clocking (4:20pm-5:50pm)
Session Chair: Xiaoqing Shi, ARM Research

4:20pm-4:50pm
"Clock Tree Synthesis for Heterogeneous 3-D ICs"
IsuruDaulagala and IoannisSavidis
Drexel University

4:50pm-5:20pm
"A Charge Recovery Logic System Bus"
Leo Filippini and BarisTaskin
Drexel University

5:20pm-5:50pm
"Slew-Down: Analysis of Slew Relaxation for Low-Impact Clock Buffers"
Scott Lerner, Eric Leggett and BarisTaskin
Drexel University

Closing Remarks and Awards Presentation (5:50pm)