SLIP 2018 FINAL PROGRAM

June 23, 2018 Saturday
Co-Located with DAC in San Francisco
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Opening Remarks (9:00am-9:10am)
Chengmo Yang, University of Delaware, Technical Program Co-Chair

Keynote Talk (9:10am-10:10am)
“Big Data Analytics: Practices and Applications”
Xin Li
Duke University

Break (10:10am-10:20am)

Session I (10:20am-11:50am)
Session Chair: Bei Yu, The Chinese University of Hong Kong

10:20am-10:50am
“Resource and Data Optimization for Hardware Implementation of Deep Neural Networks Targeting FPGA-based Edge Devices”
Xinheng Liu, Dae Hee Kim, Chang Wu and Deming Chen
University of Illinois

10:50am-11:20am
“A Study of Optimal Cost-Skew Tradeoff and Remaining Suboptimality in Interconnect Tree Constructions”
Kwangsoo Han, Andrew B. Kahng and Christopher Moyes
University of California San Diego

11:20am-11:50am
“A Design Framework for Processing-In-Memory Accelerator”
Di Gao and Cheng Zhuo
Zhejiang University

Lunch (11:50am-1:30pm)

Session II: (1:30pm-3:00pm)
Session Chair: Yanzhi Wang, Northeastern University

1:30pm-2:00pm
"Fast and Precise Routability Analysis with Conditional Design Rules"
Ilgweon Kang, Dongwon Park, Changho Han and Chung-Kuan Cheng
University of California San Diego

2:00pm-2:30pm
"Adaptive Sensitivity Analysis with Nonlinear Power Load Modeling"
Po-Ya Hsu, Chun-Han Yao and Chung-Kuan Cheng
University of California San Diego

2:30pm-3:00pm
"Exploiting PDN Noise to Thwart Correlation Power Analysis Attacks in 3D ICs"
Jaya Dofe and Qiaoyan Yu
University of New Hampshire

Break (3:00pm-3:10pm)

Panel: Emerging Trends in On-chip Power Delivery and Management (3:10pm-4:10pm)
Panel Chair: Selcuk Kose, University of South Florida
Panelists:
Inna Partin-Vaisband, University of Illinois at Chicago
Pingqiang Zhou, Shanghai Tech
Rahul Limaye, Intel
Corporation Arijit Raychowdhury, Georgia Tech

Closing Remarks(4:10pm-4:15pm)
Chengmo Yang, University of Delaware, Technical Program Co-Chair

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