FINAL PROGRAM

SLIP 2019 Technical Program
June 2, 2019 Sunday
Co-Located with DAC in San Francisco
www.sliponline.org

08:45 - 09:00 - Opening Remarks

09:00 - 09:45 – Keynote: *"Challenges for the Next Decade of SLIP"*

Speaker: Andrew B. Kahng, CSE and ECE Departments, UC San Diego
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Speaker Bio: Andrew B. Kahng is Professor of CSE and ECE and holder of the endowed chair in high-performance computing at UC San Diego. He was visiting scientist at Cadence

(1995-97) and founder/CTO at Blaze DFM (2004-06). He is coauthor of 3 books and over 400 journal and conference papers, holds 34 issued U.S. patents, and is a fellow of ACM and IEEE. He served as general chair of DAC, ISPD and other conferences, and from 2000-2016 as international chair/co-chair of the ITRS Design and System Drivers working groups. He is currently PI of "OpenROAD", an $11.3M U.S. DARPA project targeting open-source, autonomous ("no humans") tools for IC implementation. With Dirk Stroobandt, he co-founded SLIP in 1999.

Abstract: Today, 20 years after the first SLIP, challenges of interconnect prediction are more dominant, wide-ranging, and critical to solve than ever before.
(1) To achieve "equivalent scaling" from design cost and schedule reduction, there is now tremendous focus on the use of machine learning "inside and around" the design process. Here, uncertainties of interconnect prediction cause bottlenecks and expensive loops at every step of design: partitioning, floorplanning, power delivery, routability, crosstalk / voltage drop, performance estimation, etc.

(2) How to supply, interconnect, and synchronize devices with best-possible PPAC (power, performance, area, cost) is the central question of DTCO (design-technology co-optimization). The nature and orchestration of middle-of-line and back-end-of-line interconnect technologies dominate today's DTCO analyses and decision-making.

(3) As the industry continues to scale product value, myriad "More than Moore" and "Beyond X" (X = Moore, CMOS, von Neumann, …) possibilities demand new "pathfinding" technology and methodology, so that system architecture, partitioning and integration can identify best paths forward, as well as necessary design enablements, with sufficient certainty and lead times. This has always been a central task of SLIP.

In its 20-year history, the SLIP workshop has illuminated many ideas that remain highly relevant to the above challenges. This talk will describe how the need for SLIP is greater than ever. The question is: How will the SLIP community respond?
09:45 - 10:00 - Q&A
10:00 - 10:15 - Coffee Break
10:15 - 11:35 - Technical Session I: *"Secure Networks and Circuits"*
• Security Network On-Chip for Mitigating Side-Channel Attacks • FSNoC: Safe Network-on-Chip Design with Packet Level Lock Stepping • Bus-Invert Coding as a Low-Power Countermeasure Against Correlation Power Analysis Attack • A Novel PUF Architecture Against Non-Invasive Attacks
11:35 - 12:35 - Panel I: *"The future for interconnect planning and prediction"*
Panelists: Shantanu Dutt, David Pan, Paul Franzon, Gregory M Schaeffer
12:35 - 01:40 - Lunch
01:40 - 03:00 - Technical Session II: *"System Design: On-chip and Beyond"*
• Communication Considerations for Silicon Interconnect Fabric • Investigation of Cost-Optimal Network-on-Chip for Passive and Active Interposer Systems • Distributed Digital Low-Dropout Regulators with Phase Interleaving for On-Chip Voltage Noise Mitigation • An Analytical Approach for Time-Division Multiplexing Optimization in Multi-FPGA based Systems
03:00 - 03:15 - Coffee Break
03:15 - 04:00 - Invited Talk
Title: Brain-inspired Circuits and Systems for Ubiquitous Intelligence **Speaker:** Arijit Raychowdhury
04:00 - 04:45 - Panel II: *"Computer Aided Design for Superconducting Electronics"*
Panelists: Yanzhi Wang, Tsung-Yi Ho, Olivia Chen, Naveen Katam, Deliang Fan
04:45 - 05:00 - Closing Remarks