PROGRAM

Time (Pacific Time)	Program
8:30	Welcome, Program Overview, Housekeeping, Keynote Introduction
8:40	**Keynote Session 1 — Outlook of device and assembly technologies enabling high-performance mobile computing** (abstract) Mustafa Badaroglu *(Qualcomm, Belgium)*
9:20	Q&A
9:35	Break
9:45	**Paper Session 1 — Interconnect Aspects of Advanced Technologies and Applications** (3 x 20 min.) Session Chair: Brian Cline *(ARM, USA)* ◦ Communication architecture enabling 100X accelerated simulation of biological neural networks Kevin Kauth, Tim Stadtmann, Ruben Brandhofer, Vida Sobhani and Tobias Gemmeke *(IDS, RWTH Aachen University, Germany)* ◦ Pathfinding for 2.5D interconnect technologies Saptadeep Pal and Puneet Gupta *(UCLA, USA)* ◦ Global interconnects in VLSI complexity SFQ systems Tahereh Jabbari and Eby Friedman *(University of Rochester, USA)*
10:45	Discussants + Q&A • Louis Scheffer *(HHMI, USA)* • Sung-Kyu Lim *(Georgia Tech, USA)*
11:00	**Invited Session 1 — Quantum Computing** (2 x 25 min.) Session Chair: Rasit O. Topaloglu (IBM, USA) ◦ Building a quantum computer Barry C. Sanders *(University of Calgary, Canada)* ◦ Extending quantum systems with optical interconnects Jason Orcutt *(IBM, USA)*
11:50	Discussants + Q&A • Koen Bertels *(QBee, Portugal & University of Porto, Portugal)*
12:00	Break / Open Discussion — Problems and Pathfinding Challenges
12:30	**Keynote Session 2 — Wafer scale interconnect and pathfinding for machine learning hardware** (abstract) Patrick Groeneveld *(Cerebras Systems, USA)*
13:10	Q&A
13:25	**Invited Session 2 — NoCs** (2 x 25 min.) Session Chair: Dirk Stroobandt *(Ghent University, Belgium)* ◦ Analytical modeling of NoCs for fast simulation and design exploration Raid Ayoub *(Intel, USA)* ◦ Role of on-chip networks in building domain-specific architectures (DSAs) for sparse computations Abhishek Jain *(Xilinx, USA)*
14:15	Discussants + Q&A • Henri Fraisse *(Xilinx, USA)* • Paolo D'Alberto *(Xilinx, USA)*
14:25	Break
14:35	**Paper Session 2 — Interconnect Prediction, Analysis and Optimization** (3 x 20 min.) Session Chair: Mahesh Iyer *(Intel, USA)* ◦ Revisiting inherent noise floors for interconnect prediction Tuck-Boon Chan *(Qualcomm, USA)*, Andrew B. Kahng *(UCSD, USA)* and Mingyu Woo *(UCSD, USA)* ◦ 3D NoC emulation model on a single FPGA Jonathan D'hoore *(Ghent University, Belgium)*, Poona Bahrebar *(UC Irvine, USA & Ghent University, Belgium)* and Dirk Stroobandt *(Ghent University, Belgium)* ◦ Optimal bounded-skew Steiner trees to minimize maximum k-active dynamic power Hamed Fatemi *(NXP Semiconductors, USA)*, Andrew B. Kahng *(UCSD, USA)*, Minsoo Kim *(UCSD, USA)* and Jose Pineda de Gyvez *(NXP Semiconductors, USA)*
15:35	Discussants + Q&A • Patrick Groeneveld *(Cerebras Systems, USA)* • Rob Aitken *(ARM, USA)*
15:50	Workshop Closing — Future directions/Community mechanisms