23rd ACM/IEEE International Workshop on System-level Interconnect Pathfinding (SLIP)

Co-hosted with ACM/IEEE Intl. Conf. on Computer-Aided Design (ICCAD)

November 4, 2021
Virtual Event

Accepted papers are published in IEEE/ACM proceedings.

GENERAL INFORMATION

The 2021 ACM/IEEE International Workshop on System-Level Interconnect Pathfinding (SLIP) is the 23rd edition of the Workshop.

SLIP, co-hosted with ICCAD 2021, will bring together researchers and practitioners who have a shared interest in the challenges and futures of system-level interconnect, coming from wide-ranging backgrounds that span system, application, design and technology.

The technical goal of the workshop is to

1. identify fundamental problems, and,
2. foster new pathfinding of design, analysis, and optimization of system-level interconnects with emphasis on system-level interconnect modeling and pathfinding, DTCO-enhanced interconnect fabrics, memory and processor communication links, novel dataflow mapping for machine learning, 2.5/3D architectures, and new fabrics for the beyond-Moore era.

Original submissions in the form of regular technical papers, invited sessions (tutorials, panels, special-topic sessions), workshop discussion topics, and posters are welcome. Program content is accepted based on novelty and contributions to the advancement of the field. Accepted technical papers will be published in the ACM and IEEE digital libraries.

PROGRAM

Time (Pacific Time)	Program
6:00	**General Chair Message — Welcome Message & Opening Remarks** (15 min.) Mustafa Badaroglu *(Qualcomm, Belgium)*
6:15 7:30	**Session 1 — System Technology Co-Optimization for Advanced Physical Design** (3 x 25 min.) Session Chairs: Yuzo Fukuzaki *(TechInsights, Canada)* & Ivan Ciofi *(imec, Belgium)* - A novel system-level physics-based electromigration modelling framework; Application to the power delivery network Houman Zahedmanesh[1], Ivan Ciofi[1], Odysseas Zografos[1], Mustafa Badaroglu[2], and Kristof Croes[1] *[1]imec, Belgium [2]Qualcomm, Belgium* - Design and system technology co-optimization sensitivity prediction for VLSI technology development using machine learning Chung-Kuan Cheng, Chia-Tung Ho, Chester Holtz, and Bill Lin *University of California, San Diego, USA* - Enabling chiplet integration beyond 7nm (Invited Talk) Suresh Ramalingam *Xilinx Inc., USA* Q&A (10 min.)
7:40 8:55	**Session 2 — 3D EDA and Security** (3 x 25 min.) Session Chairs: Shantanu Dutt *(University of Illinois at Chicago, USA)* & Seungwon Kim *(University of California, San Diego, USA)* - Design and sign-off methodologies for wafer-to-wafer bonded 3D-ICs at advanced nodes (Invited) Giuliano Sisto[1], Rongmei Chen[2], Richard Chou[1], Geert Van der Plas[2], Eric Beyne[2], Rod Metcalfe[1] and Dragomir Milojevic[2] *[1]Cadence Design Systems, USA [2]imec, Belgium* - Chip stacking and packaging technology explorations for hardware security (Invited Talk) Makoto Nagata *Kobe University, Japan* - Performance-aware interconnect delay insertion against EM side-channel attack Minmin Jiang and Vasilis Pavlidis *University of Manchester, UK* Q&A (10 min.)
9:05 9:45	**Keynote Address — Recent advances and future challenges in 2.5D/3D heterogeneous integration** (Abstract) Tanay Karnik *(Intel Corp., USA)* Session Chairs: Ismail Bustany *(Xilinx, USA)* & Brian Cline *(ARM, USA)* Q&A (10 min.)

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9:55	**Session 3 — Next Generation Optical Interconnects** (3 x 25 min.)
	Session Chairs: Dirk Stroobandt *(Ghent University, Belgium)* & Rasit Topaloglu *(IBM, USA)*
	- Reconfigurable on-chip wireless interconnections through optical phased arrays Giovanna Calò[1], Gaetano Bellanca[2], Davide Bertozzi[2], Marina Barbiroli[3], Franco Fuschini[3], Giovanni Serafino[4], Velio Tralli[2], and Vincenzo Petruzzelli[1] [1]*Polytechnic University of Bari, Italy* [2]*University of Ferrara, Italy* [3]*University of Bologna, Italy* [4]*TeCIP Institute, Italy*
	- Silicon photonics technology for terabit-scale optical I/O (Invited Talk) Joris Van Campenhout *imec, Belgium*
11:10	- Designing a multi-chiplet manycore system using the POPSTAR optical NoC architecture (Invited Talk) Yvain Thonnart *CEA-LIST, France*
	Q&A (10 min.)
11:20	**Session 4 — 3D Interconnects and Networks-on-Chips** (4 x 25 min.)
	Session Chairs: Pascal Vivet *(CEA, France)* & Poona Bahrebar *(Ghent University, Belgium)*
	- The open domain-specific architecture: An introduction (Invited Talk) Bapi Vinnakota *ODSA, USA*
	- SID-Mesh: Diagonal mesh topology for silicon interposer in 2.5D NoC with introducing a new routing algorithm Babak Sharifpour, Mohammad Sharifpour, and Midia Reshadi *Islamic Azad University, Iran*
	- RAMAN: Reinforcement learning inspired algorithm for mapping applications onto mesh Network-on-Chip Jitesh Choudhary[1], Soumya J[1], and Linga Reddy Cenkeramaddi[2] [1]*BITS Pilani, India* [2]*University of Agder, Norway*
13:05	- Network-on-Chips for future 3D stacked dies (Invited Talk) Tiago Mück *Arm, USA*
	Q&A (15 min.)
13:20	**General Chair Closing Remarks — Audience Poll & Closing Remarks** (10 min.)
	Mustafa Badaroglu *(Qualcomm, Belgium)*

Committee Members

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Mustafa Badaroglu *Qualcomm, Belgium*

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