Power and Area Estimation/Optimization in Behavioral Synthesis

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1 Problem Statement 1

In order to offer better design space exploration, the HLS tool must provide the designers a way to investigate diverse interconnection schemes. Little works reported on mixed bus and mux architectures. Cathedral-II [2] has a restricted bus-mux interconnection model, where interconnections inside EXU's are mux-based and global connections are bus-based. In general, mux-based interconnections are more efficient for resources with low sharing factors. Contrarily, designs that employs a large controller or a large interconnection set to enable high resource sharing factors give better results with bus-based interconnections [3]. However, like in Harvard architecture with contrast to Von Neuman architecture, maximum sharing of busses and functional units may not guarantee lower power solution. Thus, the problerm is to how to estimate power consumption due to switching activities related with both mux and bus.

2 Problem Statement 2

There are essentially two problems in HLS: 1. The cost of the solution is measured in the structural domain rather than in the physical domain. 2. Subdividing the synthesis problem results in sub-optimal solutions. Physical level information is becoming too important to be overlooked by high-level synthesis algorithms. For instance, datapath interconnection styles and related synthesis/evaluation are directly affected by the availability of several routing layers. Then, the problem is how to design the datapath considering layout styles.

3 Problem Statement 3

The circuit area can be estimated as follows. $S_T = \alpha(A_D + A_C)$, where S_T: critical area, A_D: data path cell area, A_C: controller cell area, α: routing area factor.
By experimentation from [3], the routing area factor is a constant factor of cell area. About 70% of the circuit area is due to interconnections (routing wires). However, the constant will depend on the datapath and architecture styles. There is also no good behavioral-level interconnection delay estimation yet.

4 Problem Statement 4

The communication synthesis algorithm builds a graph where each node represents a point-to-point connection. There will be an edge linking two nodes if the two associated connections will never be used simultaneously. After clique partitioning, one bus is allocated for each clique. This approach does not address switch minimization. One possibility for finding the optimal solution in terms of buses and switches is to use a dynamic programming approach. Even though, it remains an expensive solutions on very large designs. On large designs we need to use fast heuristics to evaluate each architectural possibility.

5 Problem Statement 5

The overall effect is to provide a global optimization of a cost function which is closely related to the physical cost of the solution. COBRA [1] target architecture and layout style eliminate global wiring in the final datapath. The datapath is partitioned into a number of communication processors each with functional units and local memory. Each processor is designed around a three bus consisting of two read buses and one write bus. Then the problem is to how to define the global bus in terms of power consumption and routing space.

References

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[3] P. Guillaume W.O. Cesario, P. Kission and A.A.Jerraya (TIMA Lab.). “Unified evaluation model for interconnection schemes used in behavioral synthesis”. *IWLAS’97, Grenoble, France*, Dec. 1997.