Can Fast Algorithms Be Used as Good Predictors?

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Placement is an important stage in VLSI design. Since the floorplanning/placement problem is NP-hard, as the complexity of VLSI design increases, even the best existing placement algorithm can not get the placement done in a short period. After the placement is done, the chip designer might learn that performance constraints/objectives are not met. Then, a lengthy iteration loop begins. A floorplan/placement predictor is extremely useful in speeding-up the iteration process.

Here, we contrast two classes of predictors: constructive and statistical. A constructive predictor is one that generates an exact or an approximate solution to a problem. A fast placement annealer or a global placer are examples of constructive predictors. A model that estimates the wirlength based on the properties of a given netlist is an example of a statistical predictor. Here, we focus on constructive predictors and open the discussion to how they differ from statistical models.

First, we will discuss a class of predictors based on fast and approximate algorithms. We will argue that fast floorplan/placement algorithms are effective in estimating the final quality of a design. In terms of fast algorithm, we will argue that for example a fast annealer reveals a lot of information about the difficulty of a design. In terms of approximate algorithms, as an example, we will show that the result of a first-level partition in the placement process teaches us a great deal about the quality of the netlist.

We will outline a framework that allows us to grade the quality and applicability of fast algorithms in the floorplanning/placement process. We will show examples where the proposed framework is successful and where it fails. We will then open the discussion on the applicability of fast and approximate algorithms in the physical design process.