Rent's Rule
Coincidence or the Result of the Design Process?

Dirk Stroobandt*

University of Ghent, ELIS Department
Sint-Pietersnieuwstraat 41
B-9000 Gent, Belgium
dstr@elis.rug.ac.be

The design process for VLSI systems requires several iterations of the physical design cycle. After a partitioning of the circuit and a floorplanning step, the circuit components are placed. The wires between the components are then routed taking the placement into account. A bad placement cannot be solved by a good routing. Therefore, the information obtained during routing generally leads to a new placement step to improve the placement results. A new routing is then performed and so on.

In order to fasten the iteration process and to improve the placement and routing results, it is mandatory to efficiently use estimates of area, wire length, etc. Three kinds of estimates are used: a priori, on line, and a posteriori estimates [1, 2]. The first kind estimates circuit parameters before any of the layout steps (floorplanning, placement, or routing) is performed. On line estimates are obtained during the layout process and are based on the information that results from the layout process itself. A posteriori estimates are obtained after a complete layout step and present the layout results.

A priori estimates need basic information on the circuit to be designed, on the architecture in which it is to be designed, and on the layout process that performs the implementation of the circuit into the architecture [3, 4]. In this position statement, we consider the circuit information.

Apart from the number of gates (or blocks) in the circuit, its number of in- and outputs, its number of nets and number of pins, the most important information is the notion of interconnection complexity of the circuits netlist.

The interconnection complexity information is provided by Rent's rule [5]

$$P = T_b\, B^r$$

where B is the number of gates (blocks) in the circuit, P is the number of pins, and T_b is the average number of terminals per gate (block). The exponent r is called the Rent exponent and is a measure for the interconnection complexity of the circuit. The problem is: "can we rely on the Rent exponent to make a priori estimations?" To answer this question, we have to ask ourselves some related questions:

*The author is Postdoctoral Fellow of the Fund for Scientific Research of Flanders (Belgium).

- Is Rent's rule a coincidence?
  This would be hardly believable since Rent's rule has been found to apply well to several real designs [5, 6, 2]. Moreover, it has been shown that random graphs do not obey Rent's rule. So, Rent's rule is rather specific for "real circuits" and not for "any circuit graph" you could think of.

- Is Rent's rule inherently due to the design process?
  Based on experimental analysis, there are certainly reasons enough to assume this is true. In fact, the design process is hierarchical and the interconnection complexity must be manageable at each hierarchical level. Therefore, it seems reasonable to assume that the conceptual interconnection complexity remains equal at each stage. In that case, we introduce a self-similarity within the circuits structure. Rent's rule is a result of this self-similarity.

  Also, the exceptions to Rent's rule can easily be addressed using our view on interconnection complexity. At the boundaries of the circuit (the inputs and the outputs), the complexity will differ due to two major causes:

  1. Designers change the circuit's number of inputs and outputs because they have to cope with pin limitation problems if they want to implement the circuit in a chip. The number of pins is therefore kept as low as possible. Several techniques can change the pin count (e.g., serializing the output lines) and they generally lower the interconnection complexity but increase the timing complexity (it takes longer for all the output lines to be available at the output pin).
  2. The way information is presented at inputs and outputs. Any algorithm generally takes information at its input in an encoded form. If we have to input an integer value between 0 and 255 to a circuit, we will not use 256 lines and set the line corresponding to the desired integer high. Instead, we will use the binary encoding. That way, we only need 8 lines to present the integer. The same applies to the outputs.

  In both cases, the number of pins is lowered which results in a deviation from Rent's rule, generally known as Rent's region II [5].

  Also, local differences in interconnection complexity do occur in real circuits [7]. Consider a processor. It has cache memory on chip and an ALU. These two blocks have a totally different interconnection complexity since the cache is a rather regular structure while the ALU is not. The first one thus is less complex than the second one. We could say that Rent's rule is not applicable here anymore. We should then split the circuit into two (or more) parts, each with their own Rent exponent. In each of the parts, Rent's rule will result as a fundamental result from the design process but the Rent exponents will be different. However, even in such cases, an "overall Rent exponent" seems to exist as some *average* Rent exponent. In [8], a heterogeneous Rent's rule is presented as an extension to include such variations. The question remains if results based on this heterogeneous Rent's rule are still valid.

- What would happen if the design process was not hierarchical anymore?
  Would Rent's rule still apply for a flatly computer generated netlist? If the self-similarity would also result from the way we describe algorithms, it could well be that this self-similarity is preserved by the design process. In such a view Rent's rule might be not only resulting from the

design process itself but from a combination of the algorithm description and the design process. This would be an interesting research subject.

As a conclusion, we can state that, inside large blocks (e.g., after partitioning and floorplanning), Rent's rule is a result of the self-similarity and can be used for a priori estimations. Of course, this could change if we decide to drastically change the way we design circuits (certainly if the answer to the last question is negative). However, the question if a heterogeneous Rent's rule can be used in the floorplanning phase, remains open.

References

[1] A. E. Caldwell, A. B. Kahng, S. Mantik, I. L. Markov, and A. Zelikovsky. On wirelength estimations for row-based placement. In *Proc. of the 1998 Intl. Symp. on Physical Design*. ACM Press, 1998.

[2] D. Stroobandt. Analytical methods for a priori wire length estimates in computer systems, November 1998. Ph.D. thesis (translated from Dutch), University of Ghent, Faculty of Applied Sciences. Available at http://www.elis.rug.ac.be/˜dstr/dstr.html.

[3] D. Stroobandt, H. Van Marck, and J. Van Campenhout. An accurate interconnection length estimation for computer logic. In *Proc. 6th Great Lakes Symp. on VLSI*, pages 50–55. IEEE Computer Society Press, March 1996.

[4] D. Stroobandt and J. Van Campenhout. Estimating interconnection lengths in three-dimensional computer systems. *IEICE Trans. on Inf. & Syst., Special Issue on Synthesis and Verification of Hardware Design*, vol. E80–D (no. 10): pages 1024–1031, October 1997.

[5] B. S. Landman and R. L. Russo. On a pin versus block relationship for partitions of logic graphs. *IEEE Trans. on Comput.*, vol. C–20: pages 1469–1479, 1971.

[6] W. V. Vilkelis. Lead reduction among combinatorial logic circuits. *IBM Journal of Research and Development*, no. 26: pages 342– 348, 1982.

[7] H. Van Marck, D. Stroobandt, and J. Van Campenhout. Towards an extension of Rent's rule for describing local variations in interconnection complexity. In S. Bai, J. Fan, and X. Li, editors, *Proc. 4th Intl. Conf. for Young Computer Scientists*, pages 136–141. Peking University Press, 1995.

[8] P. Zarkesh-Ha, J. A. Davis, W. Loh, and J. D. Meindl. On a pin versus gate relationship for heterogeneous systems: Heterogeneous rent's rule. In *Proc. of IEEE Custom Integrated Circuit Conf.*, pages 93–96. IEEE, May 1998.