On the Bound of Time-Domain Power Supply Noise Based on Frequency-Domain Target Impedance

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ABSTRACT

One of the popular design methodologies for power distribution networks (PDNs) is to identify a target impedance to be met across a broad frequency range. The methodology is based on the assumption that the ratio of the timedomain maximum output voltage noise to the multiplication of target impedance and time-domain maximum input current is no more than one. In this paper, the ratios for different impedance profiles are analyzed, and the assumption is proved to be not necessarily true. Particularly, for second-order impedances, the maximum ratio can be two. Several cases with real PDN structures are investigated to support our analysis. A real case of the complete PDN path with the ratio of 1.585 is given.

Categories and Subject Descriptors

B.7.1 [Integrated Circuits]: Types and Design Styles— VLSI

General Terms

Theory

Keywords

power distribution network, voltage noise, target impedance

1. INTRODUCTION

Design of power distribution networks (PDNs) becomes a challenging task for nanoscale CMOS technology. As technology advances, supply voltage scales down to less than 1 volt [1]. This brings a tighter noise margin requirement for the PDN. In addition, as circuit density increases, the current density and the total amount of current grow rapidly, causing large IR drops. At the same time, the faster switch-

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ing of transistors produces faster current transients. This results in significant simultaneous switching noise (SSN).

The PDN design objective is to guarantee that the output voltage noise is no larger than a specified value, say, 5% of the nominal supply voltage. One of the most popular PDN design methodologies is to define a target impedance and design the PDN so that its output impedance is no larger than this target impedance over the whole operation frequency range [9, 11, 12]. The target impedance is calculated as [11]

$$Z_{target} = \frac{\text{(power supply voltage)} \times \text{(allowed ripple)}}{\text{current}}, \quad (1)$$

where current is the average current flowing through the PDN. Let V_{max} , Z_{max} (i.e., Z_{target}), and I_{max} denote the maximum magnitude of the worst-case PDN voltage noise v(t), the maximum magnitude of the PDN output impedance $Z(\omega)$, and the maximum magnitude of the time-domain input current i(t), respectively, i.e.,

$$V_{max} = \max_{t} |v(t)|,$$

$$Z_{max} = \max_{\omega} |Z(\omega)|,$$

$$I_{max} = \max_{t} |i(t)|.$$

The assumption behind Eqn. (1) is that V_{max} is less than Z_{max} times I_{max} , i.e., the ratio

$$\gamma = V_{max}/(Z_{max}I_{max}) \tag{2}$$

is no more than 1.

However, since the impedance is a frequency-domain metric while the voltage noise and input current are measured in time domain, such assumption based on Ohm's law does not necessarily hold. Actually, the ratio γ may be larger than 1. The frequency-domain design methodology may lead to a PDN design with much larger power supply noise than expected. For instance, if the allowed noise of a PDN design is 5% of the nominal supply voltage and the ratio γ is 2, then the real maximum noise of the designed PDN may be 10% of the nominal supply voltage, which is not tolerable.

Several works have been done which are related to the time-domain and the frequency-domain response of a linear system [3, 4, 5, 7]. In [4], a method of generating the worst-case PDN voltage noise based on the superposition of step responses is proposed. The effect of pole and zero locations on the locations and magnitudes of the extrema of the step response of a linear system is studied in [7]. The influence of zero locations on the number of extrema in the step re-

sponse is investigated in [5, 3]. However, none of these works provide a quantitative analysis on the relation between the maximum worst-case PDN voltage noise and the peak value of the frequency response magnitude.

The contributions of this paper are as follows. (1) The relationship between the peak of the frequency-domain output impedance and the maximum time-domain voltage noise is analyzed for different impedance profiles. It is proved that for second-order impedances, the maximum ratio γ can be 2. (2) Several cases with real PDN structures are studied to support our analysis. The ratio of a complete PDN path is shown to be 1.585.

The rest of the paper is organized as follows. The problem formulation is given in section 2. The method of generating the worst-case PDN voltage noise is introduced in section 3. In section 4, the ratios for the impedance profiles with right-half-plane zeros are discussed. In section 5, first-order and second-order impedances are analyzed under such constraints. Sections 6 studies real-case PDN structures. Finally, conclusions and future work are remarked in section 7.

2. PROBLEM FORMULATION

We would like to find out the maximum of the ratio γ . Without loss of generality, I_{max} is set to be 1. Thus, the problem formulation is described as

$$max \quad \gamma = V_{max}/Z_{max} \tag{3}$$

$$s.t. I_{max} = 1 (4)$$

In the problem formulation above, the input current i(t) is presumed to be no less than 0. The output impedance Z(s) can be distinguished by two categories: Z(s) without passive realizability constraints and Z(s) with passive realizability constraints. Usually a PDN is modeled by RLC components, which is a passive network. However, if the active voltage regulator module is included, Z(s) may not be passive.

3. WORST-CASE PDN OUTPUT VOLTAGE NOISE

We first need to generate the worst-case voltage noise of the PDN in order to find the maximum γ . In [13], an inequality is given to show the relation between V_{max} , I_{max} and the impulse response of a system, i.e.,

$$V_{max} \le I_{max} ||z(t)||_{L_1}, \tag{5}$$

where z(t) is the impulse response of a system, and $||z(t)||_{L_1}$ is the L_1 norm of z(t), i.e., the step response of the system. In our problem formulation, the input current i(t) is no less than zero and the bound of i(t) is one. From the convolution relation between the output and input of a system, i.e.,

$$V(t) = \int_0^t z(t-\tau)i(\tau) d\tau, \qquad (6)$$

it can be seen that the worst-case voltage response can be created by letting $i(\tau)$ be 1 when $z(t-\tau)$ is larger than 0 and by letting $i(\tau)$ be zero when $z(t-\tau)$ is less than zero.

In [4], Drabkin *et al.* proposed a method of creating the worst-case PDN voltage noise. This method is based on the superposition of step responses and it corresponds to the worst-case generation method based on impulse response

discussed above. Let us assume the unit step response of a PDN is $v_u(t)$. Note that the DC supply voltage is ignored, as usually the case in PDN analysis. The idea is to overlay all the local maximums of $v_u(t)$ and its inverse $-v_u(t)$ (i.e., the inverse of the local minimums of $v_u(t)$) at the same point. The resultant input pattern is the superposition of many reverse time-shifted step inputs and inverse step inputs. The value "1" of the input covers the increasing period of the step response and the value "0" of the input covers the decreasing period of the step response. It can be proved that the method proposed in [4] generates the worst-case output voltage noise:

Theorem of Step Response Derivation. Assuming the input current is no less than zero, the worst-case PDN voltage noise is generated by the superposition of step responses. Let $V_{M1}, V_{M2}, \ldots, V_{MN}$ denote the local maximums of $v_u(t)$ and V_{m1} and V_{m2}, \ldots, V_{mN} denote the local minimums of $v_u(t)$. According to [4], the maximum worst-case voltage noise is derived as

$$V_{max} = V_{M1} - V_{m1} + \ldots + V_{MN} - V_{mN}. \tag{7}$$

The theorem above can be proved by observing that the input current is no less than zero and the impulse response is the derivative of the step response. The increasing of the step response corresponds to the positive value of the impulse response and vice versa.

4. IMPEDANCE WITHOUT REALIZABIL-ITY CONSTRAINTS

This section analyzes the maximum ratios of the output impedance Z(s) without the constraint that Z(s) is realizable by passive components. This imposes no constraints on the locations of the poles or zeros of Z(s). Although a stable network cannot have RHP poles, it may include RHP zeros if there is a feedback system. Therefore, we focus on the impedances with left-half-plane (LHP) poles and RHP zeros in this section.

Claim 1. If the poles of Z(s) are in the left half plane while Z(s) has RHP zeros, there exists a case of Z(s) such that $\gamma=2.405$ under the step response derivation assumption.

RHP zeros may cause undershoots in the step response. According to the assumption of step response derivation, each undershoot represents a local maximum and minimum pair and contributes to the maximum worst-case output voltage noise. If |Z(s)| keeps small over the whole frequency range, γ can also be much larger than 1. For example, there is a family of rational functions called *all-pass Padé delay functions* which are used to approximate the delay unit e^{-sT} . The all-pass Padé delay function can be expressed as [10]

$$R_n(s) = Q_n(-sT)/Q_n(sT), \tag{8}$$

where

$$Q_n(sT) = \sum_{j=0}^n \frac{(n+j)!}{j!(n-j)!} (sT)^{n-j}.$$
 (9)

One of the properties of all-pass Padé delay functions is that their magnitudes are 1 for all the frequencies. However, the step response of an all-pass Padé delay function displays a very narrow undershoot of height about equal to its final value. Take the second-order all-pass Padé delay function for example where n=2 and T=1 in Eqn. (8), then Z(s) is expressed as

$$Z(s) = \frac{s^2 - 6s + 12}{s^2 + 6s + 12}. (10)$$

Its step response can be calculated as

$$v_u(t) = 1 - 4\sqrt{3}e^{-3t}\sin\sqrt{3}t. \tag{11}$$

Eqn. (11) is plotted in Fig. 1, from which we can see that the envelope of the sinusoidal waveform displays a large undershoot.

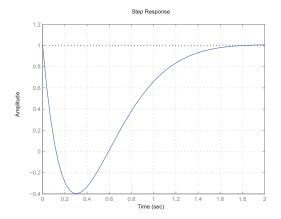


Figure 1: Step response of a second-order all-pass Padé delay function.

We first calculate the values of all the local extrema in the step response. By setting the derivative of Eqn. (11) to be 0 and solving the equation, we have the time points of the local extrema as

$$t_k = (1/6 + k)\pi/\sqrt{3}, \ k = 0, 1, 2, \dots$$
 (12)

Consequently, the values of these extrema are

$$V_{ek} = 1 - 2\sqrt{3}e^{-\sqrt{3}(1/6+k)\pi}(-1)^k, \quad k = 0, 1, 2, \dots$$
 (13)

Then we can calculate the maximum worst-case output voltage noise by using Eqn. (7), i.e.,

$$V_{max} = 1 + 2\sqrt{3} \lim_{k \to \infty} e^{-\sqrt{3}(1/6+k)\pi}$$

 ≈ 2.405 (14)

Since |Z(s)| is 1 over the whole frequency range, the ratio is

$$\gamma \approx 2.405. \tag{15}$$

5. IMPEDANCE WITH REALIZABILITY CONSTRAINTS

In this section, the maximum ratios of Z(s) under the constraints that Z(s) can be realized by passive networks are discussed. A function Z(s) is passive realizable as an impedance if and only if it is a rational positive real function of s. A function F(s) is positive real (p.r.) if the following conditions are satisfied [8]:

- (1) Z(s) is real for real s and is a ratio of polynomials in s.
- (2) $Re[Z(j\omega)] > 0$ for all ω .
- (3) All the poles of Z(s) are in the left half plane, with any poles on the imaginary axis being simple and having positive residues.

In the following sub-sections, the ratios for first-order and second-order Z(s) with the passive realizability constraints are discussed respectively.

5.1 First-order Impedance

Theorem 1. For first-order Z(s) of a passive network, γ is always 1.

PROOF. A first-order Z(s) can be represented as

$$Z(s) = \frac{k}{s - p},\tag{16}$$

or

$$Z(s) = \frac{s-z}{s-p},\tag{17}$$

where k is a constant, z and p are the zero and the pole respectively. To satisfy the realizability constraints, $k \geq 0$, $z \leq 0$ and $p \leq 0$.

(a) For Z(s) expressed by Eqn. (16), the magnitude of Z(s) with frequency can be expressed as

$$|Z(\omega)| = k\sqrt{\frac{1}{\omega^2 + p^2}}. (18)$$

Its step response is represented as

$$v_u(t) = -\frac{k}{p}(1 - e^{pt})u(t).$$
 (19)

Since $p \leq 0$, $v_u(t)$ increases with t while $|Z(\omega)|$ decreases with ω . We can find that $V_{max} = Z_{max} = -k/p$.

(b) For Z(s) expressed by Eqn. (17), the magnitude of Z(s) with frequency can be expressed as

$$|Z(\omega)| = \sqrt{1 + \frac{z^2 - p^2}{\omega^2 + p^2}},$$
 (20)

and its step response is represented as

$$v_u(t) = \left[\frac{z}{p} + (1 - \frac{z}{p})e^{pt}\right]u(t).$$
 (21)

Similarly, we can see that $|Z(\omega)|$ and $v_u(t)$ both increase or decrease monotonically with ω and t respectively. The maximum of $|Z(\omega)|$ and the maximum of $v_u(t)$ are both equal to the larger one of 1 and z/p, i.e., $V_{max} = Z_{max} = max(1, z/p)$.

In summary, $V_{max} = Z_{max}$ for both cases. Thus, the ratio

$$\gamma = 1. \tag{22}$$

5.2 Second-order Impedance

Under passive realizability constraints, all the poles and zeros are in the left half plane, and the highest or lowest powers of the numerator and denominator polynomials may

differ at most by 1 [8]. Thus, a second-order Z(s) can be represented as

$$Z(s) = \frac{s - z_1}{(s - p_1)(s - p_2)},\tag{23}$$

where the poles p_1 , p_2 can be real values or complex conjugate pairs while the zero z_1 can only be real, or

$$Z(s) = \frac{(s-z_1)(s-z_2)}{(s-p_1)(s-p_2)},$$
(24)

where the zeros z_1 , z_2 and the poles p_1 , p_2 can be real values or complex conjugate pairs. The real parts of $z_{1,2}$ and $p_{1,2}$ are no larger than 0 in order to satisfy the realizability constraints, i.e., $Re[z_{1,2}] \leq 0$ and $Re[p_{1,2}] \leq 0$.

For second-order Z(s) with only one zero, i.e., Z(s) expressed in Eqn. (23), we directly give the following claim:

CLAIM 2. For second-order Z(s) with only one zero, there exists a case where $\gamma = 1.062$ under passive realizability constraints. Empirically, for sufficiently large ranges of parameters z_1 , p_1 and p_2 , γ is no more than 1.062.

The result in Claim 2 is obtained by solving a nonlinear programming problem which is similar with the following analysis for second-order Z(s) with complex poles.

In this section, we focus on second-order Z(s) with two zeros, i.e., Z(s) represented in Eqn. (24). We distinguish four categories according to the positions of zeros and poles in the s plane: (1) both the poles and the zeros are real; (2) the poles are real while the zeros are complex conjugate pairs; (3) the poles are complex conjugate pairs while the zeros are real; (4) both the poles and the zeros are complex conjugate pairs. The maximum ratios for each category are investigated respectively.

5.2.1 Real Poles and Real Zeros

CLAIM 3. For second-order Z(s) with two real poles and two real zeros, there exists a class of cases where the ratio γ can be arbitrarily close to 2 under the passive realizability constraints. Empirically, for sufficiently large ranges of parameters z_1 , z_2 , p_1 and p_2 , γ is no more than 2.

For two real poles and two real zeros, the step response of Z(s) can be represented as

$$v_u(t) = K_1 + K_2 e^{p_1 t} + K_3 e^{p_2 t}, (25)$$

where

$$K_1 = \frac{z_1 z_2}{p_1 p_2},$$

$$K_2 = \frac{(p_1 - z_1)(p_1 - z_2)}{p_1(p_1 - p_2)},$$

$$K_3 = \frac{(p_2 - z_1)(p_2 - z_2)}{p_2(p_2 - p_1)}.$$

By setting the derivative of Eqn. (25) to be 0 and solving t, we can find that $v_u(t)$ has a local extremum at the time point

$$t_0 = \frac{1}{p_1 - p_2} ln \left[\frac{(p_2 - z_1)(p_2 - z_2)}{(p_1 - z_1)(p_1 - z_2)} \right]$$
 (26)

as long as t_0 is real and larger than 0.

Firstly let us assume $z_1z_2=p_1p_2$ and $|p_1|\leq |z_1|\leq |z_2|\leq |p_2|$. Then we have |Z(0)|=1 and $|Z(\infty)|=1$. According to the relative positions of the poles and zeros we have

$$Z_{max} = 1. (27)$$

We also find that the step response $v_u(t)$ always has a local minimum for this case. Using Eqn. (7), we can calculate the maximum worst-case voltage noise as

$$V_{max} = v_u(0) - v_u(t_0) + v_u(\infty), \tag{28}$$

where $v_u(0)$, $v_u(t_0)$ and $v_u(\infty)$ can be obtained from Eqn. (25). Since the zeros and the poles are all real, we let $z_1 = kp_1$ and $p_2 = mp_1$, where $1 \le k \le \sqrt{p_2/p_1}$ and $m \ge 1$. According to Eqn. (27) and Eqn. (28), for a fixed m, the ratio γ reaches its maximum when $k = \sqrt{p_2/p_1}$. By setting $k = \sqrt{p_2/p_1}$, γ can be represented solely by m as

$$\gamma = 1 + \frac{(\sqrt{m} - 1)^2}{1 - m} \left(m^{\frac{m}{1 - m}} - m^{\frac{1}{1 - m}} \right). \tag{29}$$

From its derivative we can see that the right hand side of Eqn. (29) is an increasing function on m for $m \ge 1$ and its limit is 2 as m goes to infinity, i.e.,

$$\max \gamma = 2. \tag{30}$$

For general cases, the parameter space of z_1 , z_2 , p_1 , and p_2 is searched for sufficiently large ranges. We first fix the value of p_1 and p_2 , and sweep z_1 and z_2 . For each (p_1, p_2) pair, a local maximum γ is identified. The local maximum γ for different p_1 and p_2 values is shown in Fig. 2. From Fig. 2, we can see that the maximum γ is no larger than 2.

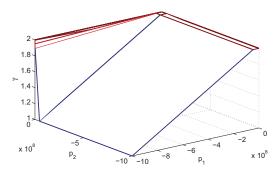


Figure 2: Maximum ratio of second-order Z(s) with real poles and zeros.

The cases where $\gamma \approx 2$ can be realized by passive networks. For example, let $p_1 = -1$, $p_2 = -10000$, and $z_1 = z_2 = -100$, an RLC circuit can be synthesized as shown in Fig. 3. For this case, γ is 1.978, which is close to 2.

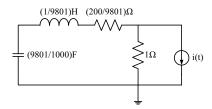


Figure 3: Synthesized passive circuit for maximum ratio with real poles and real zeros.

5.2.2 Real Poles and Complex Zeros

Claim 4. For second-order Z(s) with real poles and complex zeros, there exists a class of cases where the ratio γ can

be arbitrarily close to 2 under the passive realizability constraints. Empirically, for sufficiently large ranges of parameters z_1 , z_2 , p_1 and p_2 , γ is less than 2.

For complex zeros, let $z_{1,2} = a \pm bj$, where $a \leq 0$ and b > 0. The coefficients K_1 , K_2 , K_3 in the step response expressed by Eqn. (25) then become

$$K_1 = \frac{a^2 + b^2}{p_1 p_2},$$

$$K_2 = \frac{p_1^2 - 2ap_1 + a^2 + b^2}{p_1 (p_1 - p_2)},$$

$$K_3 = \frac{p_2^2 - 2ap_2 + a^2 + b^2}{p_2 (p_2 - p_1)}.$$

The step response $v_u(t)$ has a local extremum at the time point

$$t_0 = \frac{1}{p_1 - p_2} ln \left[\frac{p_2^2 - 2ap_2 + a^2 + b^2}{p_1^2 - 2ap_1 + a^2 + b^2} \right]$$
(31)

as long as t_0 is real and larger than 0.

Similarly, we first assume $a^2 + b^2 = p_1 p_2$. According to the relative positions of the poles and zeros we find that

$$Z_{max} = 1. (32)$$

The step response $v_u(t)$ always has a local minimum for this case and V_{max} can also be calculated by Eqn. (28). Let $p_2 = mp_1$, where $m \ge 1$ (assume $|p_1| \le |p_2|$), then for fixed m, the ratio γ reaches its maximum when a = 0. Thus, by setting a = 0, we represent γ solely by m as

$$\gamma = 1 + \frac{m+1}{1-m} \left(m^{\frac{m}{1-m}} - m^{\frac{1}{1-m}} \right). \tag{33}$$

The right hand side of Eqn. (33) is an increasing function on m for $m \ge 1$ and its limit is 2 as m goes to infinity, i.e.,

$$\max \gamma = 2. \tag{34}$$

As in section 5.2.1, we then search the parameter space of a, b, p_1 , and p_2 for sufficiently large ranges. The local maximum γ for different p_1 and p_2 values is shown in Fig. 4, from which we can see that the maximum γ is no larger than 2.

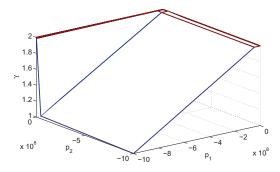


Figure 4: Maximum ratio of second-order Z(s) with real poles and complex zeros.

5.2.3 Complex Poles and Real Zeros

CLAIM 5. For second-order Z(s) with complex poles and two real zeros, there exists a case where $\gamma = 1.047$ under passive realizability constraints. Empirically, for sufficiently large ranges of parameters, $\gamma \leq 1.047$.

Let the complex poles $p_{1,2} = \alpha \pm \beta j$, where $\alpha \leq 0$ and $\beta > 0$. A nonlinear programming problem can be formulated to solve the maximum γ :

$$max \quad \gamma = \frac{V_{max}(z_1, z_2, \alpha, \beta)}{Z_{max}(z_1, z_2, \alpha, \beta)}$$

$$s.t. \quad z_1 \leq 0$$

$$z_2 \leq 0$$

$$\alpha \leq 0$$

$$\beta > 0$$
(35)

Sequential quadratic programming (SQP) method [2] is used to solve this problem. This method solves constrained optimization problems in a similar way as Newton's method for unconstrained optimization. It uses a quasi-Newton method to generate an approximation from the Hessian of the Lagrangian function at each iteration. Then the approximation is used to generate a quadratic programming (QP) subproblem whose solution is used to form a search direction for a line search procedure. The solved maximum γ is

$$\max \gamma = 1.047. \tag{37}$$

And the parameter values for the maximum γ are $z_1 = -7.02 \times 10^6$, $z_2 = -8.38 \times 10^5$, $\alpha = -2.89 \times 105$, and $\beta = 2.89 \times 10^5$.

The local maximum γ for different z_1 and z_2 is shown in Fig. 5. From the figure we can also see that the maximum γ is around 1.047.

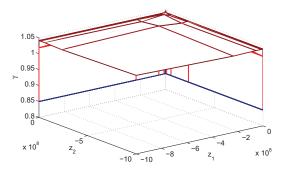


Figure 5: Maximum ratio of second-order Z(s) with complex poles and real zeros.

5.2.4 Complex Poles and Zeros

CLAIM 6. For second-order Z(s) with complex poles and complex zeros, there exists a case where $\gamma=1.815$ under passive realizability constraints. Empirically, for sufficiently large ranges of parameters $\gamma \leq 1.815$.

As in the previous cases, let $p_{1,2} = \alpha \pm \beta j$ and $z_{1,2} = a \pm b j$, and the problem formulation can be written as

$$max \quad \gamma = \frac{V_{max}(a,b,\alpha,\beta)}{Z_{max}(a,b,\alpha,\beta)}$$

$$s.t. \qquad a \le 0$$
(38)

$$b > 0$$

$$\alpha \le 0$$

$$\beta > 0$$
(39)

By solving this nonlinear programming problem using SQP, we find that the maximum γ is

$$\max \gamma = 1.815. \tag{40}$$

The parameter values for the maximum γ are $a = -1.43 \times$ 10^7 , $b = 5.88 \times 10^7$, $\alpha = -2.03 \times 107$, and $\beta = 2.03 \times 10^7$.

The local maximum γ for different a and b is shown in Fig. 6. From the figure we can also see that the maximum γ is around 1.815.

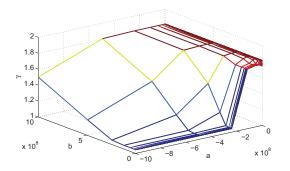


Figure 6: Maximum ratio of second-order Z(s) with complex poles and complex zeros.

REAL-CASE POWER DISTRIBUTION NETWORKS

In this section, the maximum ratios for real-case PDN structures are analyzed. Two standard LC tanks are first considered. One is that without the equivalent series resistance of the capacitor (ESR_C) . The other has an ESR_C with the capacitor. After that, a complete PDN path is discussed.

Standard LC Tank Without ESR_C

Fig. 7 shows a standard LC tank. R and L are to model the parasitic resistance and inductance of the PDN interconnects. C is to model the decoupling capacitors. In this case, C is considered ideal without ESR_C .

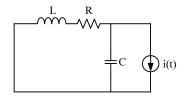


Figure 7: Standard LC tank without ESR_C .

Theorem 2. For the LC tank as in Fig. 7, the maximum ratio γ is 1.041.

PROOF. The output impedance of the LC tank can be represented as

$$Z(s) = \frac{sL + R}{s^2LC + sRC + 1}. (41)$$

Let $\lambda = R^2 C/L$. According to the properties of Z(s), the circuit can be analyzed under the following three categories.

(a)
$$\lambda > 4$$

For this category, Z(s) has real poles and decreases monotonically with frequency. As in section 4.1, we can derive that $Z_{max} = R$ and $V_{max} = R$. Thus, the ratio is

$$\gamma = 1. \tag{42}$$

(b)
$$1 + \sqrt{2} < \lambda < 4$$

For this category, Z(s) has complex poles and decreases monotonically with frequency. Thus, $Z_{max} = R$. As in section 4.2, the maximum worst-case voltage noise can be calculated and the ratio is

$$\gamma = 1 + \sqrt{\frac{1}{\lambda}} \frac{e^{\frac{1}{\sigma} \tan^{-1}(\sigma)}}{1 - e^{\frac{\pi}{\sigma}}},\tag{43}$$

where $\sigma = -\sqrt{4/\lambda - 1}$. (c) $\lambda \le 1 + \sqrt{2}$

$$(c) \ \lambda \le 1 + \sqrt{2}$$

For this category, Z(s) has complex poles and one local maximum. Though tedious, the ratio can be obtained as

$$\gamma = \sqrt{2\sqrt{2\lambda^3 + \lambda^2} - (\lambda^2 + 2\lambda)} \left(1 + \sqrt{\frac{1}{\lambda}} \frac{e^{\frac{1}{\sigma} \tan^{-1}(\sigma)}}{1 - e^{\frac{\pi}{\sigma}}}\right). \tag{44}$$

From Eqn. (42) ~ Eqn. (44), we can obtain that when $\lambda \approx$ 2.12 the maximum ratio

$$\max \gamma \approx 1.041. \tag{45}$$

The ratio γ as a function of λ is plotted in Fig. 8.

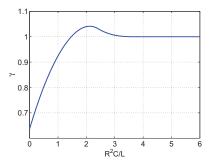


Figure 8: The ratio λ of the LC tank without ESR_C .

6.2 Standard LC Tank With ESR_C

In this sub-section, a resistor is added in series with C to consider the effect of ESR_C , as shown in Fig. 9.

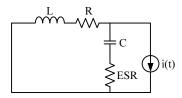


Figure 9: Standard LC tank with ESR_C .

Claim 7. For the LC tank as in Fig. 9, there exists a case where $\gamma = 1.5$. Empirically, for certain ranges of the circuit parameters $\gamma \leq 1.5$.

A nonlinear programming problem can be formulated as

$$max \quad \gamma = \frac{V_{max}(L, C, R, ESR_C)}{Z_{max}(L, C, R, ESR_C)}$$

$$s.t. \quad 10^{-10} \le L \le 10^{-6}$$

$$10^{-10} \le C \le 10^{-6}$$

$$10^{-3} \le R \le 1$$

$$10^{-3} \le ESR_C \le 1.$$

$$(47)$$

The constraints of those parameters are chosen according to the reasonable value ranges of the PDN parameters [11]. This nonlinear programming problem is solved by using SQP method and the maximum ratio is found to be

$$\max \gamma \approx 1.5. \tag{48}$$

The parameter values for the maximum γ are $L=0.1\,nH$, $C=1\,\mu F,\,R=0.52\Omega,$ and $ESR_C=0.52\Omega.$

6.3 Complete PDN Path

In this sub-section, a real PDN case is discussed as in Fig. 10. It is a complete PDN path including VRM, board, package, on-chip power distribution, and decoupling capacitors [6]. The on-chip power grid model is lumped with the package model.

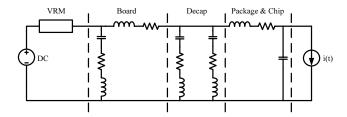


Figure 10: Complete PDN path.

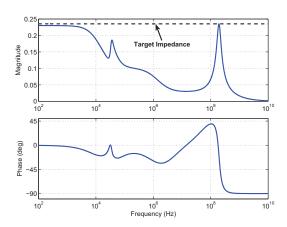


Figure 11: Output impedance of the complete PDN path.

The output impedance of the PDN is shown in Fig. 11. The output impedance displays mainly 2 anti-resonance peaks around $30\,KHz$ and $160\,MHz$. The maximum magnitude of the impedance is

$$Z_{max} = 0.232.$$
 (49)

Those anti-resonance peaks cause low-frequency and high-frequency fluctuations in the PDN step response. By catching the maximums and minimums of the step response and applying Eqn. (7), we can calculate the maximum worst-case voltage noise as

$$V_{max} = 0.368. (50)$$

Thus, the maximum γ for this PDN case is

$$\gamma = 1.585. \tag{51}$$

The worst-case voltage noise of the PDN is displayed in Fig. 12. The corresponding input pattern is plotted in Fig. 13, where the small sub-figure zooms in on the high-frequency transition of the input.

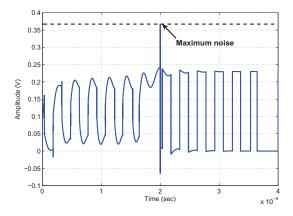


Figure 12: Worst-case voltage noise of the complete PDN path.

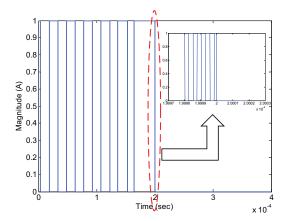


Figure 13: Input pattern for worst-case voltage noise of the complete PDN path.

7. CONCLUSIONS AND FUTURE WORK

In this paper, the ratio of the maximum PDN output voltage noise to the maximum output impedance is analyzed. For second-order Z(s) the maximum γ is found to be 2. A real case of a complete PDN path is given where γ is 1.585. The analysis results contradict the assumption of the well-known "target impedance" design methodology. From the results it can be seen that making output impedance below

the target impedance does not necessarily guarantee a good PDN design.

The future work includes: (1) theoretical analysis of the ratio for the impedances with orders larger than 2, and (2) implementation of a new methodology for PDN design considering both target impedance and the ratio.

8. ACKNOWLEDGEMENTS

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9. REFERENCES

- [1] S. I. Association. International technology roadmap for semiconductors. In http://www.itrs.net.
- M. C. Biggs. Constrained Minimization Using Recursive Quadratic Programming. Towards Global Opptimization, pages 341–349, 1975.
- [3] B. A. L. de la Barra S. On Undershoot in SISO System. *IEEE Transactions on Automatic Control*, 39:578–581, Mar. 1994.
- [4] V. Drabkin, C. Houghton, I. Kantorovich, and M. Tsuk. Aperiodic Resonant Excitation of Microprocessor Power Distribution Systems and the Reverse Pulse Technique. In *IEEE Electrical* Performance of Electronic Packaging, 2002.
- [5] M. El-Kfoury and R. Longchamp. Influence of Zero Locations on the Number of Extrema in the Step Response. In American Control Conference, pages 1192–1194, 1991.

- [6] D. J. Herrell and B. Beker. Modeling of Power Distribution Systems for High-Performance Microprocessors. *IEEE Transactions on Advanced Packaging*, 22(3):240–248, Aug. 1999.
- [7] J. J. H. Mulligan. The Effect of Pole and Zero Locations on the Transient Response of Linear Dynamic Systems. *Proceedings of the IRE*, 37:516–529, May 1949.
- [8] F. F. Kuo. Network Analysis and Synthesis. John Wiley & Sons, Inc., New York, 1962.
- [9] M. Popovich and E. G. Friedman. Impedance Characteristics of Decoupling Capacitors in Multi-power Distribution Systems. In 11th IEEE International Conference on Electronics, Circuits and Systems, pages 160–163, Dec. 2004.
- [10] R.W.Jones. Recursive Estimation of Time-Delay using a High-order Pade Approximant. In SICE Annual Conference, volume 2, pages 1328–1333, Aug. 2004.
- [11] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy. Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology. *IEEE Transactions on Advanced Packaging*, 22(3):284–291, Aug. 1999.
- [12] M. Swaminathan, J. Kim, I. Novak, and J. P. Libous. Power Distribution Networks for System-on-Package: Status and Challenges. *IEEE Transactions on Advanced Packaging*, 27(2):286–300, May 2004.
- [13] K. Zhou, J. C. Doyle, and K. Glover. Robust and Optimal Control. Prentice Hall, New Jersey, 1995.